SIEMENS

ICs für die Unterhaltungselektronik
ICs for Entertainment Electronics

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Typen alphanumerisch geordnet
Types in Alphanumerical Order

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[redacted]			
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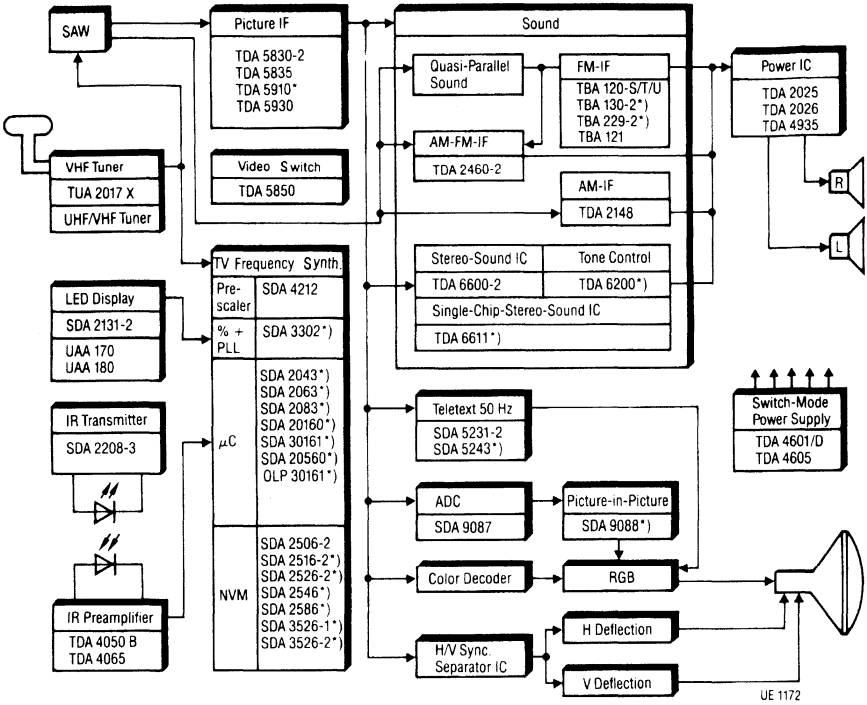
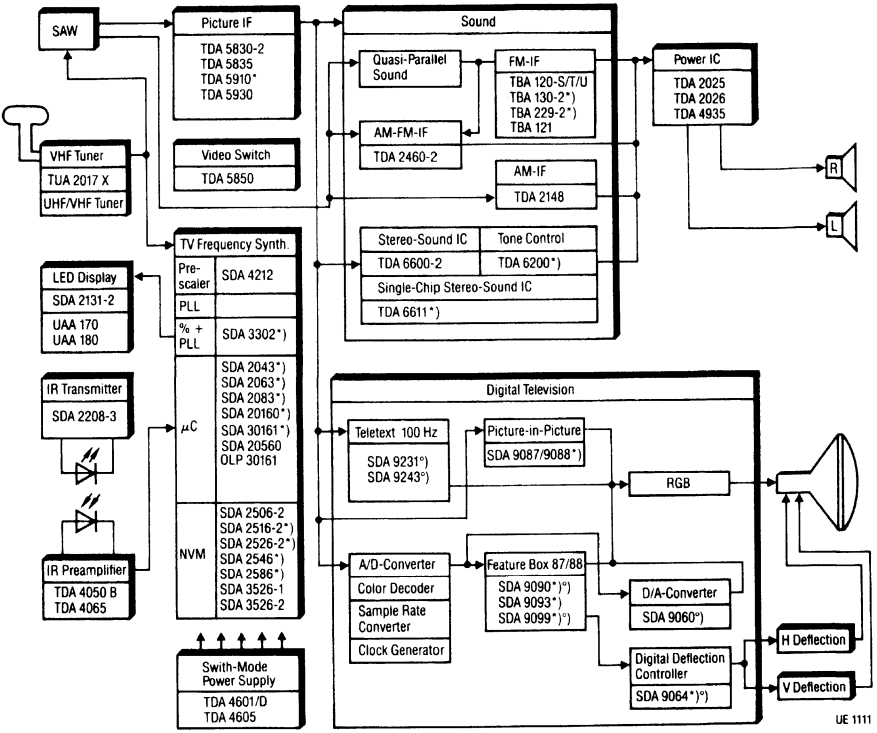
[redacted]



*) ICs mit I²C-Bus
I²C-Bus ist ein patentrechtlich geschütztes Bus-System der Fa. Philips

*) ICs with I²C Bus
I²C Bus is a patented bus system from the Philips Company

ICs für Fernsehgeräte (Typen nach Anwendung geordnet)
ICs for TV Sets (in application-oriented order)



*) With I²C Bus

°) ICs not included in this databook.
Please consult the databook "Flicker Free Television"

ICs für Digitales Fernsehen (Typen nach Anwendung geordnet)
ICs for Digital TV (in application-oriented order)

Funktion Function	Typ Type	Seite Page
Tuner Tuner	TUA 2017-X	738
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Ton-ZF-Verstärker Sound ICs	TDA 2148 TDA 2460-2 TBA 120 T/UB TBA 121 TBA 130-2 TBA 229-2	396 406 343 354 364 377
Stereoton-ICs Stereo Sound ICs	TDA 6200 TDA 6600-2 TDA 6611	632 648 668
Leistungsverstärker Power ICs	TDA 4935	510
Teletext Teletext	SDA 9231 SDA 9243	siehe Datenbuch "Flicker Free TV" see databook "Flicker Free TV"
Picture in Picture Picture in Picture	SDA 9087 SDA 9088	295 315
Feature Box Feature Box	SDA 9090 SDA 9093 SDA 9099	siehe Datenbuch "Flicker Free TV" see databook "Flicker Free TV"
D/A Wandler D/A Converter	SDA 9060	siehe Datenbuch "Flicker Free TV" see databook "Flicker Free TV"
Dig. Deflection Controller Dig. Deflection Controller	SDA 9094	siehe Datenbuch "Flicker Free TV" see databook "Flicker Free TV"
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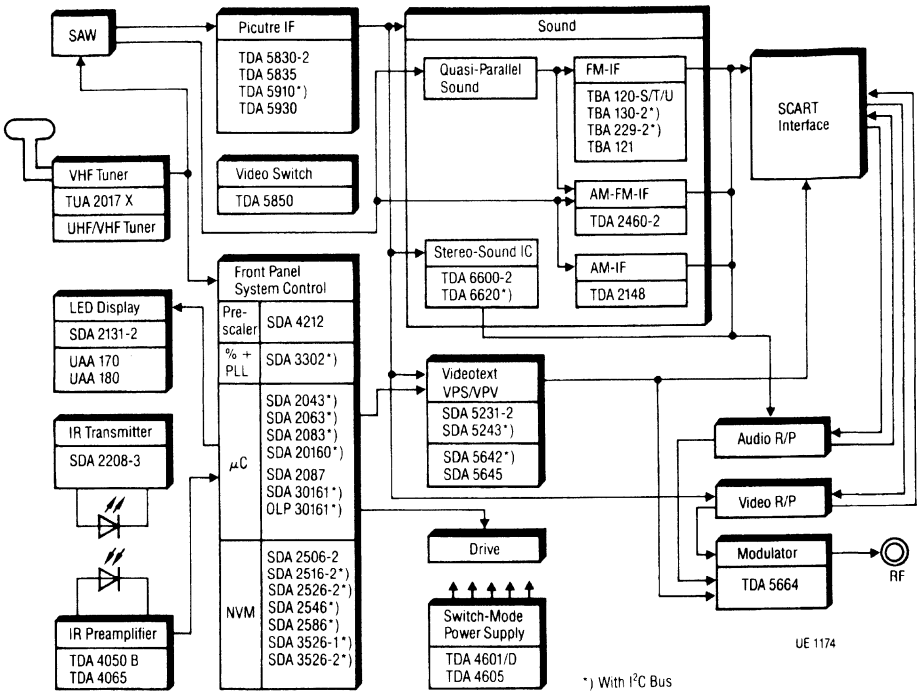
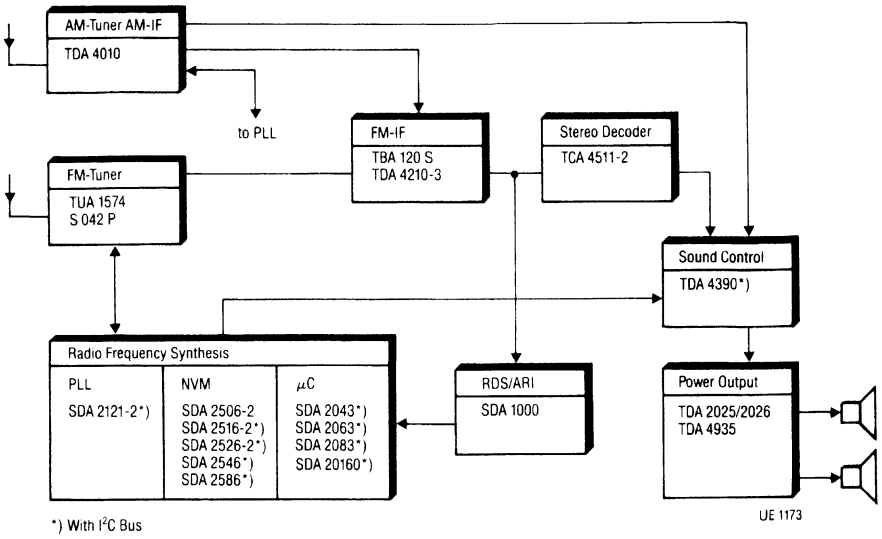


*) With I²C Bus

°) IC's not included in this databook.
Please consult the databook 'Flicker Free Television"

ICs für Videorecorder (Typen nach Anwendung geordnet)
ICs for Video Recorder (in application-oriented order)

Funktion Function	Typ Type	Seite Page
Tuner Tuner	TUA 2017-X	738
LED-Treiber LED Driver	SDA 2131-2 UAA 170 UAA 180	90 752 760
Fernsteuer-ICs Remote Control ICs	SDA 2208-3 TDA 4050-B TDA 4065	97 427 433
Video ZF ICs Video IF ICs	TDA 5830-2 TDA 5835 TDA 5910 TDA 5930 TDA 5850	543 558 577 610 574
Teiler/PLL Prescaler/PLL	SDA 4212 SDA 3302	206 164
Mikrocontroller Microcontroller	SDA 2043 SDA 2063 SDA 2083 SDA 2087 SDA 20160 SDA 20560 SDA 30161 OLP 30161 SDA 30560	69 69 69 70 71 72 73 73 69
Nichtflüchtige Speicher Nonvolatile Memory	SDA 2506-2 SDA 2516-2 SDA 2526-2 SDA 2546 SDA 2586 SDA 3526-1 SDA 3526-2	106 116 128 140 152 182 194
Ton-ZF-Verstärker Sound ICs	TDA 2148 TDA 2460-2 TBA 120 T/UB TBA 121 TBA 130-2 TBA 229-2	396 406 343 354 364 377
Stereoton-ICs Stereo Sound ICs	TDA 6600-2 TDA 6620	648 702
Videotext Videotext	SDA 5231-2 SDA 5243-2 SDA 5642	214 232 280
Modulator Modulator	TDA 5664 TDA 5664-X	524 524
Schaltnetzteil-ICs Switched-Mode Power Supplies	TDA 4601/D TDA 4605	464 492


AM-Tuner AM-IF
TDA 4010
to PLL
FM-IF
TBA 120 S
TDA 4210-3
Stereo Decoder
TCA 4511-2
FM-Tuner
TUA 1574
S 042 P
Sound Control
TDA 4390*)
Radio Frequency Synthesis
PLL
SDA 2121-2*)
NVM
SDA 2506-2
SDA 2516-2*)
SDA 2526-2*)
SDA 2546*)
SDA 2586*)
µC
SDA 2043*)
SDA 2063*)
SDA 2083*)
SDA 20160*)
RDS/ARI
SDA 1000
Power Output
TDA 2025/2026
TDA 4935
UE 1173

*) With I²C Bus

ICs für Autoradios (Typen nach Anwendung geordnet)
ICs for Car Radios (in application-oriented order)

Funktion Function	Typ Type	Seite Page
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FM-ZF FM-IF	TBA 120 T/UB TDA 4210-3	343 420
Stereo-Decoder Stereodecorder	TCA 4511-2	387
PLL PLL	SDA 2121-2	74
Nichtflüchtige Speicher Nonvolatile Memory	SDA 2506-2 SDA 2516-2 SDA 2526-2 SDA 2546 SDA 2586	106 116 128 140 152
Mikrocontroller Microcontroller	SDA 2043 SDA 2063 SDA 2083 SDA 20160	69 69 69 71
Radio-Data-System Radio Data System	SDA 1000	61
Klangregler Tone Control	TDA 4390	447
NF-Leistungsverstärker AF Output Stage	TDA 4935	510

Technische Angaben

Technical Information

1. Typenbezeichnungssystem für integrierte Schaltungen

Für die Typenbezeichnungen der ICs wird das europäische System nach Pro Electron verwendet. Der Bezeichnungsschlüssel ist in der Pro Electron-Broschüre D 15*) Ausgabe 1988 erläutert.

*) Bezugsaddresse: Pro Electron
Avenue Louise, 430 (B.12)
B-1050 Bruxelles, Belgium

2. Einbauhinweise

Kunststoff-Gehäuse

Die Anschlüsse der Gehäuse sind um 90° nach unten abgebogen und passen in ein Lochraster von 2,54 mm, Lochkreisdurchmesser 0,7 bis 0,9 mm. Das Maß X ist der entsprechenden Gehäusezeichnung zu entnehmen.

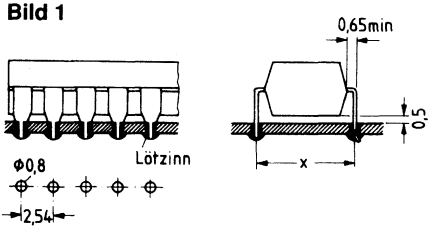
Der Gehäuseboden berührt nach dem Einsetzen die Leiterplatte nicht, weil die Anschlußfahnen kurz vor dem Gehäuse breiter werden (**siehe Bild 1**).

Nach dem Einsetzen des Gehäuses in die Leiterplatte ist es vorteilhaft, zwei Anschlußenden in einem Winkel von ca. 30° zur Leiterplatte abzubiegen, während des Lötvorgangs braucht dann das Gehäuse nicht auf die Leiterplatte gepreßt zu werden.

Kunststoff-Steckgehäuse werden auf der dem Gehäuse abgewandten Plattenseite gelötet.

Die maximal zulässige Löttemperatur beträgt bei Handlötung 350 °C (max. 3 s) und bei Tauchlötung und Schwallötung 260 °C (max. 10 s).

Bild 1



Leistungs-Gehäuse mit 5, 7 und 9 Anschlüssen

Leistungsgehäuse weisen i.A. breitere Anschlüsse auf, so daß der erforderliche Lochkreisdurchmesser bei Leiterkarten 1,1 – 1,8 mm beträgt. Bei einem eventuellen Biegen der Anschlüsse darf keine mechanische Beanspruchung zwischen Anschlüssen und Gehäuse auftreten. Der Abstand vom Gehäuse zur Biegestelle ist min. 2 mm.

Kunststoff-Gehäuse (P-DSO und PL-CC) für die Oberflächenmontage (SMD)

Kolbenlötung:	Löttemperatur 350 °C max. 3 s. Abstand Gehäuse zur Lötstelle 1,5 mm min. Gehäusetemperatur max. 150 °C, keine mechanische Belastung der Anschlüsse zum Gehäuse
Dampfphasenlötung:	Löttemperatur 215 °C, Lötzeit max. 40 s, 2 ×. (Vapor Phase Soldering)
Schwallötung:	Löttemperatur 260 °C, Lötzeit max. 8 s. (Anschlüsse und Gehäuse in das Zinnbad getaucht)

Lagerung, Vorbehandlung zur Weiterverarbeitung von ICs in PL-CC-Gehäusen

Die Bauelemente sind trocken zu lagern. Bei der Anwendung von Lötverfahren, die zu Hitzeschockbelastungen führen können, (z.B. Dampfphasenlöten) empfiehlt es sich ICs im PL-CC-Gehäuse 24 Stunden einem Trocknungsvorgang bei 125 °C zu unterziehen.

Sonstige Hinweise

Es ist darauf zu achten, daß zwischen Lötbad bzw. Lötkolben und Platine keine Ströme fließen können. Es wird daher empfohlen, die zu lötenden Anschlüsse und das Lötbad bzw. den Lötkolben an Masse zu legen.

Beim Vorbereiten und Einsetzen in die Platine sollen die Schaltungen vor statischer Aufladung geschützt werden. Auf keinen Fall dürfen die Bauteile bei eingeschalteter Betriebsspannung aus der Schaltung entnommen werden bzw. in die Schaltung eingefügt werden.

Die Erhöhung der Chiptemperatur beim Löten hat eine vorübergehend erhöhte elektrostatische Empfindlichkeit der integrierten Schaltungen zur Folge. Besondere Vorsicht ist daher vor Netztransienten, z.B. durch Schalten von Induktivitäten an Magnetrutschen usw. geboten.

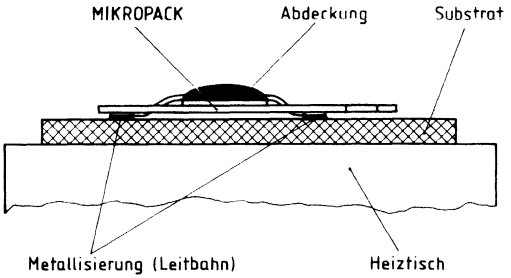
MIKROPACK-Bauform (SMD)

Die Anlieferung der MIKROPACK-Bauformen erfolgt auf Filmrollen.

Einbauvorschläge

a) Wir empfehlen Dampfphasenlötung: Löttemperatur 215 °C, Lötzeit max. 40 s.
b) Für Mustereinbau und kleinere Stückzahlen (bis z.B. 50.0 Stck/J.) ist auch Heiztischlötung (**Bild 3**) anwendbar.

Bild 3



Benötigte Vorrichtungen und Hilfsmittel

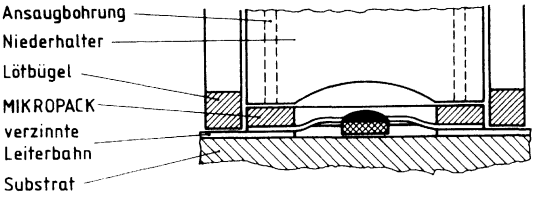
- Schneidevorrichtung
- Heiztisch-, Temp.-geregelt (z.B. Fa. Weld-Equip, Unitek)
- Stereomikroskop (z.B. Wild, Fa. Zeiss, Vergrößerung 6...40fach)
- Substratmaterial: Epoxydharz, Hartpapier, Keramik (Dick-Dünnschicht)

Lötdaten

- Löttemperatur: 210 °C max.
- Lötbeschichtung auf Substrat: Pb/Sn (z.B. 60/40), schwallverzinnt oder galvanisch abgeschieden
- Lötzeit: ca. 10 s
- Flußmittel: z.B. Kolophonium in Alkohol gelöst
- Reinigungsmittel (bedarfsweise): z.B. Freon TP-35, TE, TF

c) Für größere Stückzahlen (z.B. 50.0 Stck/J.) kommt auch die Bügellötung (**Bild 4**) in Frage.

Bild 4



Benötigte Vorrichtung

- Lötvorrichtung (z.B. Fa. Weld-Equip, Fa. Farco, Fa. Jade)
- Substratmaterial: Epoxydharz, Hartpapier, flexible Materialien z.B. Polyamid

Lötdaten

- Löttemperatur: 220 °C max.
- Lötbeschichtung auf Substrat: Pb/Sn (z.B. 60/40), schwallverzinnt oder galvanisch abgeschieden
- Lötzeit: ca. 10 s
- Flußmittel: z.B. Kolophonium in Alkohol gelöst
- Reinigungsmittel (bedarfsweise): z.B. Freon TP-35, TE, TF

3. Verarbeitungsrichtlinien für integrierte Schaltungen

Integrierte Schaltungen sind **e**lektrostatisch **g**efährdete **B**auelemente (EGB). Die Forderung nach immer größeren Integrationsdichten hat zu immer kleineren Strukturen auf den Halbleiterchips geführt, so daß heute grundsätzlich jede integrierte Schaltung bipolar, MOS und CMOS elektrostatisch geschützt werden muß.

MOS- und CMOS-Schaltungen enthalten meist in den Bausteinen integrierte Schutzschaltungen und sind durch rein statische Elektrizität kaum mehr zerstörbar. Andererseits besteht eine akute Gefährdung durch elektrostatische Entladungen (ESD = **E**lectro**s**tatic **D**ischarge).

Von der Vielzahl möglicher Entladungsquellen sind neben aufgeladenen Personen vor allem aufgeladene Bausteine zu nennen. Bei niederohmigen Entladungen können Spitzenleistungen im kW-Bereich auftreten.

Zum Schutz der Bausteine sind folgende Grundsätze zu beachten:

a) Verringerung der Aufladungsspannung - möglichst unter 220 V.
Wirksame Mittel sind die Erhöhung der relativen Luftfeuchte auf ≥ 60% und das Ersetzen hochaufladbarer Kunststoffe durch antistatische Werkstoffe.

b) Bei jeglicher Berührung der Bausteinanschlüsse ist mit einem Ladungsausgleich zu rechnen. Dieser soll stets hochohmig (ideal $R = 10^6$ bis $10^9\ \Omega$) erfolgen.

Zusammengefaßt heißt dies, daß integrierte Schaltungen eine besondere Handhabung erfordern, da unkontrolliert aufgebrachte Ladungen, Spannungen von nicht geerdeten Geräten oder Personen, Überspannungsspitzen oder andere ähnliche Einflüsse das Bauelement zerstören können. Selbst wenn die Bauelemente Schutzschaltungen (z.B. Schutzdioden) an den Eingängen enthalten, müssen nachfolgende Handhabungsrichtlinien beachtet werden.

Kennzeichnung

Die Verpackung elektrostatisch gefährdeter Bauelemente wird mit folgendem Kennzeichen herstellerseitig versehen: 

Geltungsbereich

Diese Richtlinie gilt für Lagerung, Transport, Prüfung und Verarbeitung aller Arten von integrierten Schaltungen, bestückten und gelöteten Leiterplatten, die mit solchen Bauelementen versehen sind.

Handhabung der Bauelemente

1. Integrierte Schaltungen müssen bis zu ihrer Verarbeitung in der Verpackung bleiben.
2. Die Handhabung von integrierten Schaltungen darf nur an speziell eingerichteten Arbeitsplätzen erfolgen. Diese Plätze müssen hochohmig leitende Beläge in der Größenordnung von 10^6 bis $10^9\ \Omega$/cm haben.
3. Bei Luftfeuchten > 50% genügt ein Arbeitsmantel aus reiner Baumwolle. Bei Verwendung von aufladbaren Kunstfasern soll die Kleidung enganliegend getragen werden. Das Handgelenkband muß fest an der Haut anliegen und über einen Ableitwiderstand von 50 kΩ bis 100 kΩ geerdet sein.

4. Sind elektrisch leitende Fußböden $R_E = 5 \times 10^4$ bis 10^7 Ω vorhanden, dann kann durch Verwendung von sog. MOS-Stühlen und Schuhen mit elektr. leitender Sohle ($R_E \approx 10^5$ bis 10^7 Ω) ein weiterer Schutz erzielt werden.
5. Alle Transporteinheiten für elektrostatisch gefährdete Bauelemente und bestückte Leiterplatten müssen zuerst durch Abstellen auf dem Arbeitsplatz bzw. Anfassen durch das beschäftigte Belegschaftsmitglied auf das gleiche Potential gebracht werden, bevor nach den einzelnen MOS-Bauelementen gegriffen wird. Der Potentialausgleich soll über einen Widerstand von 10^6 bis 10^8 Ω erfolgen.
6. Beim Beschicken von Maschinen und Fertigungseinrichtungen ist zu beachten, daß die Bausteine aufgeladen aus der Versandstange kommen und bei metallischer Berührung beispielsweise mit Maschinenteilen Schaden nehmen können.

   Beispiel 1) volumenleitende (schwarze) Schienen.
   Bausteine können durch aufgeladene Personen u.U. in der Schiene zerstört werden,
   oder die Schiene aufgeladen verlassen, wenn diese von einer aufgeladenen Person entleert wird.
   Volumenleitende Schienen dürfen nur an EGB-Arbeitsplätzen (hochohmige Arbeitsplatz- und Personenerdung) gehandhabt werden.

   Beispiel 2) antistatisierte (transparente) Schienen.
   Bausteine können durch aufgeladene Personen in der Schiene nicht zerstört werden (seltene Ausnahme kann es bei kundenspezifischen ICs mit ungeschützten Gate-Anschlüssen geben). Eine Bausteingefährdung ist wie bei 1) beim Entleeren der Schiene gegeben, wenn diese insbesondere bei geringeren Luftfeuchten nach längerer Lagerzeit ($t >$ 1 Jahr) nicht mehr genügend antistatisiert ist.

   In beiden Fällen können Schädigungen dadurch vermieden werden, daß die Bausteine über einen geerdeten Adapter aus hochohmigem Material ($\approx 10^6$ bis 10^8 Ω/cm) zwischen Schiene und Maschine entladen werden.

   Von der Verwendung metallischer Schienen - insbesondere aus eloxiertem Alu - wird wegen der Gefahr niederohmiger Bausteinentladungen abgeraten.

Lagerung

Die Einlagerung von EGB nur an bestimmten, gekennzeichneten Lagerplätzen vornehmen.

Im Lager sollen die Bauelemente in der Anlieferverpackung verbleiben. Die Lagertemperatur sollte 60 °C nicht übersteigen.

Transport

EGB in zugelassenen Verpackungsschienen dürfen nur in geeigneten Behältern aus hochohmig leitenden bzw. langzeitantistatisch imprägnierten Kunststoffen evtl. unlackiertem Holz transportiert werden. Behälter aus hochaufladbaren Kunststoffen oder aus sehr niederohmigen Materialien sind gleichermaßen ungeeignet.

Transportwagen und dessen Rollen sollen eine hinreichende elektrische Leitfähigkeit besitzen ($R < 10^6$ Ω). Schleifkontakte und Erdungsketten bieten keine zuverlässige Ladungsableitung.

Eingangsprüfung

Bei Eingangsprüfungen sind die Richtlinien zu beachten. Andernfalls erlischt ein evtl. Rückgaberecht bei Nichtbestehen der Eingangsprüfung.

Betriebsmittel und Montage

1. Antriebsriemen von verarbeitenden Maschinen, soweit sie mit diesen Bauelementen in Berührung kommen (z.B. Biege- und Beschneidemaschinen, Transportbänder), sind mit Antistatikspray (z.B. Antistatikspray 100 der Fa. Kontaktchemie) zu behandeln. Besser ist es, solche Fälle ganz zu vermeiden.
2. Müssen EGB von Hand ein- oder ausgelötet werden, sind nur Lötkolben ohne Thyristorregelung zu verwenden. Gegen Netztransienten haben sich Siemens Funkentstörkondensatoren vom Typ B 81711-A-B31...36 sehr gut bewährt.
3. Mit EGB bestückte und gelötete Leiterplatten sind grundsätzlich als gefährdet zu betrachten.

Elektrische Prüfungen und Anwendungsschaltung

1. Die Bauelemente sind unter Beachtung dieser Richtlinien zu verarbeiten. Vor dem Prüfen der bestückten und gelöteten Leiterplatten sind noch eventuell vorhandene Kurzschlußringe abzunehmen.
2. Prüffassungen bzw. integrierte Schaltungen müssen beim Stecken oder Ziehen von Einzelbauelementen oder bestückten Leiterplatten spannungsfrei sein, wenn in den entsprechenden Werksunterlagen nichts anderes angegeben ist. Es ist sicherzustellen, daß die Prüfgeräte und Stromversorgungen keine Spannungsspitzen erzeugen, weder bei betriebsmäßigem Ein- und Ausschalten noch beim Ausfall der Netzsicherung oder beim Ansprechen anderer Sicherungen.
3. Bei der Stromversorgung bipolarer integrierter Schaltungen ist immer zuerst die negative Spannung ($-U_S$ bzw. Masse) anzuschließen. Eine Unterbrechung dieses Potentials im Betrieb ist in der Regel nicht zulässig.
4. Signalspannungen dürfen an Eingängen der integrierten Schaltungen erst mit oder besser nach dem Einschalten der Versorgungsspannung angelegt werden. Sie müssen mit oder möglichst vor dem Abschalten der Versorgungsspannung abgeschaltet werden.
5. Stromversorgungen von integrierten Schaltungen sind möglichst nahe an den Versorgungsanschlüssen des ICs abzublocken. Bei bipolaren integrierten Schaltungen ist die Verwendung eines induktivitätsarmen Elektrolytkondensators, zumindest jedoch die Parallelschaltung eines Keramikkondensators von z.B. 100 nF bis 470 nF empfehlenswert.
   Bei integrierten Schaltungen mit hohen Ausgangsströmen muß der nötige Wert des Elektrolytkondensators der Prüf- bzw. Anwendungsschaltung angepaßt werden. Zu berücksichtigen sind Einschwingverhalten und dynamischer Ausgangswiderstand der Stromversorgungen, Leitungsinduktivitäten im Versorgungs- und Lastkreis und insbesondere induktive Lasten oder Motoren. Beim Abschalten von Leistungsinduktivitäten oder induktiver Lasten muß die gespeicherte Energie, wenn nicht anders angegeben, extern aufgenommen werden (z.B. durch einen Elektrolytkondensator, Dioden, Z-Dioden oder die Stromversorgung). Dabei ist auch ein Abschalten der Versorgungsspannung vor dem Zeitpunkt der Lastabschaltung zu beachten.

6. Integrierte Schaltungen mit Tiefpasscharakter der Ausgangsstufen (z.B. PNP-Treiber oder PNP/NPN-Endstufen) benötigen in der Regel eine zusätzliche externe Kompensation am Ausgang. Dies gilt insbesondere bei komplexen Lasten. Bei NF-Leistungsverstärkern wird der Ausgang mit dem Boucherot-Glied kompensiert. Bei Brückenschaltungen genügt im Einzelfall die Überbrückung der Last mit einer Kapazität. Je nach Anwendung ist aber auch hier je ein Kondensator von jedem Ausgang gegen Masse zu empfehlen.
7. Die Hinweise mit den jeweiligen Datenbüchern sind zu beachten.

Verpackung von bestückten Leiterplatten bzw. Flachbaugruppen

Das Verpackungsmaterial soll eine geringe Volumenleitfähigkeit besitzen:
$10^5\Omega/cm < \rho < 10^{10}\Omega/cm$.

In den meisten Fällen – insbesondere bei Luftfeuchten > 40% – wird diese Forderung von einfacher Wellpappe erfüllt.

Einen besseren Schutz erzielt man mit Beuteln aus hochohmig leitfähigem Polyäthylenschaum; (z.B. RCAS 1200 von Richmond, Redlands, Californien; Vertreter Deutschland: Arno Marx, 7830 Emmendingen, Postfach 1129).

Grundsätzlich ist darauf zu achten, daß eine Berührung verschiedener Platinen ausgeschlossen wird.

In extremen Sonderfällen kann ein Schutz vor starken elektrischen Feldern notwendig sein, wie sie beispielsweise von Transportbändern erzeugt werden können.

Hierfür wird eine Umhüllung mit Alu-Folie empfohlen, wobei eine direkte Berührung der Folie mit der Platine ausgeschlossen werden muß.

Pappschachteln mit innenliegender Alu-Folie, wie sie zum Versand unserer Bausteine verwendet werden, liefert z.B. Fa. Laber, München.

Ultraschallreinigung integrierter Schaltungen

Nachfolgende Empfehlung gilt für Kunststoffgehäuse. Für Hohlraumgehäuse (Metall und auch Keramik) sind gesonderte Vorschriften zu beachten.

Als Lösungsmittel kommen Freon und Isopropylalkohol (Handelsname Propanol) in Frage. Diese Lösungsmittel sind auch für Kunststoffgehäuse zulässig, da sie das Plastikmaterial nicht angreifen.

Ein Ultraschallbad in Doppel-Halbwellen-Betrieb ist aufgrund der geringen Bauteilebeanspruchung zu empfehlen.

Folgende Ultraschallwirkungen sind zulässig:

Schallfrequenz	$f > 40$ kHz
Einwirkungszeit	$t < 2$ min
Schallwechseldruck	$p < 0{,}3$ atü
Schalleistung	$N < 0{,}5$ W/cm²/Liter

4. Beschreibung der Datenangaben

Grenzdaten

Die Grenzdaten sind absolute Grenzwerte, bei deren Überschreitung auch nur eines Wertes die integrierte Schaltung zerstört werden kann.

Kenndaten

Die Kenndaten umfassen den garantierten Streubereich der Werte, die im angegebenen Betriebsbereich von der integrierten Schaltung eingehalten werden.

Unter den typischen Kenndaten werden Mittelwerte angegeben, die fertigungsmäßig erwartet werden. Wenn nicht anders vermerkt, gelten die typischen Kenndaten bei T_U = 25 °C und angegebener Speisespannung.

Funktionsdaten

Im Funktionsbereich werden die in der Schaltungsbeschreibung angegebenen Funktionen erfüllt.

5. Angaben zur Qualität

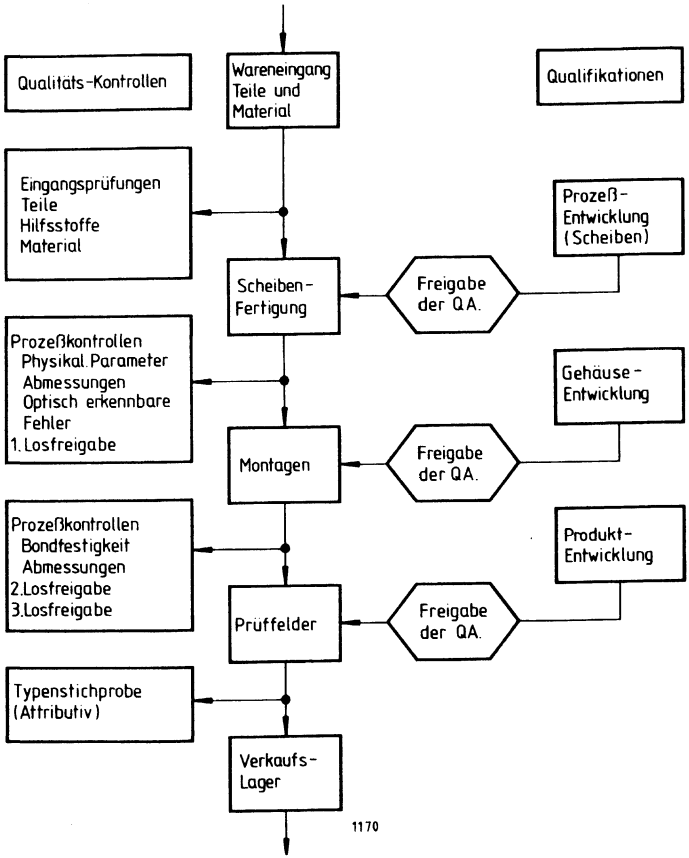
Qualitätssicherungssystem

Der hohe Qualitätsstandard der integrierten Schaltungen von Siemens ist das Ergebnis eines sorgfältigen Herstellungsprozesses, der in jeder Phase systematisch überwacht wird. Dazu dient ein Qualitätssicherungssystem, das in der Druckschrift "SIEMENS Qualitätssicherung bei Integrierten Schaltungen", kurz "SQS-IC", ausführlich beschrieben ist.

Die wichtigsten Aspekte des "SQS-IC" sind in **Bild 6** dargestellt. Für die ausgewählten Kontrollmaßnahmen, Freigaben und Informationsrückkopplungsschleifen ist eine, von der Entwicklung und Fertigung unabhängige Qualitätssicherungsabteilung (QA) verantwortlich. Diese Abteilung verfügt über modernste Prüf- und Meßeinrichtungen, sie arbeitet mit den bewährten Methoden der statistischen Qualitätskontrolle, und sie ist mit Einrichtungen für beschleunigte Lebensdauer- und Umweltkontrolltests ausgestattet, die zu Eignungs- und Routineüberwachungsprüfungen eingesetzt werden.

Zur ständigen Weiterentwicklung von Qualität und Zuverlässigkeit werden modernste Präparationsmethoden und Analysegeräte eingesetzt.

Bild 6


Qualitäts-Kontrollen
Wareneingang Teile und Material
Qualifikationen
Eingangsprüfungen Teile Hilfsstoffe Material
Prozeß-Entwicklung (Scheiben)
Scheiben-Fertigung
Freigabe der Q.A.
Prozeßkontrollen Physikal. Parameter Abmessungen Optisch erkennbare Fehler 1. Losfreigabe
Gehäuse-Entwicklung
Montagen
Freigabe der Q.A.
Prozeßkontrollen Bondfestigkeit Abmessungen 2. Losfreigabe 3. Losfreigabe
Produkt-Entwicklung
Prüffelder
Freigabe der QA.
Typenstichprobe (Attributiv)
Verkaufs-Lager
1170

Auslieferungsqualität

Jede integrierte Schaltung wird als Abschluß des Fertigungsprozesses einer Endprüfung unterzogen. Da diese Prüfung häufig Hunderttausende von Betriebszuständen, viele statische und dynamische Parameter zu berücksichtigen hat, wird sie von rechnergesteuerten Prüfautomaten durchgeführt. Diese Automaten sind äußerst zuverlässig. Die Qualitätssicherungsabteilung führt schließlich eine losweise Stichprobenprüfung der ICs durch, um so diese minimale Fehlerquote sowie die Herstellungsgrenzqualität (AQL) zu gewährleisten. Die Stichprobenprüfung bedient sich der Stichprobenpläne der DIN 40080 oder der identischen MIL-STD-105 oder IEC 410.

Die Ergebnisse solcher Stichprobenprüfungen, die an vielen Hunderttausenden von ICs im Jahre 1987 durchgeführt wurden, sind in der nachfolgenden Tabelle wiedergegeben. Diese Ergebnisse entsprechen der mittleren Auslieferungsqualität (Average Outgoing Quality, kurz: AOQ) und werden in "**d**efectives **p**er **m**illion" (DPM) angegeben.

	Total-fehler AOQ (DPM)	Summe elektr. Fehler AOQ (DPM)	Summe mech. Fehler AOQ (DPM)
LSI/VLSI ≥ 1000 Gatterfunktionen	90	144	250

Zuverlässigkeit

Maßnahmen bei der Entwicklung

Die Zuverlässigkeit der ICs wird bereits während der Entwicklung wesentlich beeinflußt. Deshalb hat Siemens für die Entwicklung der Schaltungen und Layouts Entwurfsregeln festgelegt, die u.a. die minimalen Breiten und Abstände von Leitbahnen auf dem Chip festlegen, die Abmessungen und elektrischen Parameter von Schutzschaltungen gegen elektrostatische Aufladungen angeben, und ähnliches mehr. Ausgefeilte Überprüfungsprogramme, die auf Großrechnern laufen, garantieren eine umgehende Lokalisierung und Behebung unbeabsichtigt eingetretener Verstöße gegen diese Entwurfsregeln.

Prozeßkontrolle in der Fertigung

Die Herstellung integrierter Schaltungen umfaßt mehrere hundert Fertigungsschritte. Da jeder Schritt fehlerfrei ausgeführt sein soll, kommt der Prozeßkontrolle eine überragende Bedeutung zu. Manche Prozesse enthalten mehr als hundert Kontrollmaßnahmen. Die Kontrollen sind so angelegt, daß die Stabilität der Prozeßparameter der Fertigungsschritte gesichert ist.

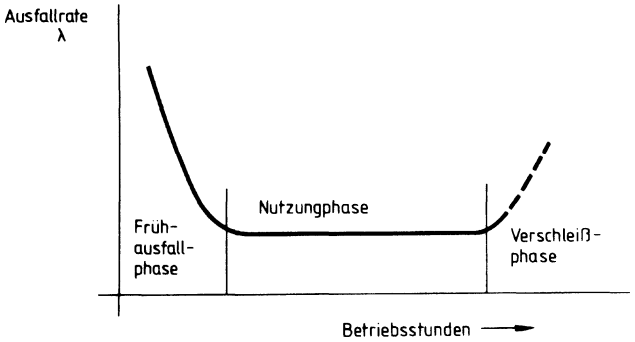
In den ständig sinkenden Ausfallraten zeigen sich die Erfolge dieser Bemühungen; im Laufe der Jahre wurde die Ausfallrate wesentlich reduziert, und dies trotz der erheblich gestiegenen Komplexität der ICs.

Beispielsweise konnte im Jahr 1987 bei beschleunigten Lebensdauertests an etwa 2 Millionen ICs mit verschiedener Komplexität eine durchschnittliche Langzeitausfallrate von etwa 80 Fit abgeschätzt werden.

Zuverlässigkeitsüberwachung

Der allgemeine Verlauf der Ausfallrate bei ICs über die Zeit wird durch die sogenannte Badewannenkurve beschrieben (**s. Bild 7**). Die Ausfallrate ist in den ersten Betriebsstunden am höchsten (Frühausfallphase). Nach Abklingen der Frühausfallphase beginnt die "konstante" Ausfallphase, während der Ausfälle in einer nahezu gleichbleibenden Anzahl auftreten können. Diese Phase endet mit einem Wiederanstieg der Kurve während der Verschleißphase. Für integrierte Schaltungen liegt diese Phase in aller Regel weit über der praktischen Betriebszeit der Geräte.

Bild 7



Zuverlässigkeitsuntersuchungen an ICs sind in der Regel zerstörende Untersuchungen. Sie werden daher in Stichproben durchgeführt. Die meisten Ausfallmechanismen laufen bei höheren Temperaturen schneller ab. Auf Grund dieser Temperaturabhängigkeit, kann die zur Simulation späterer Betriebsverhalten geforderte Zeit durch Anwenden höherer Temperaturen verkürzt werden; hierunter versteht man den Lebensdauertest.

Der Beschleunigungsfaktor F im Lebensdauertest errechnet sich aus der Arrheniusschen Gleichung

$$F = \exp\left(\frac{E_A}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

wobei T_2 die Temperatur ist, bei welcher der Lebensdauertest durchgeführt wird, T_1 die angenommene Betriebstemperatur und k die Boltzmann-Konstante ist.

Maßgebend für den Faktor F ist die Aktivierungsenergie E_A, die für Ausfallmechanismen sehr unterschiedlich ist und zwischen 0,3 und 1,3 eV liegt.

Für alle Siemens ICs werden Zuverlässigkeitsangaben aus Lebensdauertestuntersuchungen mit einer mittleren Aktivierungsenergie von 0,5 eV auf eine Betriebstemperatur von T_U = 55 °C umgerechnet. Damit ergibt sich ein Beschleunigungsfaktor für den Lebensdauertest von 24 gegenüber dem Betriebsverhalten. So werden auch Ausfallmechanismen berücksichtigt, die eine geringe Aktivierungsenergie haben, d.h. in geringer Weise durch die Temperaturauswirkung beschleunigt werden.

An Typen von integrierten Schaltungen, die repräsentativ sind für die Fertigungslinien, werden - wie in der "SQS-IC" beschrieben - routinemäßig verschiedene Zuverlässigkeitsprüfungen durchgeführt. Solche Prüfungen sind u.a. Feuchtklima-Tests bei 85 °C und 85% Feuchte, Dampfdruck-Test, sowie Lebensdauerprüfungen bis 1000 Stunden und mehr. Die Untersuchungsergebnisse liegen in Form zusammenfassender Berichte vor.

A, B	Indizies für Grenzwert
AC	Wechselspannung
AM	Amplitudenmodulation
B	Bandbreite
C	Kapazität
C_i, C_I	Eingangskapazität
C_T, C_{CLK}, C	Taktkondensator
CLK	Takt
DC	Gleichspannung
D	Differentiell
f	Frequenz
Δf	Hub
FM	Frequenzmodulation
f_i, f_I	Eingangsfrequenz
f_q, f_Q	Ausgangsfrequenz
G	Gleichwellenunterdrückung
G	giga (10^9)
GND	Masse
Hy	Hysterese
HF	Hochfrequenz
Hz	Hertz (1/s)
i, I	Eingang
I, i	Strom
I_S	Stromaufnahme
k	Klirrfaktor
k	kilo (10^3)
K	Kelvin
L	Induktivität
m	milli (10^{-3})
M	Mega (10^6)
m	Modulationsfaktor
MW	Mittelwelle
N, R	Geräusch, Rauschen
NF	Niederfrequenz
o	offset
OSZ	Oszillator
P, P_V	Verlustleistung
P_{tot}	max. zulässige Verlustleistung
φ_D	Differentielle Phase
q, Q	Ausgang
Q, Q_B	Güte
R	Widerstand
$R_{th\,JG}$	Wärmewiderstand (Sperrschicht-Gehäuse)
$R_{th\,SG}$	Wärmewiderstand (System-Gehäuse)
$R_{th\,SU}$	Wärmewiderstand (System-Umgebung)
$\frac{S+N}{N}$	Signal-Rauschabstand
SS	Spitze-Spitze

Alphabetische Zusammenstellung der verwendeten Kurzzeichen

T	Periodendauer
T	Temperatur
TK	Temperaturkoeffizient
t	Zeit
T_U	Umgebungstemperatur im Betrieb
T_{stg}	Lagertemperatur
T_j	Sperrschichttemperatur
t_a	Impulsverzögerung
t_H	Haltezeit
t_I	Eingangsimpulsdauer
t_n	Zeitpunkt vor dem Taktimpuls
t_{n+1}	Zeitpunkt nach dem Taktimpuls
t_P	mittlere Signal-Laufzeit
t_{PHL}	Signal-Laufzeit von H nach L
t_{PLH}	Signal-Laufzeit von L nach H
t_{pI}	Eingangsimpulsdauer
t_{pQ}	Ausgangsimpulsdauer
t_{pR}	Rückstellimpulsdauer
t_{pS}	Stellimpulsdauer
t_{pT}	Taktimpulsdauer
t_{pZ}	Zählimpulsdauer
t_s	Setzzeit
t_T	Signal-Übergangszeit
t_t	Totzeit
t_Q	Ausgangsimpulsdauer
t_{THL}	Signal-Übergangszeit (von H nach L)
t_{TLH}	Signal-Übergangszeit (von L nach H)
t_V	Vorbereitungszeit
U, u	Spannung allgemein
U_{Hy}	Hysteresespannung
U_i, U_I	Eingangsspannung
U_q, U_Q	Ausgangsspannung
U_R	Sperrspannung
U_S	Speisespannung
V	Volt
V	Verstärkung
V_D	Differentielle Verstärkung
W	Watt
Z	Impedanz
Z	Zener
ZF	Zwischenfrequenz

1. Type-Designation Code for ICs

IC type designations are based on the European Pro Electron system. The code system is explained in the Pro Electron brochure D 15*), edition 1988.

*) Available from Pro Electron, Avenue Louise, 430 (B.12)
B-1050 Brusells, Belgium

2. Mounting Instructions

Plastic Package

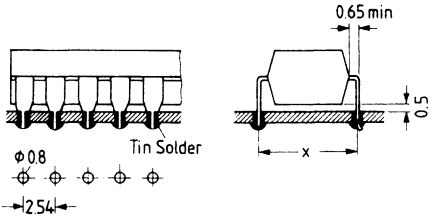
The pins of the cases are bent downwards by an angle of 90° and fit into holes with a diameter of between 0.7 and 0.9 mm spaced 2.54 mm apart. The dimension × is given in the corresponding drawing.

The bottom of the package will not touch the PC board after insertion due to the shoulders on the pins just below the package (**see figure 1**).

After insertion of the package into the PC board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. Plastic packages are soldered on the side of the PCB facing away from the package.

The maximum permissible soldering temperature is 350 °C (max. 3 s) for manual soldering and 260 °C (max. 10 s) for dip soldering and wave soldering.

Figure 1



Power Package with 5, 7, or 9 Pins

Power packages generally have wider pins, the hole diameter on the PCB must be between 1.1 and 1.8 mm. If the pins are bent, there should be no stress between the pins and the package. The minimum distance between the package and the bending point is 2 mm.

Plastic Packages (P-DSO and PL-CC) for Surface Mounting (SMD)

Iron soldering:	soldering temperature 350 °C for max. 3 s; minimum distance between package and soldering point 1.5 mm package temperature max. 150 °C; no mechanical stress on the pins
Vapor phase soldering:	soldering temperature 215 °C, max. soldering time 40 s, 2 x.
Wave soldering:	soldering temperature 260 °C, max. soldering time 8 s. (pins and package are dipped into the tin bath)

Storage, Pretreatment for Processing of ICs in PL-CC Packages

The components are to be stored in a dry place. For soldering methods which may lead to thermal shock stress (e.g. vapor phase soldering) it is recommended to dry the ICs in PL-CC package at 125 °C for a period of 24 hours.

Other Points to Note

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.

When they are being prepared and inserted in a PCB, circuits should be protected against static charging. Under no circumstances may the components be removed or inserted whilst the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensitivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through the switching of inductances on magnetic chutes, etc.

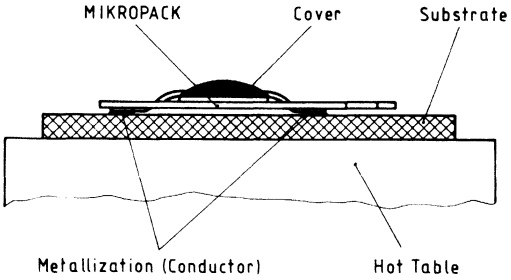
MIKROPACK (SMD)

MIKROPACK components are delivered on film reels.

Mounting Suggestions

a) We recommend vapor phase soldering: soldering temperature 215 °C, soldering time max. 40 s.
b) For prototypes and small quantities (up to approximately 50.0 items/y), the hot table soldering method can also be used (**figure 3**).

Figure 3



Required Equipment and Accessories

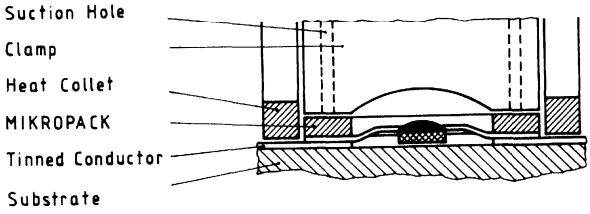
- cutting device
- hot table, temperature regulated (e.g. Weld-Equip, Unitek)
- stereo microscope (e.g. Wild, Zeiss, magnification 6...40 times)
- substrate material: epoxy resin; hard paper; ceramic (thick thin film)

Soldering Data

- soldering temperature: 210 °C max.
- solder coating on substrate: Pb/Sn (e.g. 60/40) wave-tinned or electrodeposited
- soldering time: approx. 10 s
- flux: e.g. colophony, dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

c) For large quantities (e.g. more than 50.0 items/y) thermode soldering is also suitable (**figure 4**).

Figure 4



Required Equipment

- soldering equipment (e.g. Weld-Equip, Farco, Jade)
- substrate material: epoxy resin; hard paper; flexible materials, e.g. polyamide

Soldering Data

- soldering temperature: 220 °C max.
- solder coating on the substrate: Pb/Sn (e.g. 60/40), wave-tinned or electro-deposited
- soldering time: approx. 10 s
- flux: e.g. colophony dissolved in alcohol
- cleaning agents (as required); e.g. Freon TP-35, TE, TF

3. Processing Guidelines for ICs

Integrated circuits (ICs) are **e**lectro**s**tatic-**s**ensitive (ESS) devices. The demand for greater packing density has led to smaller structures on semiconductor chips, with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is virtually impossible for them to be destroyed by purely static electricity. On the other hand, there is acute danger from **e**lectro**s**tatic **d**ischarges (ESD).

Of the multitude of possible sources of discharge, charged devices should be mentioned in addition to charged persons. Low-resistive discharges can produce peak powers amounting to kilowatts.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 220 V if possible.
Means which are effective here are an increase in relative humidity to ≥ 60% and the replacement of highly chargable plastics by antistatic materials.

b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to $10^9\ \Omega$).

To summarise, this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification

The packing of ESS devices is provided with the following label by the manufacturer: 

Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

Handling of Devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to $10^9\ \Omega$/cm.
3. With humidity of > 50% a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 to 100 kΩ.

4. If conductive floors, $R = 5 \times 10^4$ to 10^7 Ω are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to 10^7 Ω).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to 10^8 Ω.
6. When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g. machine parts.

   Example 1) conductive (black) tubes.
   The devices may be destroyed in the tube by charged persons or come out of the tube charged if this is emptied by a charged person.
   Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

   Example 2) anti-static (transparent) tubes.
   The devices cannot be destroyed in the tube by charged persons (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be endangered as in 1) when the tube is emptied if the latter, is no longer sufficiently anti-static after a long period of storage, especially at low humidity (> 1 year).

   In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistive material (≈ 10^6 to 10^8 Ω/cm) between the tube and the machine.

   The use of metal tubes - especially of anodized aluminum - is not advisable because of the danger of low-resistive device discharge.

Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 60 °C.

Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of both high-charging plastic or very low-resistance materials are unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6$ Ω). Sliding contacts and grounding chains will not eliminate charges reliably.

Incoming Inspection

In incoming inspection the above guidelines should be observed. Otherwise any right to refund or replacement if devices fail inspection may be lost.

Material and Mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid contact completely.
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control may not be used. Siemens EMI-suppression capacitors of the type B 81711-B31...-B36 have proven very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

Electrical Tests and Application Circuit

1. The devices should be processed in observance of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting rings.
2. The sockets or integrated circuits must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works'specifications state otherwise. Ensure that the test devices and power supplies do not produce any voltage spikes, either when being turned on or off in normal operation or if the power fuse blows or other fuses respond.
3. When supplying bipolar integrated circuits with current, the negative voltage ($-V_S$ or GND) has to be connected first.. In general, an interruption of this potential during operation is not permissible.
4. Signal voltages may only be applied to the inputs of ICs when or better after the supply voltage is turned on. They must be disconnected when or better before the supply voltage is turned off.
5. Power supplies of integrated circuits are to be blocked as near as possible to the supply terminals of the IC. With bipolar ICs it is recommended to use a low-inductance electrolytic capacitor or at least a paralleled ceramic capacitor of e.g.100 nF to 470 nF .
   Using ICs with high output currents, the necessary value of the electrolytic capacitor must be adapted to the test or application circuit. Transient behavior and dynamic output resistance of the power supplies, line inductances in the supply and load circuit and in particular inductive loads or motors have to be considered. When switching off line inductances or inductive loads, the stored power has to be consumed externally, unless otherwise specified (e.g. by an electrolytic capacitor, diodes, Z diodes or the power supply). Also a switching off of the supply voltage prior to the load rejection should be taken into account.
6. ICs with low-pass character of the output stages (e.g. PNP drivers or PNP/NPN end stages), normally need an additional external compensation at the output. This applies particularly to complex loads. The output of AF power amplifiers is

compensated by the Boucherot element. In individual cases, bridge circuits only need a capacitance for bypassing the load. Depending on the application it is, however, also recommended to connect one capacitor from each output to ground.

7. Observe any notes and instructions in the respective data books.

Packing of Assembled PC Boards or Flatpack Units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/cm < \rho < 10^{10}\ \Omega/cm$.

In most cases – especially with humidity of > 40% – this requirement is fulfilled by simple corrugated board. Better protection is obtained with bags of highly conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

One should always ensure that boards cannot touch.

In special cases it may be necessary to provide protection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminum foil is recommended, although direct contact between the film and the PCB must be avoided. Cardboard boxes with an aluminum-foil lining, such as those used for shipping our devices, are available from Laber of Munich.

Ultrasonic Cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations should be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not attack the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low stress, on the components.

The ultrasonic limits are as follows:

sound frequency	f > 40 kHz
exposure	t < 2 min
alternating sound pressure	p < 29 kPa
sound power	N < 0.5 W/cm²/liter

4. Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

5. Quality Assurance

Quality Assurance System

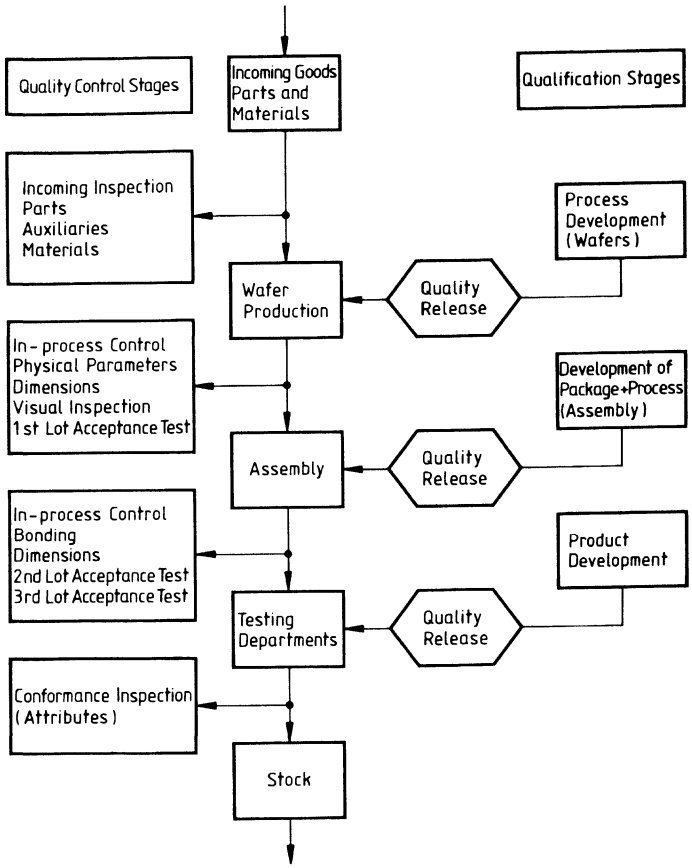
The high quality and reliability of integrated circuits from Siemens is the result of a carefully planned production which is systematically checked and controlled at each production stage.

The procedures are subject to a quality assurance system; full details are given in the brochure 'Siemens Quality Assurance - Integrated Circuits' (SQSIC).

Figure 1 shows the most important stages of the "SQS IC". A quality assurance (QA) department, which is independent of production and development, is responsible for the selected control measures, acceptance procedures, and information feedback loops. This department has state-of-the-art test and measuring equipment at its disposal, works according to approved methods of statistical quality control, and is provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.

The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

Figure 6


Quality Control Stages
Incoming Goods Parts and Materials
Qualification Stages
Incoming Inspection Parts Auxiliaries Materials
Process Development (Wafers)
Wafer Production
Quality Release
In-process Control Physical Parameters Dimensions Visual Inspection 1st Lot Acceptance Test
Development of Package+Process (Assembly)
Assembly
Quality Release
In-process Control Bonding Dimensions 2nd Lot Acceptance Test 3rd Lot Acceptance Test
Product Development
Testing Departments
Quality Release
Conformance Inspection (Attributes)
Stock

Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These tests are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as those of the identical MIL-STD-105 or IEC 410.

The table shows the results of such sampling inspections performed with hundreds of thousands of ICs during 1987. These results correspond to the average outgoing quality (AOQ), and are specified as defectives per million (DPM).

	Inoperatives AOQ (DPM)	Sum of electrical defectives AOQ (DPM)	Sum of mechanical defectives AOQ (DPM)
LSI/VLSI ≥ 1000 gate functions	90	144	250

Reliability

Measures Taken during Development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, specifying e.g. minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these design standards.

In-Process Control during Production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged such that the individual process steps can be reproduced continuously.

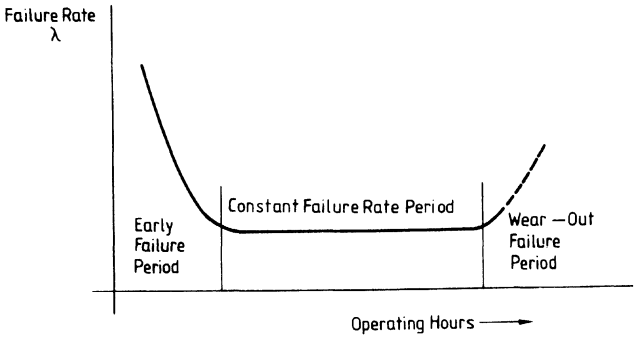
The decreasing failure rates reflect the never ending effort in this direction; in the course of the years they have been reduced considerably despite an immense rise in the ICscomplexity.

So in 1987 the typical random failure rates estimated for accelerated life tests with almost 2 million ICs of all complexities are found to be around 80 fit.

Reliability Monitoring

The general course of the ICs failure rate versus time is shown by a so-called "bathtub" curve (**figure 7**). The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts, during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Figure 7



Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius equation

$$B = \exp\left(\frac{E_A}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for the individual failure mechanisms.

For all Siemens ICs, the reliability data from life tests is converted to an operating temperature of T_A = 50 °C, assuming an average activation energy of 0.5 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behavior. This method considers also failure mechanisms with lower activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line - this is described in the brochure "SQS IC". Such tests are e.g. humidity test at 85 °C and 85% relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summarised reports.

A, B	Indices for limit value
AC	Alternating current
AF	Audio frequency
AM	Amplitude modulation
B	Bandwidth
C	Capacitance
C_i, C_I	Input capacitance
C_{CLK}, C	Clock capacitor
CLK	Clock
DC	Direct current
D	Differential
f	Frequency
Δf	Frequency deviation
FM	Frequency modulation
f_i, f_I	Input frequency
f_q, f_Q	Output frequency
G	Gain
G	giga (10^9)
GND	Ground
Hy	Hysteresis
Hz	Cycles per second (Hertz)
i, I	Input
I, i	Current
I_S	Current consumption
IF	Intermediate frequency
k	kilo (10^3)
K	Kelvin
L	Inductance
m	Milli (10^{-3})
M	Mega (10^6)
m	Modulation factor
MW	Medium wave
N, n	Noise
o	Offset
OSC	Oscillator
P, P_V	Power dissipation
P_{tot}	Max. perm. power dissipation
pp	Peak-to-peak
q, Q	Output
Q, Q_B	Q-factor
R	Resistance
$R_{th\,JC}$	Thermal resistance (junction-case)
$R_{th\,SC}$	Thermal resistance (system-case)
$R_{th\,SA}$	Thermal resistance (system-air)
RF	Radio frequency
$\frac{S+N}{N}$	Signal-to-noise ratio
T	Cycle time

Summary of Terms and Symbols in Alphabetical Order

T	Temperature
TC	Temperature coefficient
t	Time
T_A	Ambient temperature in operation
T_{stg}	Storage temperature
T_j	Junction temperature
t_H	Hold time
t_I	Input pulse duration
t_n	Instant prior to clock pulse
t_{n+1}	Instant after clock pulse
t_P	Average pulse transit time
t_{pd}	Pulse delay time
t_{PHL}	HL pulse transit time
t_{PLH}	LH pulse transit time
t_{pI}	Input pulse duration
t_{pQ}	Output pulse duration
t_{pR}	Reset pulse duration
t_{pS}	Set pulse duration
t_{pCLK}	Clock pulse duration
t_{pZ}	Count pulse duration
t_s	Set-up time
t_T	Signal transition time
t_t	Dead time
t_Q	Output pulse duration
t_{THL}	HL transition time
t_{TLH}	LH transition time
THD	Total harmonic distortion
V	Volt
V, v	Voltage, general
V_{Hy}	Hysteresis voltage
V_i, V_I	Input voltage
V_q, V_Q	Output voltage
V_R	Reverse voltage
V_S	Supply voltage
W	Watt
Z	Impedance
Z	Zener

Technische Daten **Technical Data**

SIEMENS

Mixers

S 042 P

Bipolar IC

Features

- Versatile application
- Wide range of supply voltage
- Few external components
- High conversion transconductance
- Low noise figure

Type	Ordering Code	Package
S 042 P	Q67000-A335	P-DIP-14

Symmetrical mixer for frequencies up to 200 MHz. It can be driven by an external source or by the built-in oscillator. The input signals are suppressed at the outputs. In addition to the usual mixer applications in receivers, converters, and demodulators for AM and FM, the S 042 P can also be used as electronic polarity switch, multiplier etc.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	15	V
Junction temperature	T_j	150	° C
Storage temperature range	T_{stg}	– 40 to 125	° C
Thermal resistance (system-air) .	$R_{th\,SA}$	90	K/W

Operating Range

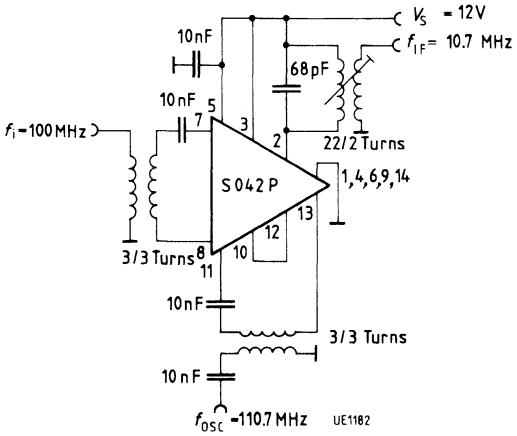
Supply voltage	V_S	4 to 15	V
Ambient temperature	T_A	–15 to 70	° C

Characteristics

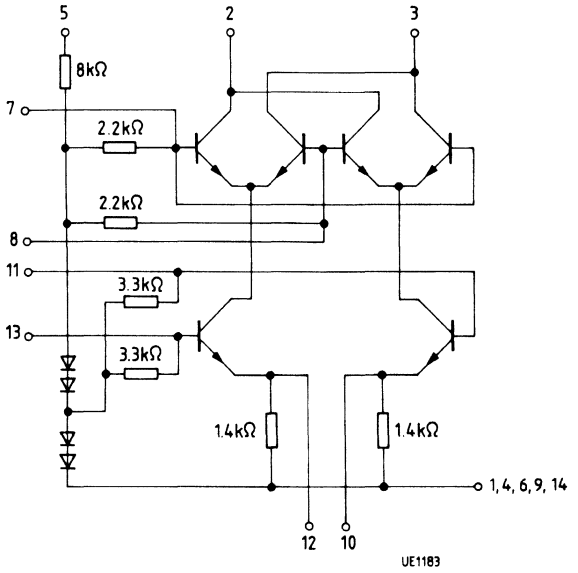
V_S = 12 V, T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption	$I_S = I_2 + I_3 + I_5$	1.4	2.15	2.9	mA
Output current	$I_2 = I_3$	0.36	0.52	0.68	mA
Output current difference	$I_3 - I_2$	–60		60	µA
Supply current	I_5	0.7	1.1	1.6	mA
Power gain f_i = 100 MHz, f_{OSC} = 110.7 MHz	G_P	14	16.5		dB
Breakdown voltage $I_{2,3}$ = 10 mA; $V_{7,8}$ = 0 V	V_2, V_3	25			V
Output capacitance	$C_{2\text{-M}}$, $C_{3\text{-M}}$		6		pF
Conversion transconductance f = 455 kHz	$S = \frac{I_2}{V_7 - V_8} = \frac{I_3}{V_7 - V_8}$		5		mS
Noise figure	NF		7		dB

Test Circuit



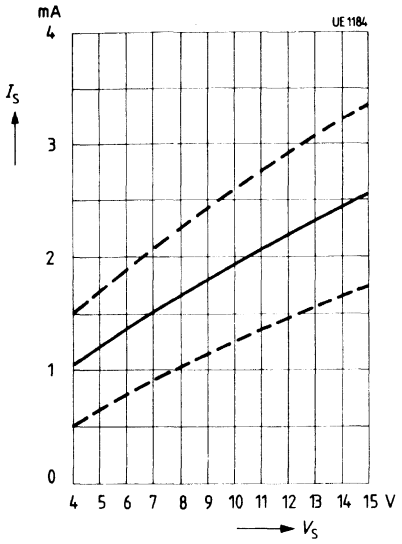
Circuit Diagram



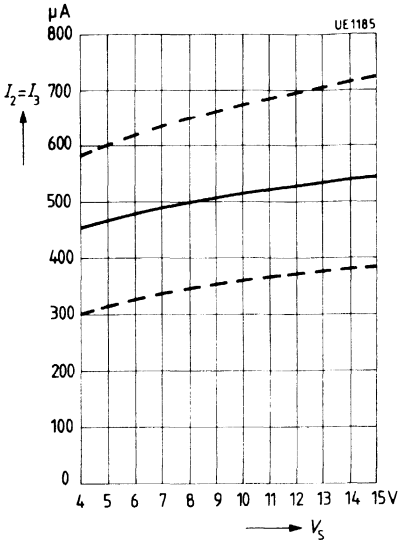
A galvanic connection between pins 7 and 8 and pins 11 and 13 through coupling windings is recommended.

A resistor of at least 220 Ω may be connected between pins 10 and 14 (ground) and between pins 12 and 14 to increase the currents and thus the conversion transconductance. Pins 10 and 12 may be connected through any impedance. In case of a direct connection between pins 10 and 12, the resistance from this pin to 14 may be at least 100 Ω. Depending on the layout, a capacitor (10 to 50 pF) may be required between pins 7 and 8 to prevent oscillations in the VHF band.

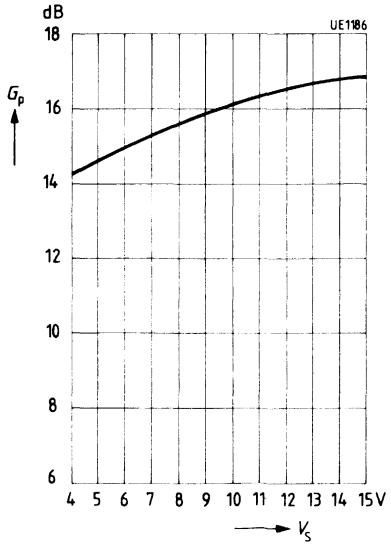
Total current consumption versus supply voltage



Output current versus supply voltage

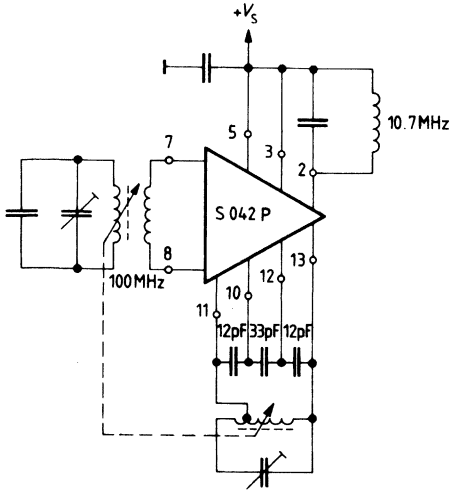


Power gain versus supply voltage

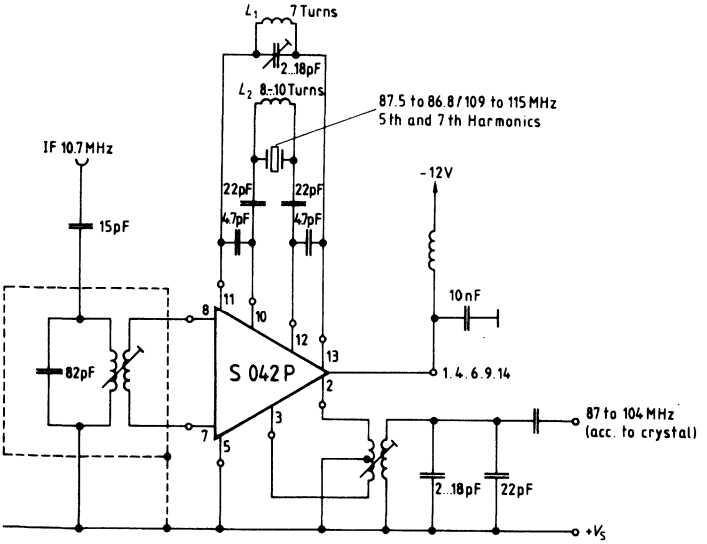


Application Circuits

FM Mixer with inductive tuning

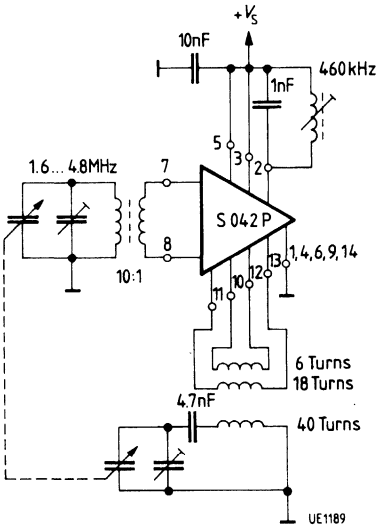


FM Mixer with crystal oscillator

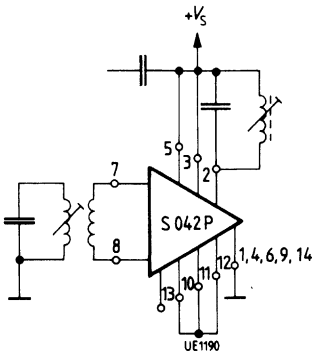


For harmonic crystals an adequate inductance is recommended between pins 10 and 12 to avoid oscillations to the fundamental.

Mixer for Short-Wave Application
in self-oscillating operation



Differential Amplifier with internal neutralization, also suited for use as limiter for frequencies up to 50 MHz or at higher currents up to 100 MHz



SIEMENS

RDS-ARI-DECODER — SDA 1000

Preliminary Data — **Bipolar IC**

Decoder unit for radio receivers (especially car radios), used to interpret RDS

Features

- RDS information is decoded (RDS Clock, RDS Data)
- Low decoding threshold
- High decoding reliability
- Open collector outputs
- Simultaneous RDS and ARI interpretation
- SK/DK decoding of ARI signals

Type	Ordering Code	Package
SDA 1000	Q67000-A8255	P-DIP-20

Circuit Description

The differentially coded PSK modulated (DPSK) RDS carrier is demodulated in a modified Costas loop. The interpreting circuit consists of a biphase symbol decoder, clock recovery and a differential decoder. The (non error adjusted) data and the clock signal are each available in serial at a TTL output.
Additionally, should ARI be present, a DK[1])/BK[2]) complete signal is available at one output, SK[3]) at a second and DK[1]) at a third, to be used as a switching signal.
The RDS DATA, CLOCK, SK[3]) and DK[1]) outputs are npn open collector outputs.

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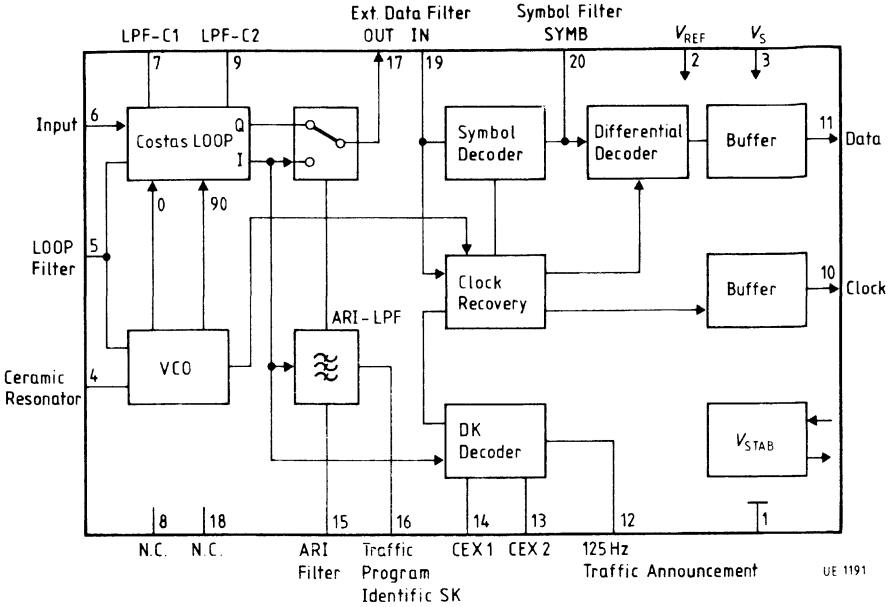
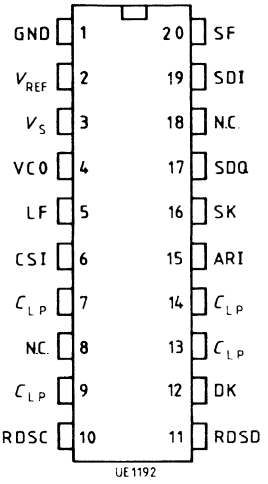
[1]) Traffic announcement identification
[2]) Area identification
[3]) Traffic program identification

Block Diagram



Pin Configuration

(top view)



Pin Definitions and Functions

Pin No.	Symbol	Description	Function
1	GND	Ground	This pin is for decoupling.
2	V_{REF}	Reference voltage	This pin has to be blocked against ground (pin 1).
3	V_S	Supply voltage	This pin has to be blocked against ground (pin 1).
4	VCO	VCO	Ceramic resonator f_o = 456 kHz against ground
5	LF	Loop filter	Ext. filter connection (RC network see application description)
6	CSI	Composite signal input	Asymmetrical input for RDS-ARI composite signal
7	C_{LP}	Low pass capacitor	The external capacitor determines the cutoff frequency. $f_{3db} \sim \frac{1}{2\pi \times 55 \times 10^3 \times C}$
8	N.C.		N.C.
9	C_{LP}	Low pass capacitors	The external capacitor determines the cutoff frequency. $f_{3db} \sim \frac{1}{2\pi \times 55 \times 10^3 \times C}$
10	RDSC	RDS Clock	1.1875 kHz output with open collector
11	RDSD	RDS Data	RDS data output with TTL level open collector
12	DK	DK	Open collector output: connected if 125-Hz DK signal (ARI) is present.
13/14	C_{LP}	Low pass capacitors	Ext. capacitors determine the interpretation bandwidth of the 125-Hz signal.
15	ARI	ARI low pass filter	Integration capacitor
16	SK	SK	Open collector output: connected if ARI is present
17	SDQ	Symbol decoder output	For additional filtering of data, an additional external filter can be connected between pin 17 and pin 19.
18	N.C.		N.C.
19	SDI	Symbol decoder input	For additional filtering of data, an additional external filter can be connected between pin 17 and pin 19.
20	SF	Symbol filter	Ext. capacitor for integration.

Absolute Maximum Ratings
$T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	– 0.3	8	V

Operating Range

Supply voltage	V_S	4.5	5.5	V
Ambient temperature	T_A	– 40	85	°C

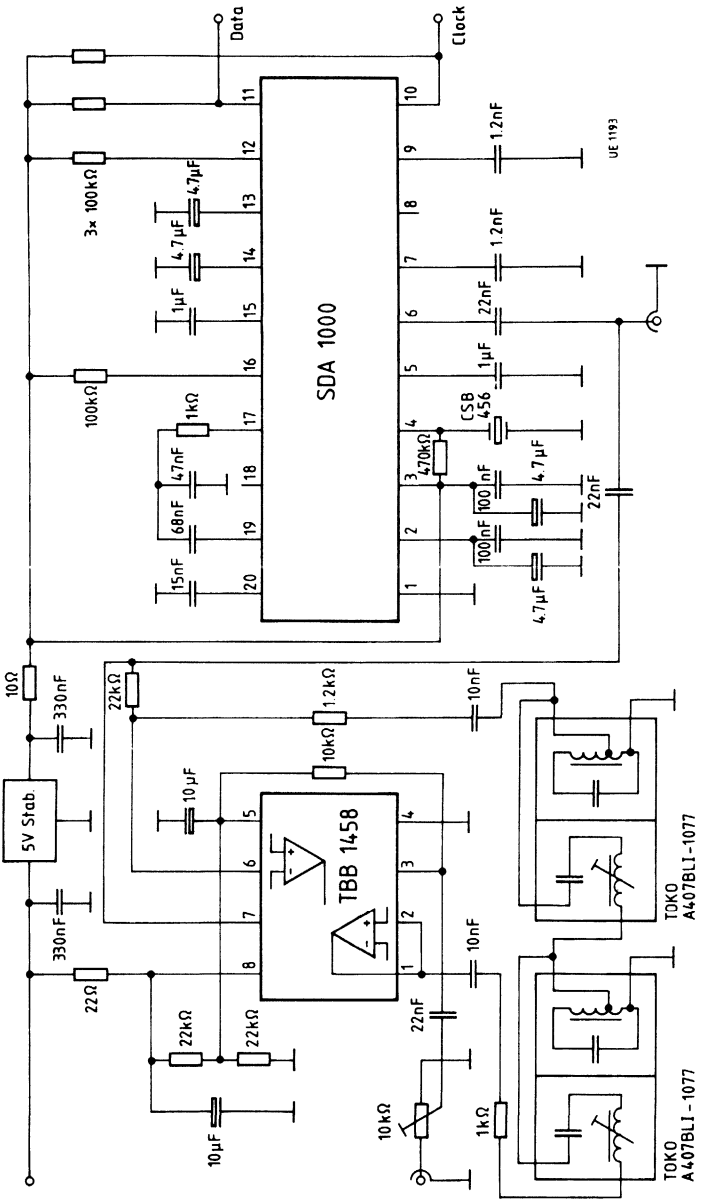
Characteristics
$V_S = 5$ V; $T_A = 25$ °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption	I_3	12	15	20	mA
Decoder input voltage range	V_{61}	15	25	40	mV
Decoding threshold RDS/ARI			6		dB
Hold time (with ARI)			10		ms
Hold time (without ARI)			5		ms
Handling time ARI-DK			100		ms
Handling time ARI-SK			10		ms
Collector current for output transistors	I_Q		50		µA
Log "1" level $R = 100$ kΩ	V_Q	2.4			V
Log "0" level $R = 100$ kΩ	V_Q			0.7	V
VCO frequency	f	450	456	460	kHz
Reference voltage	V_{REF}	2.2	2.5	2.8	V

DC Characteristics
$T_A = 25\,°C$

Parameter		Symbol	Limit Values			Unit
			min.	typ.	max.	
Reference voltage	(pin 2)	V_3	2.2	2.5	2.8	V
Oscillator	(pin 4)			3.4		V
Loopfilter	(pin 5)			2.6		V
MPX input	(pin 6)			2.6		V
AM filter	(pin 7)			2.6		V
AM filter	(pin 9)			2.6		V
Clock High	(pin 10)		2.4		5	V
Clock Low			0		0.7	V
DATA High	(pin 11)		2.4		5	V
DATA Low			0		0.7	V
DK High	(pin 12)		2.4		5	V
DK Low			0		0.7	V
DK filter	(pin 13)			2.5		V
DK filter	(pin 14)			2.5		V
ARI low pass filter	(pin 15)			2.5		V
SK High	(pin 16)		2.4		5	V
SK Low			0		0.7	V
OUT	(pin 17)			2.5		V
IN	(pin 19)			2.5		V
Integrator	(pin 20)			2.5		V

Application Circuit



8-Bit Single-Chip Microcontrollers

Survey of Microcomputers for Home-Entertainment Electronics

Device	ROM	RAM	D/As	Piggyback	Application/ Remarks
SDA 2043 SDA 2063 SDA 2083	4 Kbytes 6 Kbytes 8 Kbytes	128 Bytes 128 Bytes 128 Bytes	max. 4 max. 4 max. 4	PIG 3083 PIG 3083 PIG 3083	Cheap to upper middle-class TV
SDA 2087	External 64 Kbytes	256 Bytes	Subset of SAB 80535, eight A/D inputs, resolution 8 bits, w/o programmable references, main use in VTR		
SDA 20160	16 Kbytes	256 Bytes	max. 8	PIG 30160	Top - class TV, middle-class VTR
SDA 20560	16 Kbytes	256 Bytes	max. 8		TV with DOS
SDA 30161	External 64 Kbytes	768 Bytes	max. 8		For programs >16 Kbytes
OLP 30161	EPROM 64 Kbytes	768 Bytes	max. 8		Hybrid solution > 16 Kbytes

Emulators and Piggybacks

There are suitable emulators and piggybacks available for the above devices for generating software or creating prototypes. Enquire for further details.

SIEMENS

8-Bit Single-Chip Microcontrollers

SDA 2043
SDA 2063
SDA 2083

Preliminary Data

MOS IC

Features

- 8051 CPU
- Cycle time 1 µs at 12 MHz
- Supply voltage 5 V
- 4/6/8-Kbyte ROM
- 128-byte RAM
- Integrated I^2C bus interface
- 34 bidirectional I/O lines
- Input for directly processing IR signals
- Proven NMOS technology
- P-DIP-40 package
- Special devices like piggyback PIG 30... available for program development

The three devices SDA 2043/2063/2083 are pin and functionally compatible and differ solely in the size of their program memory. This permits custom adaptation to system requirements. The microcomputer "grows along" with the application. Applications with greater program memory can be handled by other ICs **(see table).**

There is a suitable emulator and piggyback available for these devices for generating software or creating prototypes. Enquire for further details.

Type	Ordering Code	Package
SDA 2043 (A XXX)	Q67120-C449	P-DIP-40 (4 Kbytes)
SDA 2063 (A XXX)	Q67120-C450	P-DIP-40 (6 Kbytes)
SDA 2083 (A XXX)	Q67120-C451	P-DIP-40 (8 Kbytes)

Note

The above devices can only be supplied with an application-specific program (ROM). The designation for this program is A XXX. Orders for devices without this program designation cannot be accepted.

SIEMENS

8-Bit Single-Chip Microcontroller — SDA 2087

Preliminary Data — **MOS IC**

Features

- Full software compatibility with SAB 8051
- Program memory: 64-Kbyte ROM added on (external)
- Data memory: internal 256-byte RAM or 64-Kbyte RAM added on (simultaneous use of internal and external RAM)
- Six 8-bit ports
- 56 input/output lines
- Twelve interrupt sources (five internal, seven external)
- Integrated, programmable watchdog timer for enhanced reliability
- Eight analog inputs
- Highly precise 8-bit A/D converter, total conversion time 20 µs for 12-MHz system timing
- Power-down mode with data retention of 40 bytes of internal RAM at typically 1 mA supply current
- Temperature range 0 to 70 °C

This application-specific, single-chip microcomputer is a follow-on development of SDA 2043/2063/2083, ie all characteristics of the latter devices are integrated as a subset.

SDA 2087 has no internal program memory.

Functionally it is very similar to SAB 8035. In SDA 2087 the programmable references are not available for A/D conversion.

Type	Ordering Code	Package
SDA 2087	Q67120-C262	PL-CC-68

Enquire for a data sheet and further details.

SIEMENS

8-Bit Single-Chip Microcontroller — SDA 20160

Preliminary Data — **MOS IC**

Features

- 8051 CPU
- Cycle time 1 µs at 12 MHz
- Supply voltage 5 V
- Exceptional noise immunity through special pin configuration, in particular against interference by way of supply voltage
- 16-Kbyte ROM on chip
- 256-byte RAM
- Integrated I^2C bus interface
- 34 bidirectional I/O lines
- Input for directly processing IR signals
- Proven NMOS technology
- P-DIP-40 package
- Pinning identical to SDA 2043/2063/2083
- Special devices like piggyback PIG 30... available for program development

Compared to SDA 2083, SDA 20160 offers greater ROM and RAM capacity with the same pinning. This makes it possible to implement more demanding applications. The electrical characteristics and instruction set are virtually identical.

Type	Ordering Code	Package
SDA 20160	Q67120-C440	P-DIP-40

Enquire for a data sheet and further details.

8-Bit Single-Chip Microcontroller

SDA 20560

Preliminary Data

MOS IC

Features

- Integrated DOS (Display On Screen): 96 characters, matrix of 12 × 16 dots; color display of characters and background
- 16-Kbyte ROM
- 256-byte RAM
- Compatible with SDA 20160 in major points
- 8051 CPU
- Cycle time 1 µs at 12 MHz
- Supply voltage 5 V
- Integrated I^2C bus interface
- 34 bidirectional I/O lines
- Input for directly processing IR signals
- Proven NMOS technology
- P-DIP-40 package
- Pinning virtually identical to SDA 20160
- Special devices like piggyback PIG 30... available for program development

Compared to SDA 20160, SDA 20560 offers the possibility of implementing on-screen insertion. The individual insertion software (approx. 4 Kbytes) is a constituent part of the 16-Kbyte ROM. This means that an extra, dedicated insertion device can be omitted, thus making the overall system more attractive in price.

Type	Ordering Code	Package
SDA 20560	Q67120-C600	P-DIP-40

Enquire for a data sheet and further details.

SIEMENS

8-Bit Single-Chip Microcontroller

SDA 30161
OLP 30161

Preliminary Data

MOS IC

Features

- Most powerful µC in the family
- External ROM up to 64 Kbytes
- 768-byte RAM
- Compatible with SDA 20160 in major points
- 8051 CPU
- Cycle time 1 µs at 12 MHz
- Supply voltage 5 V
- Integrated I^2C bus interface
- 34 bidirectional I/O lines
- Input for directly processing IR signals
- Proven NMOS technology
- PL-CC-68 package

SDA 30161 is the most powerful device of the µC family. It can be used to implement highly demanding applications that are only possible with very large program memory and large RAM capacity. In this performance category a ROM variant was intentionally omitted.

Type	Ordering Code	Package
SDA 30161	Q67120-C463	PL-CC-68
OLP 30161	Q67120-C603	P-DIP-40

Enquire for a data sheet and further details.

PLL with I²C Bus for AM/FM Receivers

SDA 2121-2

Preliminary Data

CMOS IC

Features

- High input sensitivity (50 mV_{rms} on FM and 30 mV_{rms} on AM)
- High input frequencies (150 MHz on FM and 25 MHz on AM)
- Extremely fast phase detector with very short anti-backlash pulses
- I²C bus
- Large divider rations:
  - 16 Bit N divider
  - 16 Bit R divider
  - Divider factor without vacancy

OSC IN	2-65535
AM IN	2-65535
FM IN /2	2-65535

- Adjustable raster width (< 1 kHz for AM, < 12.5 kHz for FM)*
- Two-pin oscillator provides connection of a piezoelectric crystal for reference frequency generation
- Switchable phase detector polarity
- Switchable phase detector current
- One phase detector output each for FM and AM with the corresponding analog phase detector outputs
- Open drain switching outputs for 10 V

Type	Ordering Code	Package
SDA 2121-2	Q67100-H5025	P-DIP-20
SDA 2121-2X	Q67100-H5026	P-DSO-20

Raster width = Input frequency / divider factor
[On FMIN input frequency / 2 is to be used due to the prescaler]

The SDA 2121-2 is an integrated circuit in CMOS technology which has been especially designed for application in radio equipment.

The SDA 2121-2 is a complex PLL component in CMOS technology for processor controlled frequency synthesis.

Function and dividing ratios are selected via an I^2C bus interface (licensed by Philips) at pins SCL, SDA and A0. The chip address is set via address input A0. Thus it is possible to address two components via the I^2C bus. The reference frequency can be applied at input OSC IN or it can be generated internally by a piezoelectric crystal. Its maximum value is 15 MHz. The VCO frequency is applied at input FM or AM respectively. Its maximum value is 150 MHz at the FM input and 25 MHz at the AM input. The FM input signal is divided by two by an asynchronous prescaler.

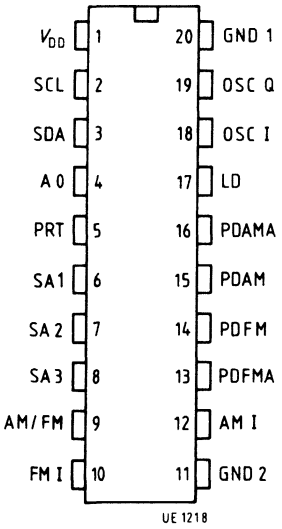
Outputs PDFM and PDAM supply the phase detector signal with especially short anti-backlash pulses to neutralize even the smallest phase deviations. Polarity and current of the PD outputs can be switched. The component also has corresponding analog phase detector outputs and lock-detect output (LD).

Additional outputs are the open-drain switching outputs (SA 1, 2, 3, AM/FM) with a dielectric strength of 10 V and a port output (PRT).

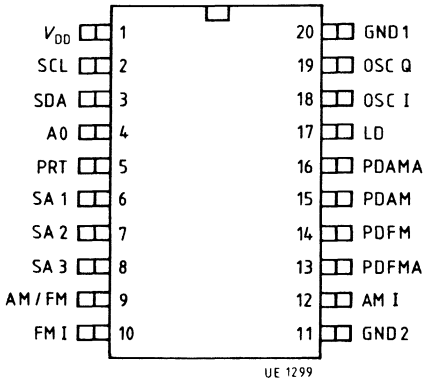
Pin Configuration

(top view)

P-DIP-20



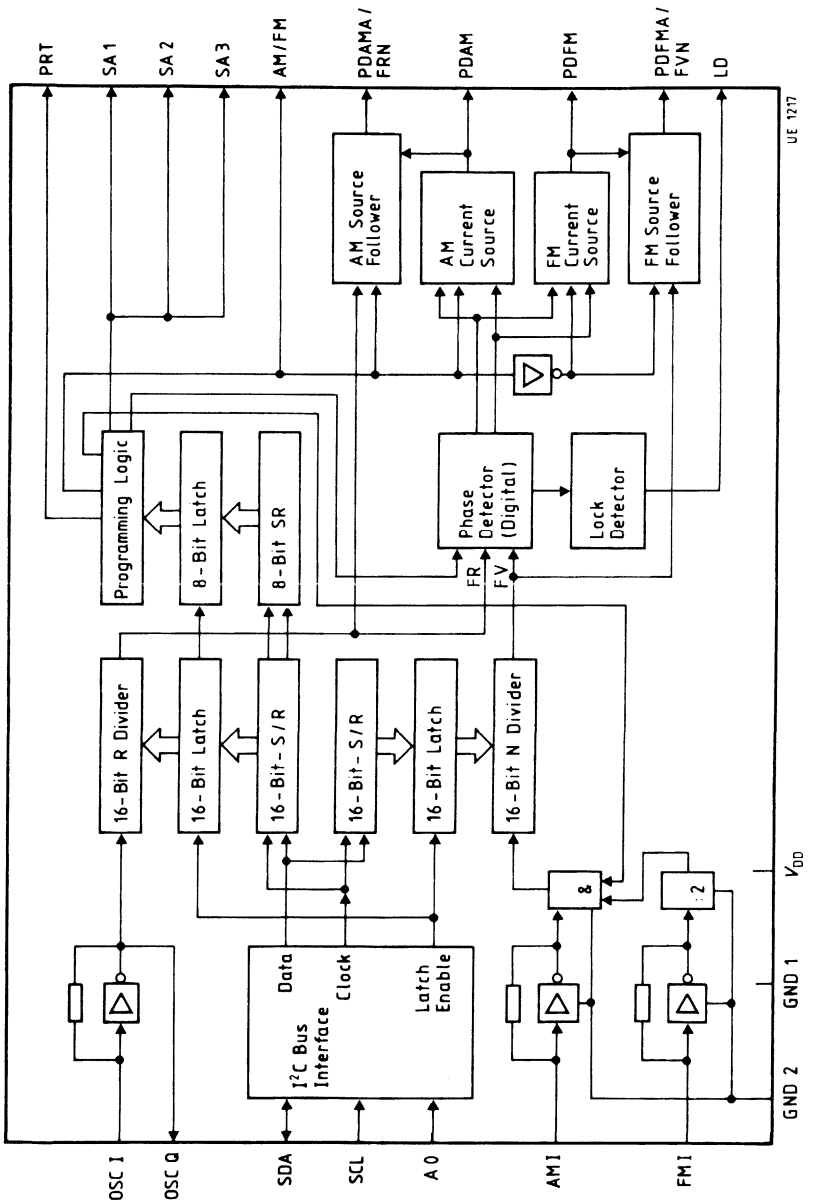
P-DSO-20



Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{DD}	Supply voltage
2	SCL	I^2C bus clock
3	SDA	I^2C bus data input and acknowledge output
4	A0	Address input
5	PRT	Port output
6	SA 1	Switch output (open drain output for 10 V)
7	SA 2	Switch output (open drain output for 10 V)
8	SA 3	Switch output (open drain output for 10 V)
9	AM/FM	Switch output (open drain output, 10 V) switching AM/FM operation
10	FMI	FM input
11	GND2	Ground connection for AM and FM input amplifier
12	AMI	AM input
13	PDFMA	Analog output corresponding to the phase detector output, in test operation open drain output of FRN and FVN signal
14	PDFM	Phase detector output for AM or FM active or tristate depending on operating mode
15	PDAM	Phase detector output for AM or FM active or tristate depending on operating mode
16	PDAMA	Analog output corresponding to the phase detector output, in test operation open drain output of FRN and FVN signal
17	LD	Lock-detect output
18	OSCI	Connection for reference oscillator input and output
19	OSCQ	Connection for reference oscillator input and output
20	GND1	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD}	– 0.3		6	V
Input voltage	V_I	– 0.3		V_{DD} + 0.3	V
Power dissipation per output	P_Q			10	mW
Total power dissipation	P_{tot}			300	mW
Storage temperature	T_{stg}	– 40		125	°C
Output voltage switch outputs	V_{QH}			10.5	V

Operating Range

Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current	I_{DD}		6	10	mA
Ambient temperature	T_A	–25		85	°C
Output voltage switch outputs	V_{QH}			10	V

Test conditions for supply voltage

- V_{DD} = 5.5 V
- T_A = 25°C outputs not connected
- No test operation
- Max. permissible operating frequency on AM, FM, OSC IN = 15 MHz
- V_{IFM}, V_{IAM}, V_{IOSCIN} = 100 mVrms
- Minimal divider ratios
- PLL in in-lock condition

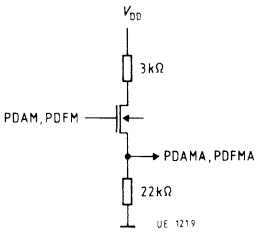
Characteristics

T_A = 25 °C; all voltages referenced to GND

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Signals SCL, SDA, A0						
H-input voltage	V_{IH}	0.7×V_{DD}		V_{DD}	V	
L-input voltage	V_{IL}	0		1.5	V	
Input capacitance	C_I			10	pF	
Input current	I_I			10	µA	$V_I = V_{DD}$
Input Signal OSC IN						
Input frequency	f			15	MHz	V_{DD} = 4.5 V
Input voltage	V_I	100			mVrms	(sine wave)
Input capacitance	C_I			10	pF	
Input current	I_I			30	µA	$V_I = V_{DD}$
Input Signal AM						
Input frequency	f	0.5		25	MHz	V_{DD} = 4.5 V
Input voltage	V_I	30			mVrms	(sine wave)
Input capacitance				10	pF	
Input current	I_I			30	µA	$V_I = V_{DD}$
Input Signal FM						
Input frequency	f	10		150	MHz	V_{DD} = 4.5 V
Input voltage	V_I	50			mVrms	(sine wave)
Input capacitance	C_I			10	pF	
Input current	I_I			30	µA	$V_I = V_{DD}$

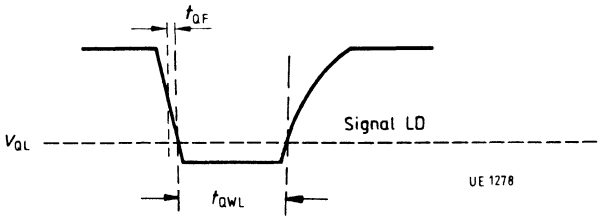
Characteristics (cont'd)
T_A = 25 °C; all voltages referenced to GND

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output signal PDFM (tristate output)						
PD current value A	I_Q	340	± 570	800	µA	V_{DD} = 5 V
PD current value B	I_Q	85	± 145	205	µA	T_A = -25°C . . . 60°C
PD leakage current	I_Q		± 50	500	nA	
Output Signal PDAM (tristate output)						
PD current value A	I_Q	70	± 115	160	µA	V_{DD} = 5 V
PD current value B	I_Q	15	± 30	45	µA	T_A = -25°C . . . 60°C
PD leakage current	I_Q		± 50	500	nA	no load at the output
Output Signal PDAMA, PDFMA (analog output)						
H-output current	I_{QH}		1	2.5	mA	V_{PD} = V_{DD} = 5 V
L-output current	I_{QL}	0.1	0.5		mA	V_{PD} = GND



Characteristics (cont'd)
T_A = 25 °C; all voltages referenced to GND

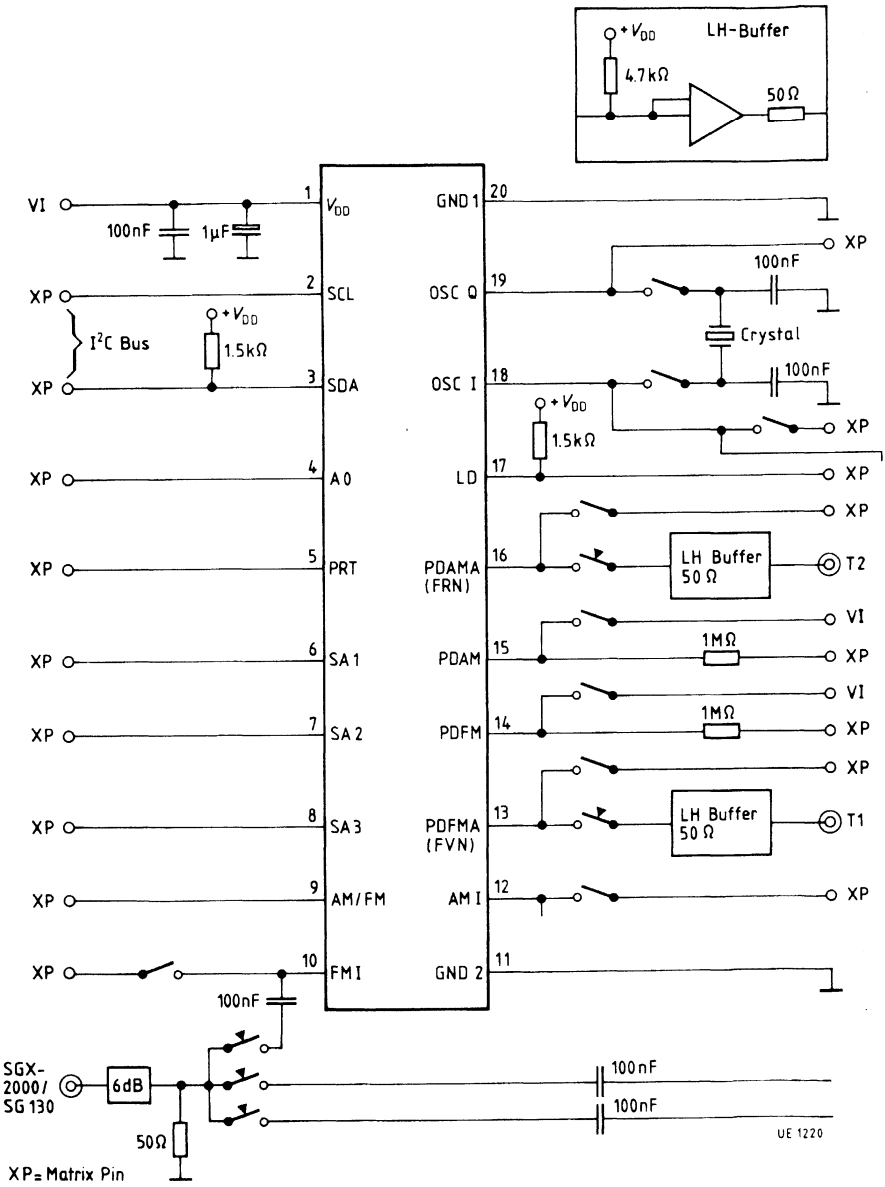
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Signal LD (open drain output)						
L-output signal	V_{QL}			0.4	V	I_{QL} = 3 mA V_{DD} = 5 V C_L = 20pF
L-output pulse width	t_{QWL}		30		ns	



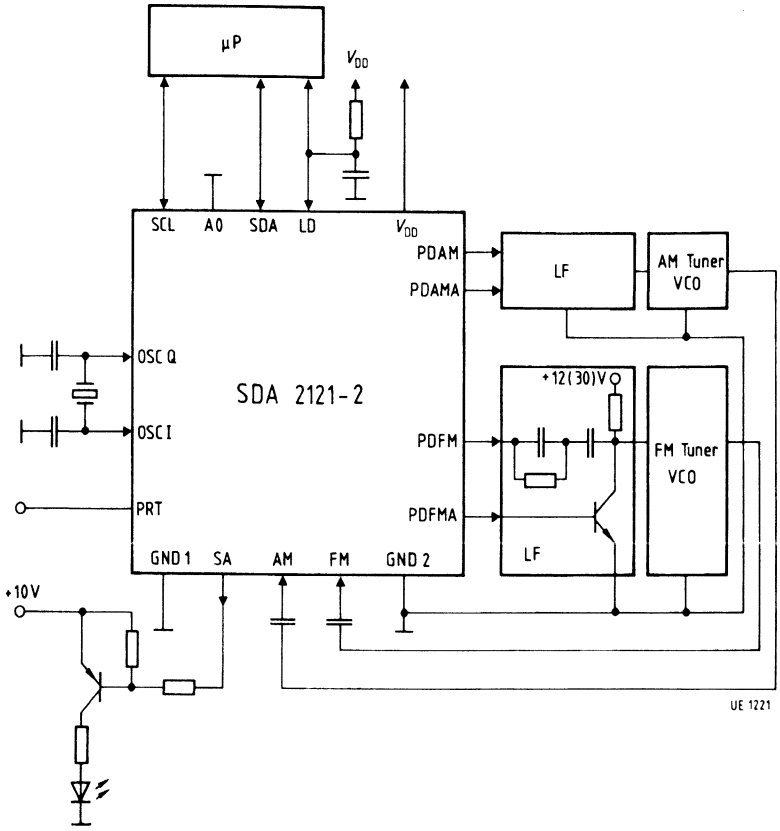
Output Signal PRT

H-output voltage	V_{QH}	V_{DD} – 0.4			V	I_{QH} = 1 mA
L-output voltage	V_{QL}			0.4	V	I_{QL} = 1 mA
	V_{QL}			0.1	V	I_{QL} = 0.1 mA
OutputSsignal SA 1, 2, 3 and FM (open drain switching outputs)						
L-output voltage	V_{QL}			0.4	V	I_{QL} = 1 mA V_{DD} = 5 V
	V_{QL}			0.1	V	I_{QL} = 0.1 mA
Output Signal SDA						
L-output voltage	V_{QL}			0.4	V	I_{QL} = 3 mA V_{DD} = 5 V C_L = 400 pF

Test Circuit



Application Circuit



Diagram

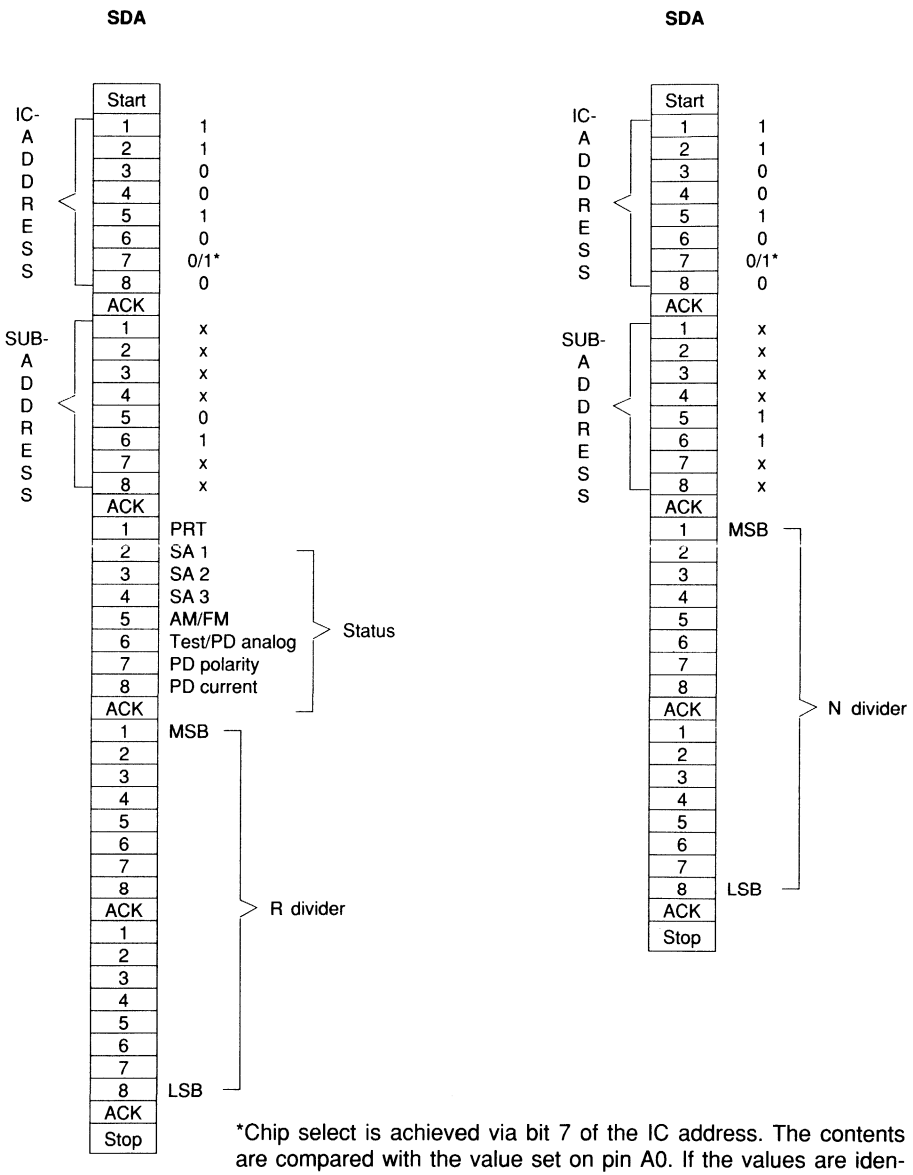
Status Programming Table

		Status Bit	
Bit		**0**	**1**
1	PRT	L	H
2	SA 1	L	H
3	SA 2	L	H
4	SA 3	L	H
5	AM/FM	L (FM operation)	H (AM operation)*
6	PD analog/test	PD analog	test**
7	PD polarity	neg.	pos.
8	PD current	value B	value A (AM or FM operation)

*When the switch output FM is switched from "H" to "L" via bit 5 (FM), operation is switched from AM to FM
PDAM is in tristate and vice versa

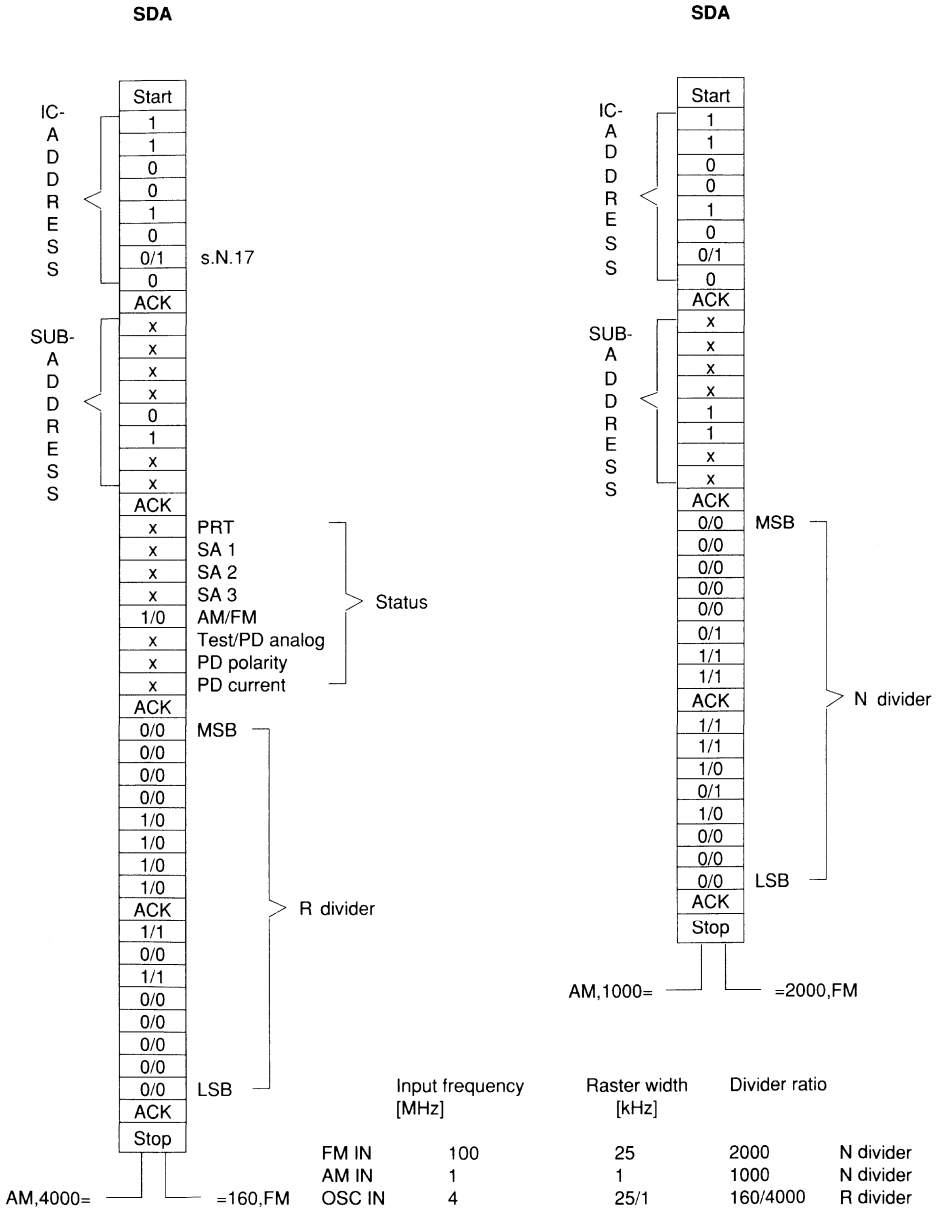
**In test operation PDFMA and PDAMA outputs are switched as FVN and FRN outputs respectively

I²C Bus Transfer Protocol



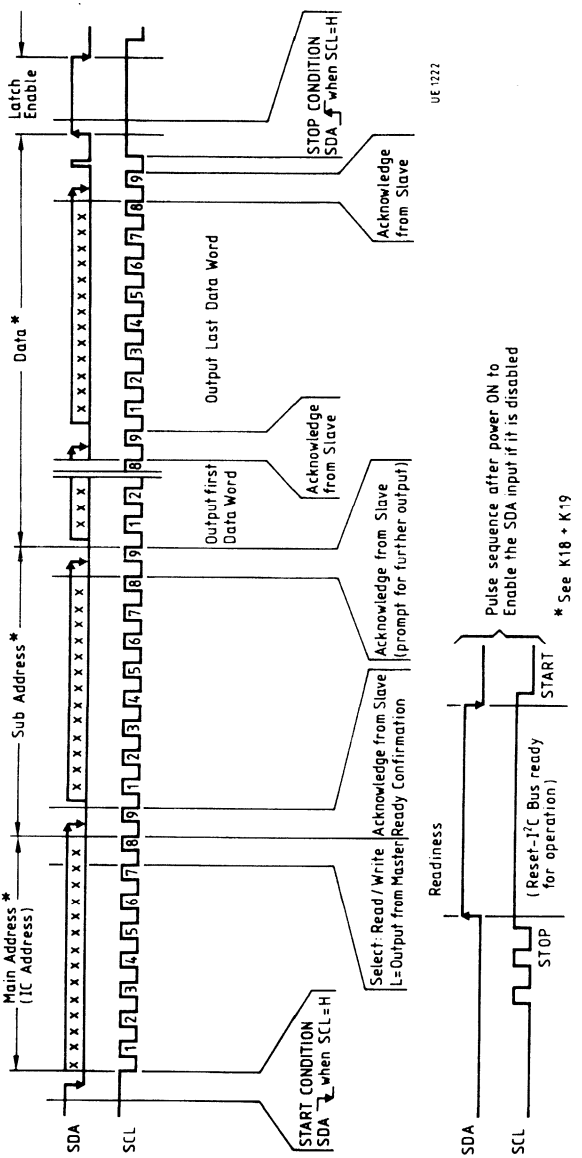
*Chip select is achieved via bit 7 of the IC address. The contents are compared with the value set on pin A0. If the values are identical, the respective chip is selected.

Programming Example

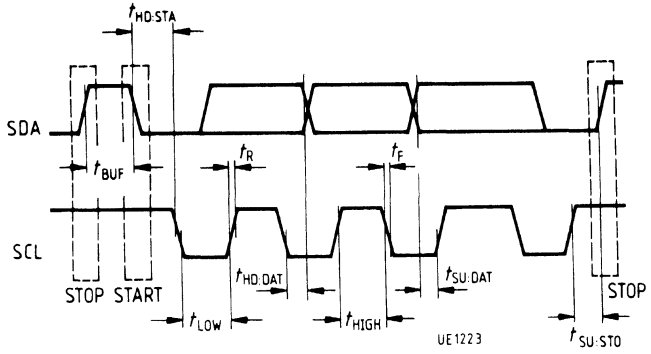


	Input frequency [MHz]	Raster width [kHz]	Divider ratio	
FM IN	100	25	2000	N divider
AM IN	1	1	1000	N divider
OSC IN	4	25/1	160/4000	R divider

Transfer Protocol for I²C Bus



I²C Bus Timing, PRT, SA, AM/FM

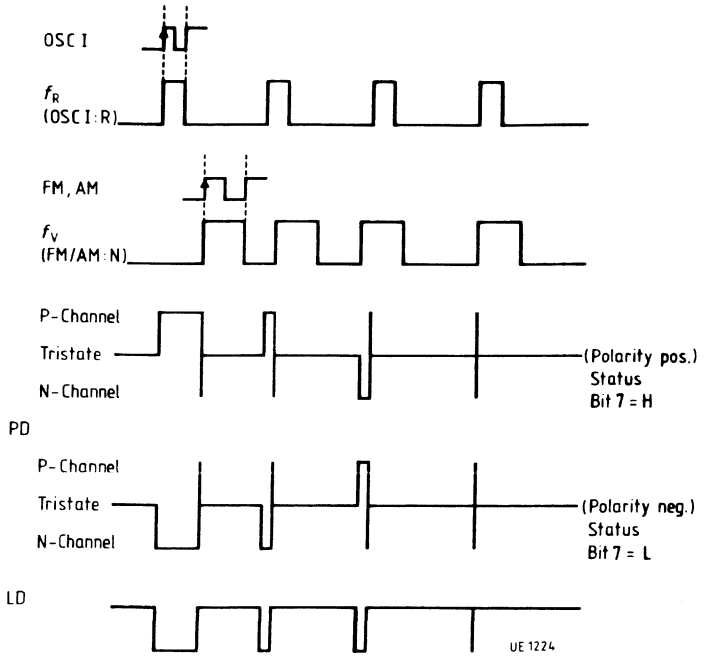


Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	f_{SCL}	0	100	kHz
Hold time data to SCL$_{LOW}$	$t_{HD:DAT}$	0		µs
Inactive time prior to next transfer	t_{BUF}	4.7		µs
Hold time during start condition (first CLOCK pulse is generated after this time period)	$t_{HD:STA}$	4.0		µs
LOW clock phase	t_{LOW}	4.7		µs
HIGH clock phase	t_{HIGH}	4.0		µs
Set-up time for DATA	$t_{SU:DAT}$	250		ns
Rise time for SDA and SCL signal	t_R		1	µs
Fall time for SDA and SCL signal	t_F		300	ns
Set-up time for SCL clock during STOP condition	$t_{SU:STO}$	4.7		µs
PRT delay time relative to STOP condition	t_D		500	µs

All values are referenced to specified input levels V_{IH} and V_{IL}.

Pulse Diagram

Phase Detector/Lock Detector



SIEMENS

Static LED Display Driver with Blanking Capability

SDA 2131-2

Bipolar IC

Features

- Integrated load resistances, thus few external components are required
- Number of LEDs software-selectable
- Blanking capability through DC-controlled input
- Simple connection to a microcomputer

Type	Ordering Code	Package
SDA 2131-2	Q67000-A2044	P-DIP-22

The SDA 2131-2 includes a static display driver for 16 LEDs, each featuring 10 mA output current. The serial data interface enables a simple connection to the microcomputer.

Circuit Description

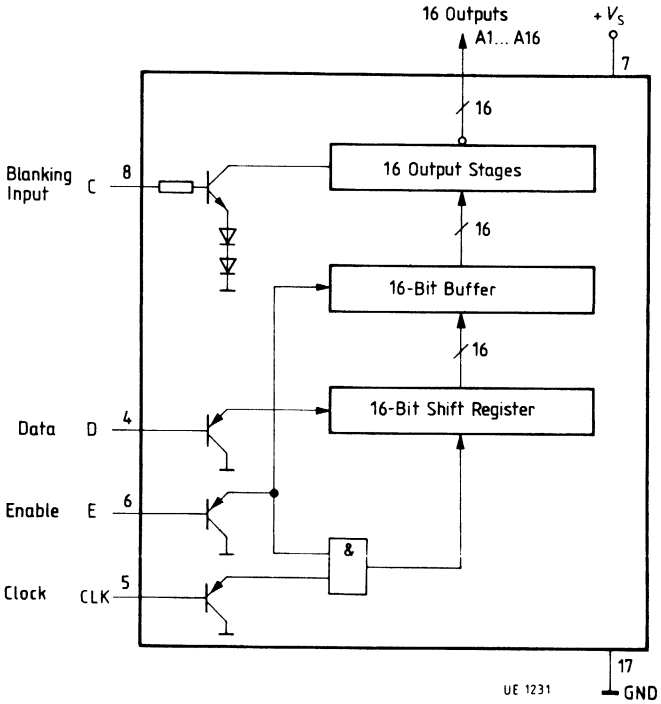
A serial interface consisting of data input D, enable input E, and clock input CLK, connects the IC to a microprocessor. The 16-bit information ("H" at input D corresponds to the current flow at outputs A1 to A16) is loaded into a 16-bit shift register via the serial data input, beginning with LSB. Data transfer is initiated by the HL slope of the clock pulse at CLK. The data transfer D can take place only during the H state of the enable input E. A buffer accepts the data from the shift register during the HL slope of the enable input. The buffer directly drives the outputs A1 to A16.

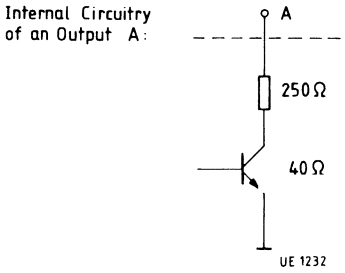
The output is limited by an internal resistor of 290 Ω.

Through input C the outputs can be switched off (V_{C8} = 0 V).

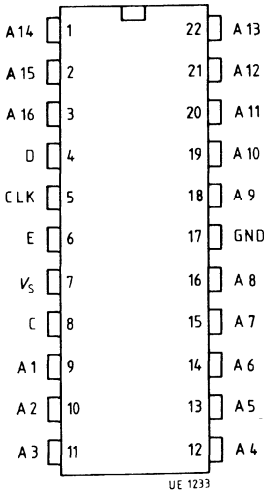
The inputs D, E, and CLK, and the input C are TTL-compatible.

Block Diagram





Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	A14	Output 14 for LED cathode
2	A15	Output 15 for LED cathode
3	A16	Output 16 for LED cathode
4	D	Input for data
5	CLK	Input for clock
6	E	Input for enable
7	V_S	Supply voltage
8	C	Input for blanking
9	A1	Output 1 for LED cathode
10	A2	Output 2 for LED cathode
11	A3	Output 3 for LED cathode
12	A4	Output 4 for LED cathode
13	A5	Output 5 for LED cathode
14	A6	Output 6 for LED cathode
15	A7	Output 7 for LED cathode
16	A8	Output 8 for LED cathode
17	GND	Ground
18	A9	Output 9 for LED cathode
19	A10	Output 10 for LED cathode
20	A11	Output 11 for LED cathode
21	A12	Output 12 for LED cathode
22	A13	Output 13 for LED cathode

Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage range	V_{S7}	– 0.3 to 7	V
Input voltage range	$V_{i4,5,6}$	– 0.3 to 7	V
Output voltage range (outputs blocked) (pins 1 to 3, 9 to 16, 18 to 22)	V_{qH}	– 0.3 to 7	V
Input voltage C range	V_{C8}	– 0.3 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 40 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	65	K/W

The anode voltage of the LEDs and the number of simultaneously active outputs should be selected so that a total power dissipation of 800 mW in the IC is not exceeded.

Operating Range

Supply voltage	V_{S7}	4.5 to 5.5	V
Ambient temperature	T_A	0 to 70	°C

Characteristics

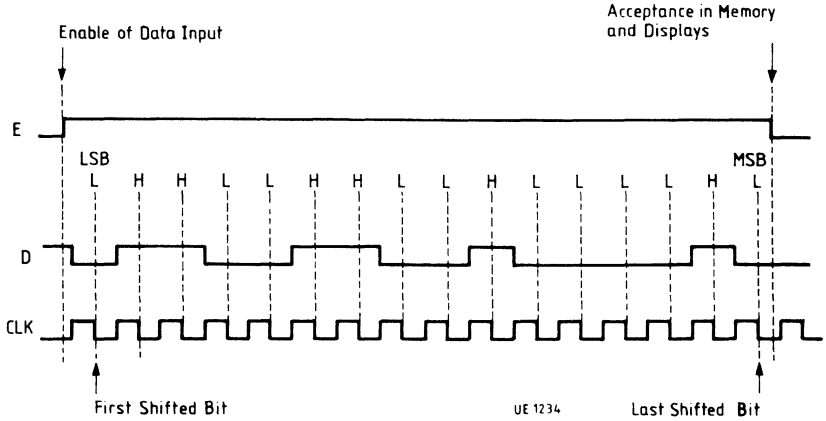
V_S = 5 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply current (all LEDs ON) I_Q = 10 mA	I_{S7}		10	15	mA
Quiescent current I_Q= 0; C = "L"	I_{S7}		2.5	3.5	mA
Switching voltage	$V_{S4,5,6}$	0.8	1.4	2.0	V
H - input current V_H = 5.5 V	$I_{H4,5,6}$			1	µA
L - input current V_L = 0.4 V	$-I_{L4,5,6}$			10	µA
Output current (V_Q = 2.9 V) (pins 1 to 3, 9 to 16, 18 to 22)	I_Q	8	10	12.5	mA
Output leakage current (V_Q = V_S) (pins 1 to 3, 9 to 16, 18 to 22)	I_{QI}			10	µA
Switching voltage C	V_{S8}	1.5	2.1	2.7	V
H - input current C V_{H8} = 5 V	I_{H8}		0.6	0.9	mA
L - input current C V_{L8} = 0 V	$-I_{L8}$			1	µA
H - input current C (at switching voltage)	I_{H8}			15	µA

Switching Times

CLK (pin 5)	H pulse width	t_{HCLK}	1			µs
	L pulse width	t_{LCLK}	2			µs
	Set-up time	t_{SCLK}	0			µs
	Hold time	t_{hCLK}	0			µs
D (pin 4)	Set-up time	t_{SD}	0.5			µs
	Hold time	t_{hD}	0.5			µs
E (pin 6)	H pulse width	t_{HE}	50			µs
	L pulse width	t_{LE}	0.5			µs
	Set-up time	t_{SE}	1.5			µs
	Hold time	t_{hE}	1			µs
A	Delay time	t_A	10			µs

Pulse Diagram



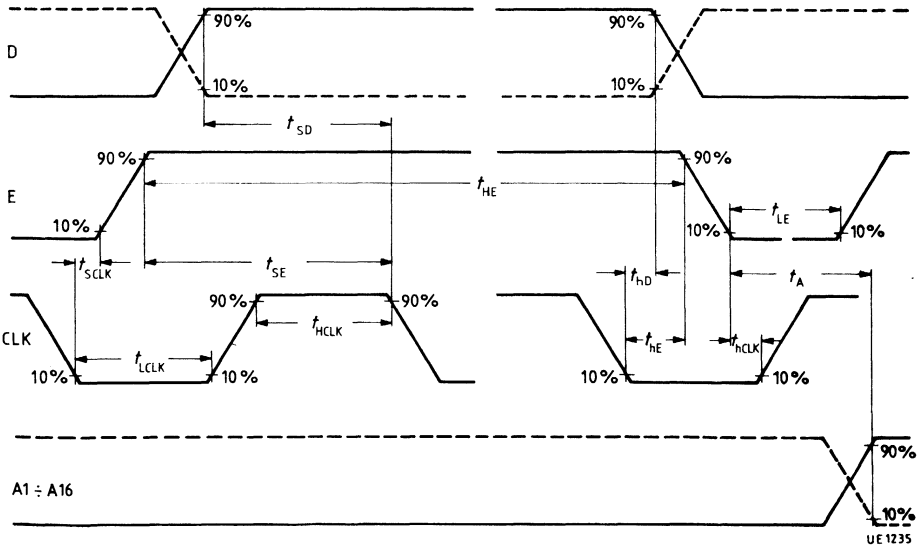
Memory contents after the falling edge of E

LSB MSB

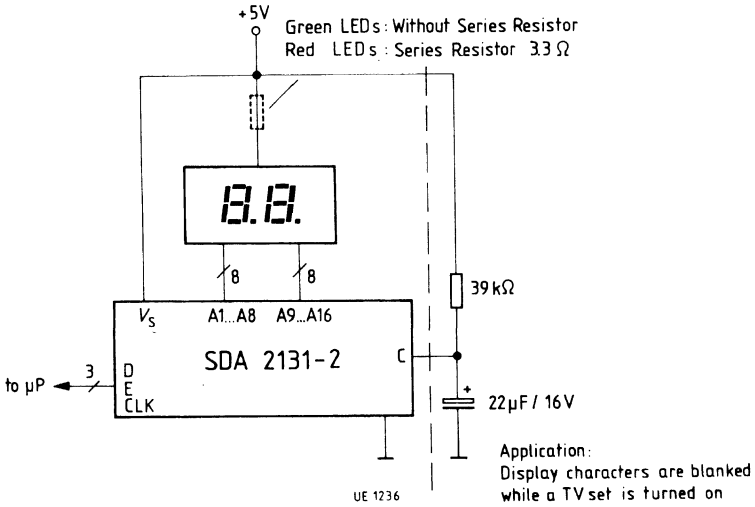
L H H L L H H L L H L L L L H L

The first information shifted to D with CLK is displayed at A1.

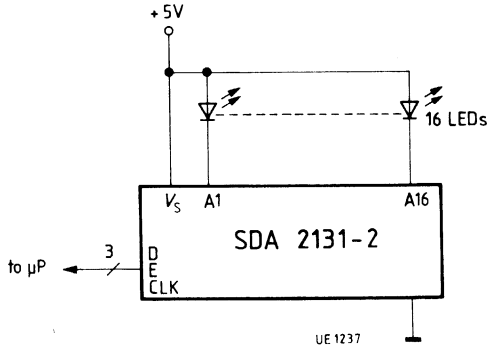
Pulse Diagram



Application Circuit 1
2-digit 7-segment display



Application Circuit 2
Point display (1 of 16 diodes illuminated)



SIEMENS

IR Remote Control Transmitter with IR Diode Driver — SDA 2208-3

Preliminary Data — **Bipolar IC**

The SDA 2208-3 is designed as a remote control transmitter for direct driving of infrared transmitter diodes. The instructions are generated by an input matrix (i. e. keyboard) in the form of biphase codes. Distributed over 8 levels, there are a max. of 512 instructions available. The newly designed SDA 2208-3 is feature compatible with the pins and functions of the SDA 2208-2. The SDA 2208-3 is much better protected against electrostatic discharges (ESD).

Type	Ordering Code	Package
SDA 2208-3	Q67000-A8235	P-DIP-20

Circuit Description

Voltage Supply

Voltage consumption ceases in the quiescent state and is activated subsequent to connecting the component's matrix. When the matrix is disconnected, the IC automatically completes the telegram and returns into the quiescent state.

Clock Input

The clock input is equipped with a ceramic resonator. This resonator oscillates with its parallel resonance. In addition, the clock signal can be injected at pin CLK I. The oscillator can be also operated by using an LC circuit with an isolating capacitor.

Input Matrix

The matrix is comprised of 8 rows and 8 columns. Column A is used as supply voltage V_S. In order to transmit a telegram, the respective rows and columns have to be connected. The transmitter is switched on and a telegram is output. The length of the telegram depends on the duration of the matrix connection. A telegram is comprised of a start command, a variable number of information commands (depending on the duration of the matrix connection).

Programming via PPIN

The programming pin is used to provide access to all command sets or 512 commands since the 8 × 8 matrix limits the use to one command set or 64 different commands. By subdividing the command sets into 8 levels of 64 commands each, a specific level can be selected by either keeping the PPIN open or by combining it with one of the seven column inputs (CPB to CPH). When connecting PPIN with one column alone, the standby supply current I_S does not increase.

Safety Features against Incorrect Operation

As a prerequisite for an error-free telegram output with at least one information command, the matrix connection has to be free of interferences and its clock-frequency-dependent, minimal duration should be approx. 60 ms at a clock frequency of 500 kHz. The applied integrated circuit is equipped with a preventive mechanism (key bouncing) against erroneous outputs, which automatically resets the circuit during each detected interference. Equally, operating errors caused by connecting more than one row and one column are detected. The telegram will be ended through continuous transmitting of end. Operating errors can be cancelled only by disconnecting all matrix connections. The level selection key (PPIN function) will be effective only if it is depressed prior to or simultaneously with the matrix key. Also, a simultaneous depressing of several selection keys has the same effect on the telegram as an erroneous matrix operation.

Composition of a Telegram

Subsequent to switch-on, the command No. 511 (10-bit word length) is output as start command to indicate to the receiver the onset of transmission. Depending on the duration of the matrix connection, a series of identical commands will follow. If a telegram is ended by disconnecting the matrix connection, not more than one additional information command will be issued to be followed immediately by the end command. This end command is identical with the start command.

Command Structure

Each command consists of a presignal, an infrared pause, a start bit and 9 information bits. During the duration of the presignal ($256/f_{CLK}$), the receiver performs a simple amplitude adjustment of the input amplifier.

The infrared pause appears between the end of the presignal and the onset of the start bit. Again, the receiver is provided with enough time to recognize transmission distortions based on the limits of the transmission range.

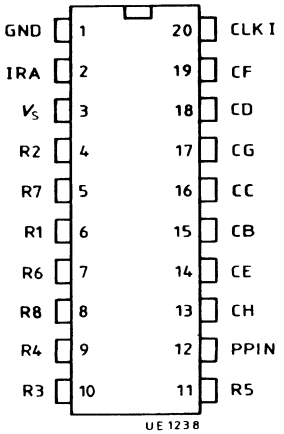
The start bit has been permanently programmed as "1" and is used as synchronization support for the receiver.

The bit structure has been **illustrated in the pulse diagram.**

Output Driver Stage

The fully integrated driver stage enables the direct connection of the infrared transmitter diodes to the infrared output IRA. The diode current is maintained at a constant level within a defined range to stabilize the transmitting power of the infrared diodes.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	GND	Ground
2	IRA	Output IRA
3	V_S	Supply voltage
4	R2	Matrix connection rows
5	R7	
6	R1	
7	R6	
8	R8	
9	R4	
10	R3	
11	R5	
12	PPIN	Programming Pin
13	CH	Matrix connection column
14	CE	
15	CB	
16	CC	
17	CG	
18	CD	
19	CF	
20	CLKI	Oscillator input

Absolute Maximum Ratings

T_A = 25 °C

Parameter	Symbol	Limit Values	Unit
Supply voltage range	V_S	– 0.3 to 10.5	V
Matrix rows	V_{row}	– 0.3 to V_S	V
Matrix columns	V_{col}	– 0.3 to V_S	V
Programming pin (PPIN)	V_{pp}	– 0.3 to V_S	V
Oscillator input (CLKI)	$V_{I\,OSC}$	– 0.3 to 2	V
Infrared output (IRA) inhibited in operation	 V_Q V_Q	 – 0.3 to 10.5 – 0.3 to 8	 V V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 40 to 150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	60	K/W

Operating Range

Supply voltage	V_S	4 to 10	V
Ambient temperature	T_A	0 to 70	°C
Oscillator frequency	f_{CLK}	430 to 530	kHz

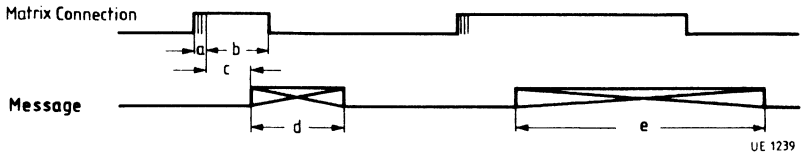
Characteristics

V_S = 5.5 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption transmitting phase standby operation	 I_S I_S		 19 < 1	 10	 mA µA
Output current IRA 2 V < V_2 < 6 V	I_2	500	900	1000	mA
Connecting resistance (row-column or column-PPIN)	$R_{row\,col}$			500	Ω

Pulse Diagrams

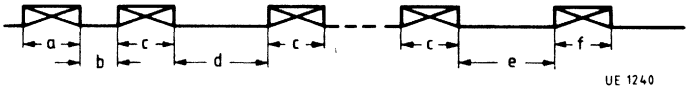
Basic Operating Sequence



for 500 kHz
b = 60.928 ms
c = 26.624 ms
d = 177.664

a) bounce
b) minimum key operating time to complete telegram with one information instruction
c) delay between the on-set of error-free matrix connection and on-set of telegram
d) telegram with one information command
e) telegram with several identical information commands

Composition of Telegram



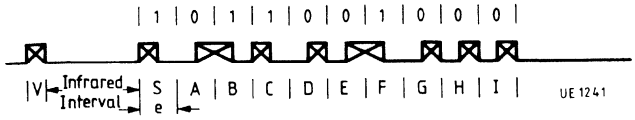
for 500 kHz
a = c = f = 13.312 ms
b = 19.968 ms
d = e = 177.76 ms

a) start command 10 bits
b) time interval between start and information command
c) information command 10 bits
d) time interval between identical information commands
e) time interval between information and end command
f) end command 10 bits

The timespan of an error-free matrix connection determines the number of identical information commands.

Pulse Diagrams

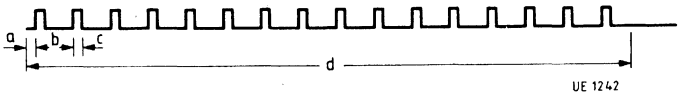
Command Structure in Biphase Code



Time duration
single bit e: $512/f_{CLK}$
presignal V: $256/f_{CLK}$
infrared pause: $5 \times 256/f_{CLK}$

start bit S is always 1
bits A to I are addressable

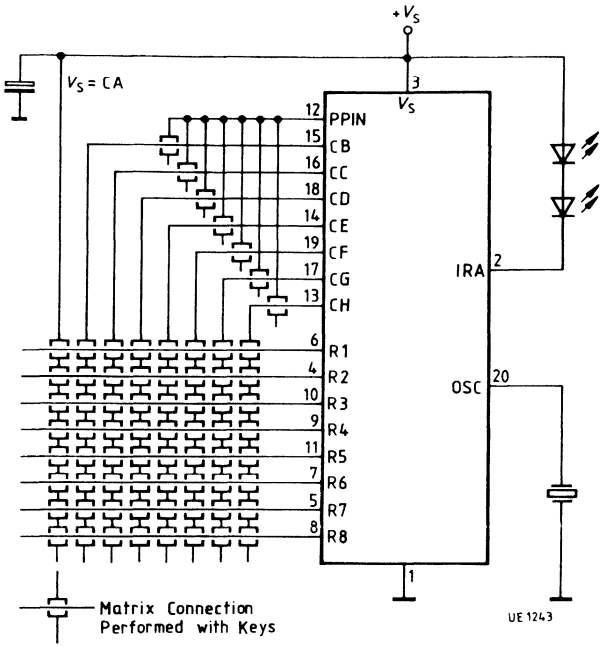
Structure of the Modulated Half Bit (as well as the presignal)



a = c = $4/f_{CLK}$
b = $16/f_{CLK}$
d = $256/f_{CLK}$
16 pulses per half bit

The H signal indicates a constant current source at Q_{IRA}. The infrared transmitter diode is then active.

Block Diagram



Since the infrared transmitter diodes have to be driven with pulse currents of approx. 1 A, the following has to be complied with during the layout of the PC board:

1) The smoothing capacitor between V_S and ground should be located as closely as possible to the pins of the IC.
2) The supply line to the transmitter diodes is not to cause cross-talk in the key matrix.
3) No residual currents are to flow over the connection ceramic oscillator/ground pin.

Truth Table

No. of the instruction	Matrix connection row-column	Binary code IRA information instruction A	B	C	D	E	F	G	H	I
0	1A	0	0	0	0	0	0	0	0	0
1	1B	1	0	0	0	0	0	0	0	0
2	1C	0	1	0	0	0	0	0	0	0
3	1D	1	1	0	0	0	0	0	0	0
4	1E	0	0	1	0	0	0	0	0	0
5	1F	1	0	1	0	0	0	0	0	0
6	1G	0	1	1	0	0	0	0	0	0
7	1H	1	1	1	0	0	0	0	0	0
8	2A	0	0	0	1	0	0	0	0	0
9	2B	1	0	0	1	0	0	0	0	0
10	2C	0	1	0	1	0	0	0	0	0
11	2D	1	1	0	1	0	0	0	0	0
12	2E	0	0	1	1	0	0	0	0	0
13	2F	1	0	1	1	0	0	0	0	0
14	2G	0	1	1	1	0	0	0	0	0
15	2H	1	1	1	1	0	0	0	0	0
16	3A	0	0	0	0	1	0	0	0	0
17	3B	1	0	0	0	1	0	0	0	0
18	3C	0	1	0	0	1	0	0	0	0
19	3D	1	1	0	0	1	0	0	0	0
20	3E	0	0	1	0	1	0	0	0	0
21	3F	1	0	1	0	1	0	0	0	0
22	3G	0	1	1	0	1	0	0	0	0
23	3H	1	1	1	0	1	0	0	0	0
24	4A	0	0	0	1	1	0	0	0	0
25	4B	1	0	0	1	1	0	0	0	0
26	4C	0	1	0	1	1	0	0	0	0
27	4D	1	1	0	1	1	0	0	0	0
28	4E	0	0	1	1	1	0	0	0	0
29	4F	1	0	1	1	1	0	0	0	0
30	4G	0	1	1	1	1	0	0	0	0
31	4H	1	1	1	1	1	0	0	0	0
32	5A	0	0	0	0	0	1	0	0	0
33	5B	1	0	0	0	0	1	0	0	0
34	5C	0	1	0	0	0	1	0	0	0
35	5D	1	1	0	0	0	1	0	0	0
36	5E	0	0	1	0	0	1	0	0	0
37	5F	1	0	1	0	0	1	0	0	0
38	5G	0	1	1	0	0	1	0	0	0
39	5H	1	1	1	0	0	1	0	0	0
40	6A	0	0	0	1	0	1	0	0	0

Truth Table (cont'd)

No. of the instruction	Matrix connection row-column	Binary code IRA information instruction A	B	C	D	E	F	G	H	I
41	6B	1	0	0	1	0	1	0	0	0
42	6C	0	1	0	1	0	1	0	0	0
43	6D	1	1	0	1	0	1	0	0	0
44	6E	0	0	1	1	0	1	0	0	0
45	6F	1	0	1	1	0	1	0	0	0
46	6G	0	1	1	1	0	1	0	0	0
47	6H	1	1	1	1	0	1	0	0	0
48	7A	0	0	0	0	1	1	0	0	0
49	7B	1	0	0	0	1	1	0	0	0
50	7C	0	1	0	0	1	1	0	0	0
51	7D	1	1	0	0	1	1	0	0	0
52	7E	0	0	1	0	1	1	0	0	0
53	7F	1	0	1	0	1	1	0	0	0
54	7G	0	1	1	0	1	1	0	0	0
55	7H	1	1	1	0	1	1	0	0	0
56	8A	0	0	0	1	1	1	0	0	0
57	8B	1	0	0	1	1	1	0	0	0
58	8C	0	1	0	1	1	1	0	0	0
59	8D	1	1	0	1	1	1	0	0	0
60	8E	0	0	1	1	1	1	0	0	0
61	8F	1	0	1	1	1	1	0	0	0
62	8G	0	1	1	1	1	1	0	0	0
63	8H	1	1	1	1	1	1	0	0	0

	G	H	I
Command 0 to 63: PPIN free	0	0	0
Command 64 to 127: PPIN connected with CB	1	0	0
Command 128 to 191: PPIN connected with CC	0	1	0
Command 192 to 255: PPIN connected with CD	1	1	0
Command 256 to 319: PPIN connected with CE	0	0	1
Command 320 to 383: PPIN connected with CF	1	0	1
Command 384 to 447: PPIN connected with CG	0	1	1
Command 448 to 511: PPIN connected with CH	1	1	1

In every command set, the assignment instruction – matrix connection (row – column) is analogous to the group 0 to 63.

Example:

Command 64 is generated, when PPIN is connected with CB, and R1 with CA.

SIEMENS

Nonvolatile Memory 1-Kbit E²PROM with 3-Line Bus — SDA 2506-2

Preliminary Data — **MOS IC**

Features

- Word-organized, reprogrammable nonvolatile memory in n-channel floating-gate technology
- 128 word × 8 bit organization
- Supply voltage 5 V
- Three lines between control processor and E²PROM for data transfer and chip control
- Serial data bus (eight data bits, seven address bits, one control bit)
- More than 10^4 reprogramming cycles per address
- Data retention for more than ten years (operating-temperature range)
- Unlimited number of readout operations without refresh
- Erase or write in 10 ms
- Temperature range 0 to 70 °C

Type	Ordering Code	Package
SDA 2506-2	Q67100-H5009	P-DIP-8

Circuit Description

Data Transfer and Chip Control

Three lines, each with several functions, are necessary for overall data transfer between the control processor and the E²PROM:

a) Data line D
- bidirectional serial data transfer
- serial entry of address and control bit
- direct control, D = 1 for erase, D = 0 for write

b) Clock line Φ
- shift clock for data, address and control bits
- start readout with transfer of data from memory into shift register or start of data change during reprogramming

c) Chip-enable line $\overline{CE}$
- chip reset and data input (active high)

Before the chip is enabled, data, address and control information is clocked in on the bidirectional data bus. These data are retained in the shift register during reprogramming and readout until the second clock pulse. The following data formats have to be entered:

a) Readout memory, one 8-bit control word consisting of
- seven address bits A0 through A6 (A0 first as LSB)
- one control bit CB = 0 after A6
-

Reprogram Memory

b) Erase, 8-bit input information consisting of
- seven bits of address information A0 through A6 (A0 first as LSB)
- one bit of control information CB = 1 after A6

c) Write, 16-bit input information consisting of
- eight bits of new memory information D0 through D7 (D0 first as LSB)
- seven bits of address information A0 through A6 (A0 first as LSB after D7)
- one bit of control information CB = 1 after A6

d) Erase and write, 16-bit input information consisting of
- eight bits of new memory information D0 through D7 (D0 first as LSB)
- seven bits of address information A0 through A6 (A0 first as LSB after D7)
- one bit of control information CB = 1 after A6
-

Read (see figure 1)

After data entry, and with CB = 0, the readout operation of the selected word address is started with the transition of $\overline{CE}$ from 1 to 0. The information on the data line during chip enable has no effect.

With the first clock pulse after $\overline{CE}$ = 0, the data word of the selected memory address is transferred into the shift register. With the trailing edge of the first clock pulse the data output goes low-impedance and the first data bit D0 can be read on the data pin. Every further clock pulse shifts another data bit to the output. The data line goes high-impedance again when $\overline{CE}$ changes from 0 to 1).

Reprogram (see figure 2a, 2b and 3)

A complete reprogramming operation consists of an erase operation followed by a write operation. During erase, all bits of the selected word are set to a uniform 1 state, and during write, 0 states are created according to the information in the shift register.

A reprogramming operation is started when, after data entry in chip enable, the control bit CB = 1 appears in the appropriate cell of the shift register. Whether an erase or a write operation is performed will depend on the information on data line D during chip enable.

For resetting to the 1 state there must also be a 1 on the data input during the transition of $\overline{CE}$ from high to low. If a write operation to the 0 state is to be started however, there must be a 0 on the data line during chip enable.

Reset

A memory that is not selected is automatically in reset status because of the 1 state of $\overline{CE}$. All flipflops of the sequencer are reset. The information in the shift register is retained on the other hand and is not altered until data are shifted. The reset status is also produced by an on-chip circuit when the memory is powered on.

After chip enable a start pulse is required on clock line Φ to initiate programming. The control information on data line D must remain stable until the leading edge of the start pulse. The programming operation begins with the trailing edge of the start pulse and ends with transition of $\overline{CE}$ from low to high.

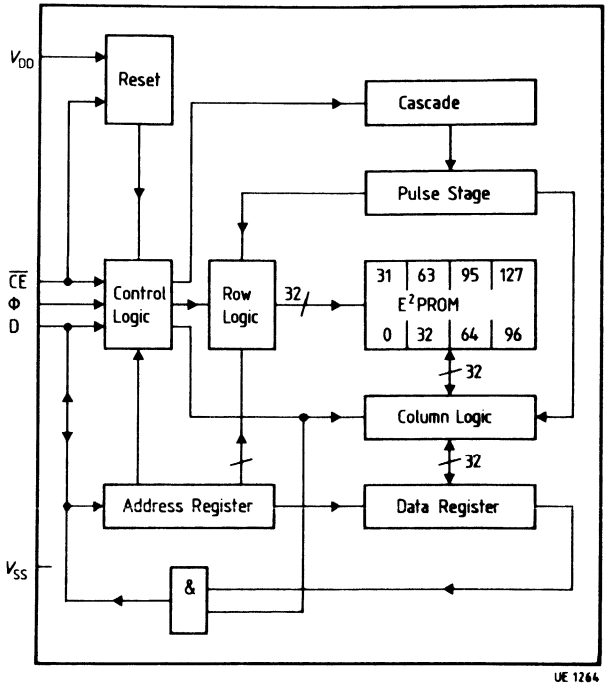
The reprogramming of a word begins with an erase operation. For this the word address is entered together with control bit CB = 1. The entry of the data word is omitted for an erase. But at this point the data for a following write operation can be entered. If this is intended, the data D0 through D7 for the write operation are entered before entry of the control word for the erase operation. For the erase the data line has to be kept high during chip enable, i. e. transition of $\overline{CE}$ from high to low, and until the trailing edge of the start pulse. An erase operation can be followed immediately by a write operation without entry of the data and word address. For this the data line is sent low, $\overline{CE}$ is again driven from high to low (chip enable) and the start pulse for the write operation is put on clock line Φ. The data line must be kept low until the trailing edge of the start pulse (**see figure 3**).

Erase and write can also be executed separately. For writing, a 16-bit control word (word address with control bit CB = 1, data D0-D7) is entered. For erasing, only the word address and CB = 1 are entered. For the erase operation the data line must be kept high during chip enable and until the trailing edge of the start pulse, and for the write operation it must be kept low (**see figure 2a and 2b**).

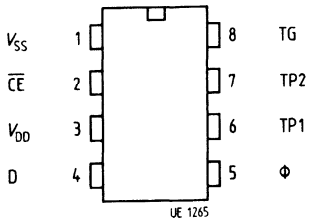
Total Erase

If input TP (pin 7) is put on V_{DD} = 5 V, this activates the mode for total erasure of memory. The word address 0 and control bit CB = 1 must be entered. The data line has to be kept high during chip enable (transition of $\overline{CE}$ from high to low) and until the trailing edge of the start pulse. A total erase operation is ended when $\overline{CE}$ goes from low to high and by switching input TP to 0 V.

Block Diagram



Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{SS}	Ground
2	$\overline{CE}$	$\overline{CE}$ = 1 for control-word entry $\overline{CE}$ = 0 for reprogramming and data readout
3	V_{DD}	Supply voltage +5 V
4	D	Bidirectional data input/output line, for reprogramming: D = 1 erase D = 0 write
5	Φ	Clock
6	TP1	Test pin
7	TP2	Test pin
8	TG	Test pin

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{DD}	– 0.3	6	V
Input voltage	V_I	– 0.3	6	V
Power dissipation	P_D		40	mW
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		100	K/W

Operating Range

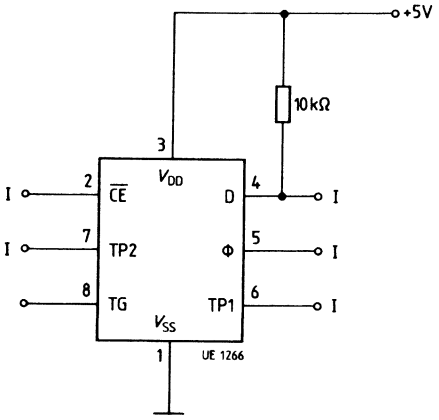
Supply voltage	V_{DD}	4.75	5.25	V
Ambient temperature	T_A	0	70	°C

Characteristics

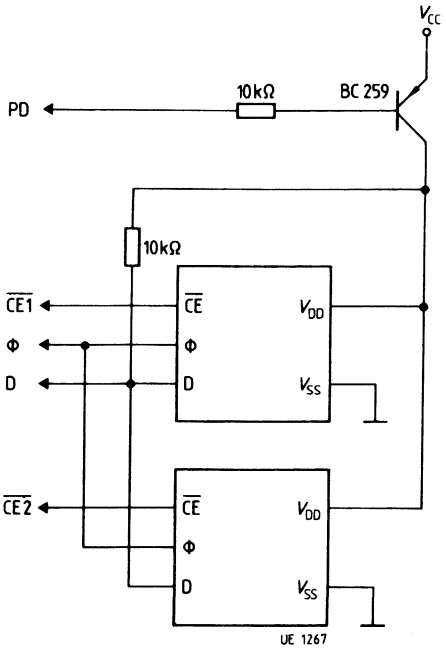
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{DD}	4.75	5	5.25	V	
Supply current	I_{DD}			3	mA	V_{DD} = 5.25 V
Inputs						
Input voltage (D, Φ, $\overline{CE}$)	V_L			0.8	V	
Input voltage (D, Φ, $\overline{CE}$)	V_H	2.4			V	
Input current (D, Φ, $\overline{CE}$)	I_H			10	µA	V_H = 5.25 V
Data Output D (open drain)						
L-output current	I_L			0.5	µA	V_L = 0.8 V
H-output current	I_H			10	µA	V_H = 5.25 V
Clock Pulse Φ						
High duration	t_H	2.5		60	µs	
Low duration	t_L	5			µs	
Edge interval $\overline{CE}$ to D	Δt	2.5			µs	
Edge interval $\overline{CE}$ to Φ	t_{CE}	5			µs	
Data hold (before/after Φ trailing edge)	t_{HD}	2.5			µs	
Data delay (after Φ trailing edge)	t_{DD}	2.5			µs	
Rise time	t_R			1	µs	
Fall time	t_F			1	µs	
Chip erase	t_{er}	10		20	ms	
Chip write	t_{wr}	10		20	ms	
Total erase	$t_{tot\ er}$			20	ms	

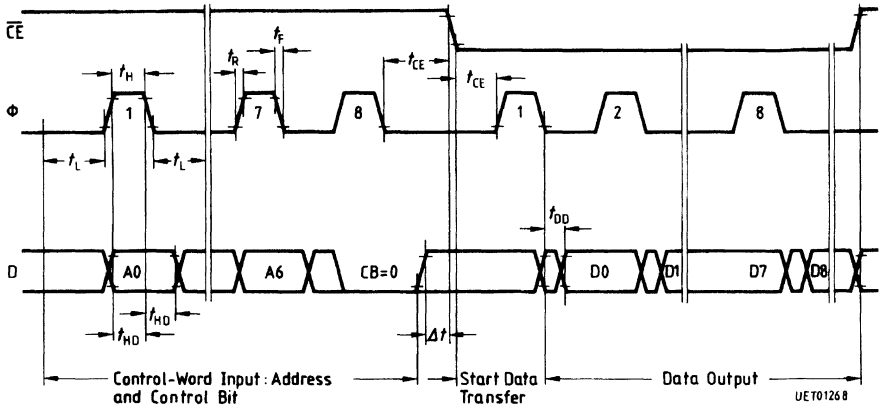
Test Circuit



Application Circuit

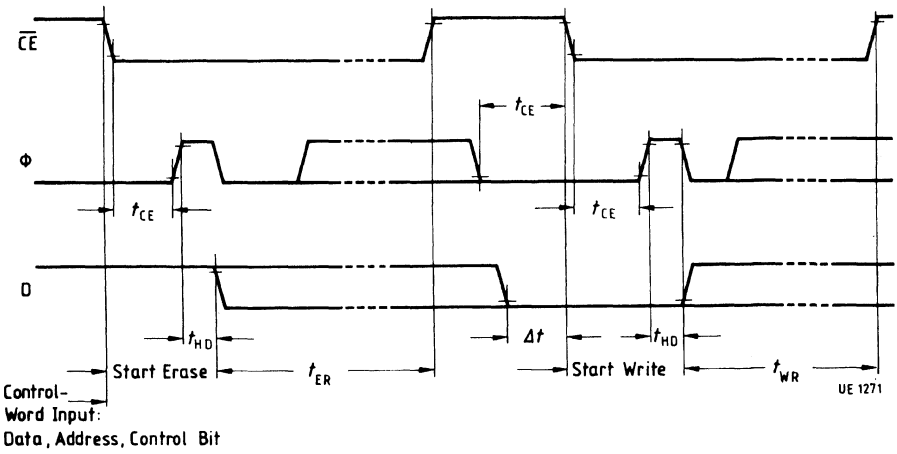


Read

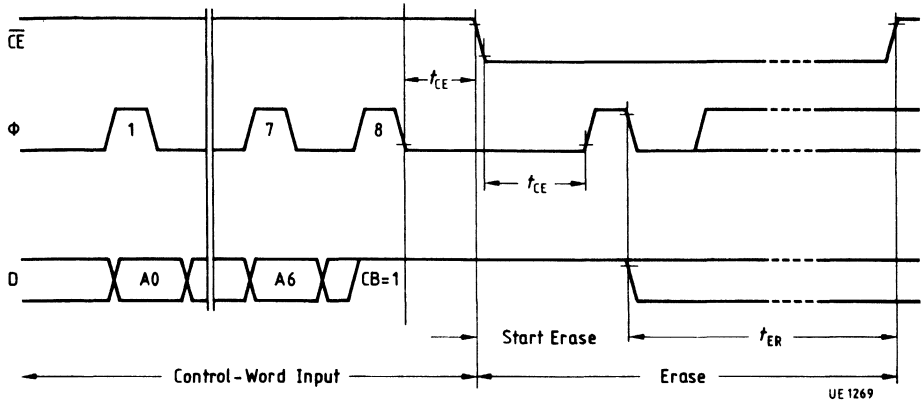


t_{CE} = 5µs ; $t_R = t_F$ = 1µs t_{DD} = 2.5µs ; t_H = 2.5µs
t_{HD} = 2.5µs ; t_L = 5µs Δt = 2.5µs

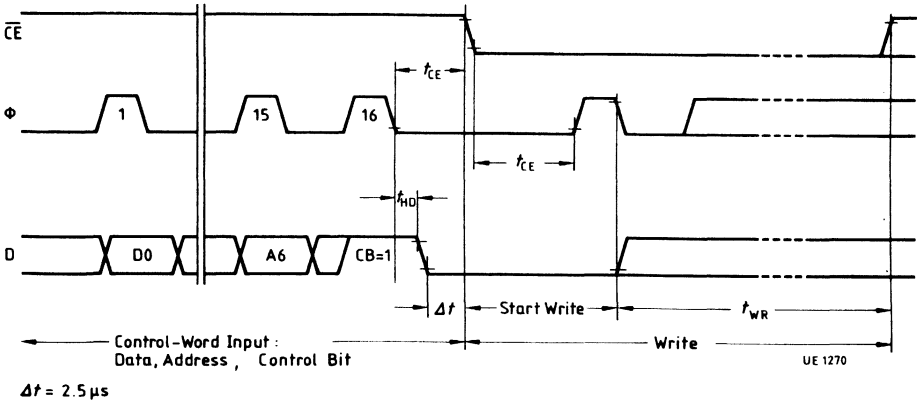
Reprogram/Erase and Write



Reprogram/Erase



Reprogram/Write



Δt = 2.5 µs

Nonvolatile Memory 1-Kbit E²PROM with I²C Bus

SDA 2516-2

Preliminary Data

MOS IC

Features

- Word-organized, reprogrammable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 128 × 8 bit organization
- Supply voltage 5 V
- Serial 2-line bus for data input and output (I²C Bus)
- Reprogramming mode, 10 ms erase/write cycle
- Reprogramming by means of on-chip control (without external control)
- Check for end of programming process
- Data retention > 10 years
- More than 10^4 reprogramming cycles per address
- Compatible with SDA 2516. Exception: Conditions for total erase and current consumption I_{DD}.

Type	Ordering Code	Package
SDA 2516-2	Q67100-H5002	P-DIP-8

Circuit Description

I²C Bus Interface

The I²C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a serial data line SDA and a serial clock line SCL. The data line requires an external pull-up resistor to V_{DD} (open drain output stage).

The possible operational states of the I²C bus are shown in **figure 1.** In the quiescent state, both lines SDA and SCL are high, i.e. the output stage of the data line is disabled. As long a SCL remains "1", information changes on the data bus indicate the start or the end of data transfer between two components.
The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" is a stop condition. During a data transfer the information on the data bus will only change while the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".
In conjunction with an I²C bus system, the memory component can operate as a receiver and as a transmitter (slave receiver or slave transmitter). Between a start and stop condition, information is always transmitted in byte-organized form. Between the trailing edge of the eighth clock pulse and a ninth acknowledge clock pulse, the memory component sets the SDA line to low as a confirmation of reception, if the chip select conditions have been met. During the output of data, the data output of the memory is high in impedance during the ninth clock pulse (acknowledge master).
The signal timing required for the operation of the I²C bus is summarized in **figure 2.**

Control Functions of the I²C Bus

The memory component is controlled by the controller (master) via the I²C bus in two operating modes: read-out cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes and an additional acknowledge clock pulse to the bus after the start condition. During a memory read, at least nine additional clock pulses are required to accept the data from the memory and the acknowledge master, before the stop condition may follow. In the case of programming, the active programming process is only started by the stop condition after data input **(see figure 3)**.
The chip select word contains the 3 chip select bits CS0, CS1 and CS2, thus allowing 8 memory chips to be connected in parallel. Chip select is achieved when the three control bits logically correspond to the selected conditions at the select inputs.

Check for End of Programming or Abortion of Programming Process

If the chip is addressed during active reprogramming by entering CS/E, the programming process is terminated. If, however, it is addressed by entering CS/A, the entry will be ignored. Only after programming has been terminated will the chip respond to CS/A. This allows the user to check whether the end of the programming process has been reached **(see figure 3).**

Memory Read

After the input of the first two control words CS/E and WA, a resetting of the start condition and the input of the third control word CS/A, the memory is set ready to read. During acknowledge clock nine, the memory information is transferred in parallel mode to the shift register. Subsequent to the trailing edge of the acknowledge clock, the data output is low impedance and the first data bit can be sampled **(see figure 4)**.
With every shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented when the master receiver switches the data line to "low" during the ninth clock (acknowledge master). Any number of memory locations can thus be read one after the other. At address 128, an overflow to address 0 is not initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into the "1" state. During write, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word.
After the 27th and last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under onchip control.
The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage, the erase/write process extends over max. 20 ms, or more typically, 10 ms. In the case of data word input without write request (write request is defined as data bit in data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

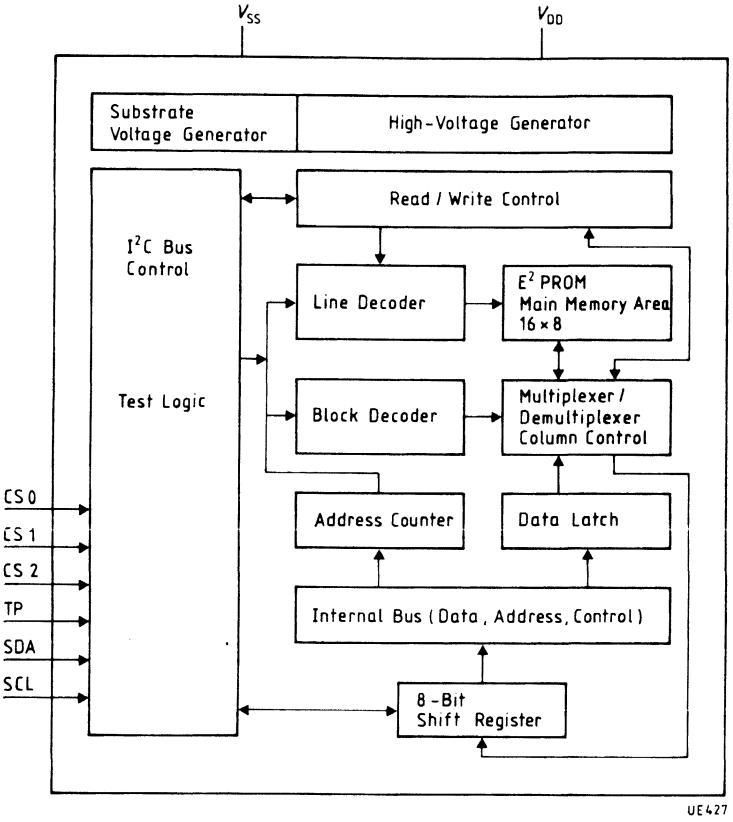
- **Important: Switch-On Mode and Chip Reset**

  After the supply voltage V_{DD} has been connected, the data output will be in high-impedance mode. As a rule, **the first operating mode** to be entered, should be the **read process of a word address.** As a result of the built-in "power on reset" circuit, programming requests will not be accepted immediately after the supply voltage has been switched on.

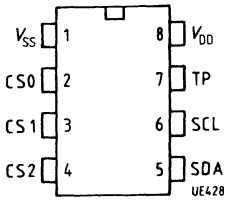
Total Erase

Enter the control word CS/E, load the address register with address 0 and the data register with FF (hex) to erase the entire contents of the memory. Switch input CS2 to "open" immediately prior to generating the stop condition. The subsequent stop condition triggers a total erase. Upon termination of "total erase", CS2 must be reconnected to either 0 V or $\geq$ 4.5 V.

Block Diagram



Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{SS}	Ground
2	CS0	Chip select
3	CS1	Chip select
4	CS2	Chip select $0 \leq V_I \leq 0.2V$; $4.5 \leq V_I \leq V_{DD}$, open, total erase condition
5	SDA	Data line
6	SCL	Clock line
7	TP	Test pin
8	V_{DD}	Supply voltage

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{DD}	– 0.3	6	V
Input voltage	V_I	– 0.3	6	V
Power dissipation	P_D		130	mW
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		100	K/W
Junction temperature	T_j		85	°C

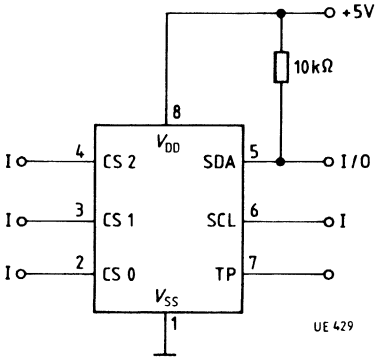
Operating Range

Supply voltage	V_{DD}	4.75	5.25	V
Ambient temperature	T_A	0	70	°C

Characteristics
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{DD}	4.75	5.0	5.25	V	
Supply current	I_{DD}			20	mA	V_{DD} = 5.25 V
Inputs						
Input voltages SDA/SCL	V_{IL}			1.5	V	
Input voltages SDA/SCL	V_{IH}	3.0		V_{DD}	V	
Input currents SDA/SCL	I_H			10	µA	$V_{IH} = V_{DD}$
Output						
Output current SDA	I_{QL}			3.0	mA	V_{QL} = 0.4 V
Leakage current SDA	I_{QH}			10	µA	$V_{QH} = V_{DD}$ max
Inputs						
Input voltages CS0/CS1/CS2	V_{IL}			0.2	V	
Input voltages CS0/CS1/CS2	V_{IH}	4.5		V_{DD}	V	
Input currents CS0/CS1/CS2	I_{IH}			100	µA	V_{DD} = 5.25 V
Clock frequency	f_{SCL}			100	kHz	
Reprogramming duration	t_{PROG}		10	20	ms	erase and write
Input capacity	C_i			10	pF	
Total erase	t_{GL}			20	ms	CS 2 = open

Application Circuit



Application Circuit

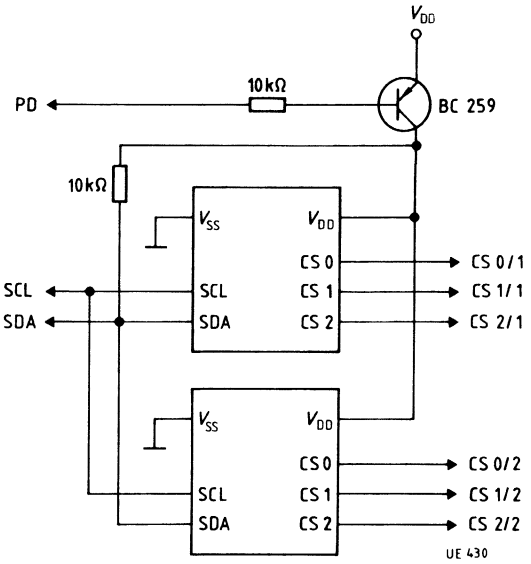


Figure 1
Operation States of the I²C Bus

Read Access Short Form

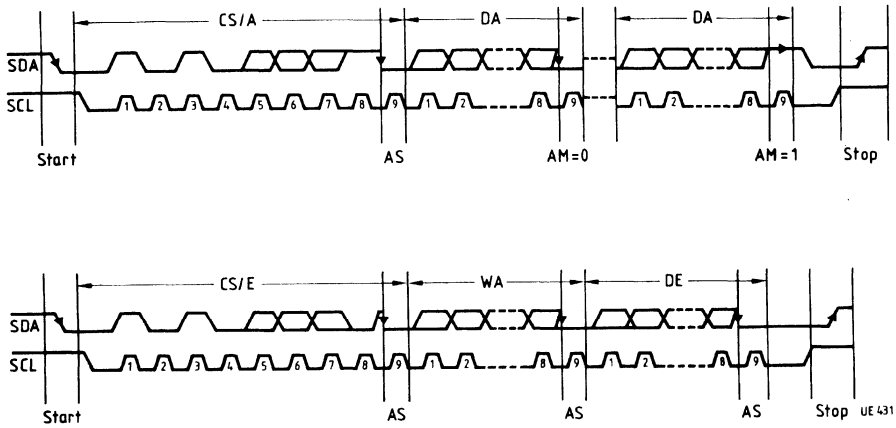
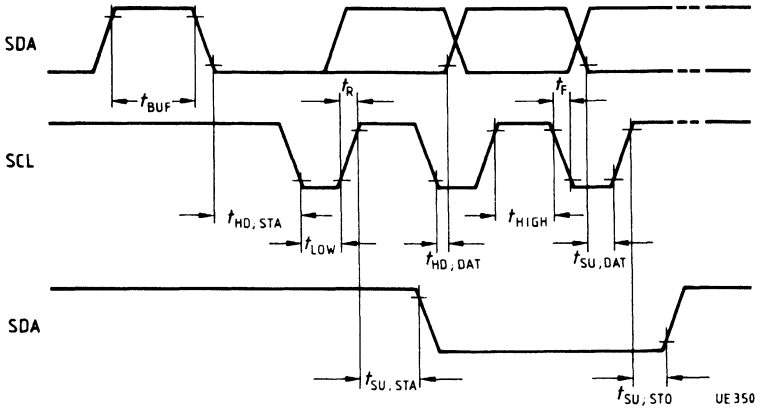


Figure 2
Timing Condition for the I²C Bus (high-speed mode)



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Minimum time the bus must be free before a new transmission can start	t_{BUF}	4.7		µS µS
Start condition hold time	$t_{HD;STA}$	4.0		µS
Clock LOW period	t_{LOW}	4.7		µS
Clock HIGH period	t_{HIGH}	4.0		
Start condition set-up time, only valid for repeated start code	$t_{SU;STA}$	4.7		µS nS
Data set-up time	$t_{SU;DAT}$	250		µS
Rise time of both the SDA and SCL line	t_R		1	nS
Fall time of both the SDA and SCL line	t_F		300	µS
Stop condition set-up time	$t_{SU;STO}$	4.7		
Hold time data	$t_{HD;DAT}$	0*)		

*) Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max .300 ns) of the falling edge of SCL.

Figure 3
Programming

Control word input

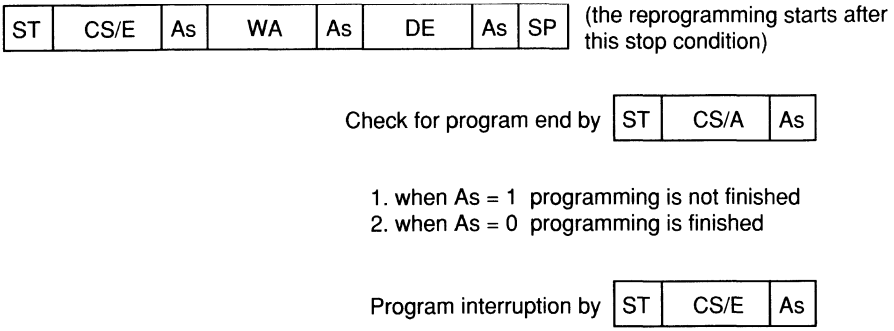
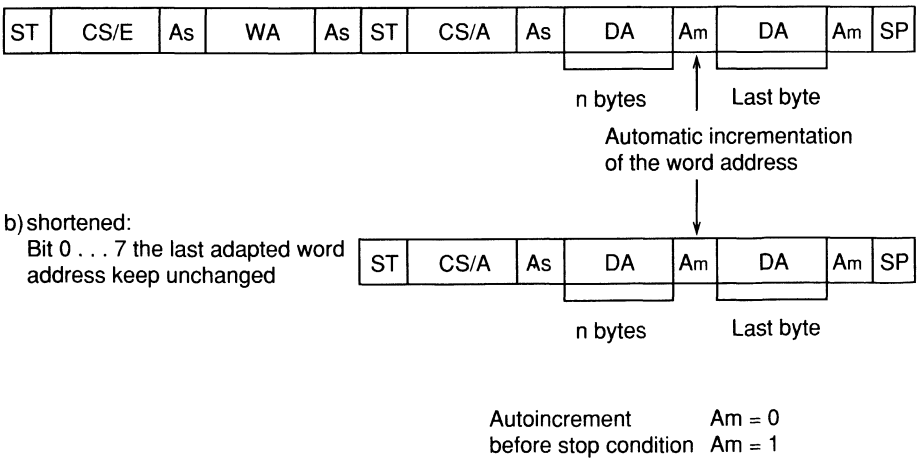


Figure 4
Read

Control word input read
a) complete (with word address input)



Control Word Table

Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	through memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	through memory
WA	0	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0/1	through master

Control Word Input Key

CS/E	Chip select data input into memory
CS/A	Chip select for data output out of memory
WA	Memory word address
DE	Data word for memory
DA	Data word read out of memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS0/CS1/CS2	Chip select bits
A0 to A6	Memory word address bits

Nonvolatile Memory 2-Kbit E²PROM with I²C Bus — SDA 2526-2

Preliminary Data — **MOS IC**

Features

- Word-organized programmable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 256 × 8 bit organization
- Supply voltage 5 V
- Serial 2-line bus for data input and output (I²C bus)
- Reprogramming mode, 10 ms erase/write cycle
- Reprogramming by means of on-chip control (without external control)
- Check for end of programming process
- Data retention > 10 years
- More than 10^4 reprogramming cycles per address
- Compatible with SDA 2526. Exceptions: Conditions for total erase and current consumption I_{DD}

Type	Ordering Code	Package
SDA 2526-2	Q67100-H5001	P-DIP-8

Circuit Description

I²C Bus Interface

The I²C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a serial data line SDA and a serial clock line SCL. The data line requires an external pull-up resistor to V_{DD} (open drain output stage).

The possible operational states of the I²C bus are shown in **figure 1**. In the quiescent state, both lines SDA and SCL are high, i.e. the output stage of the data line is disabled. As long a SCL remains "1", information changes on the data bus indicate the start or the end of data transfer between two components.

The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" is a stop condition. During a data transfer the information on the data bus will only change while the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I²C bus system, the memory component can operate as a receiver and as a transmitter (slave receiver or slave transmitter). Between a start and stop condition, information is always transmitted in byte-organized form. Between the trailing edge of the eighth clock pulse and a ninth acknowledge clock pulse, the memory component sets the SDA line to low as a confirmation of reception, if the chip select conditions have been met. During the output of data, the data output of the memory is high in impedance during the ninth clock pulse (acknowledge master).

The signal timing required for the operation of the I²C bus is summarized in **figure 2**.

Control Functions of the I²C Bus

The memory component is controlled by the controller (master) via the I²C bus in two operating modes:read-out cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes and an additional acknowledge clock pulse to the bus after the start condition. During a memory read, at least nine additional clock pulses are required to accept the data from the memory and the acknowledge master, before the stop condition may follow. In the case of programming, the active programming process is only started by the stop condition after data input (**see figure 3**).

The chip select word contains the 3 chip select bits CS0, CS1 and CS2, thus allowing 8 memory chips to be connected in parallel. Chip select is achieved when the three control bits logically correspond to the selected conditions at the select inputs.

Check for End of Programming or Abortion of Programming Process

If the chip is addressed during active reprogramming by entering CS/E, the programming process is terminated. If, however, it is addressed by entering CS/A, the entry will be ignored. Only after programming has been terminated will the chip respond to CS/A. This allows the user to check whether the end of the programming process has been reached (**see figure 3**).

Memory Read

After the input of the first two control words CS/E and WA, a resetting of the start condition and the input of the third control word CS/A, the memory is set ready to read. During acknowledge clock nine, the memory information is transferred in parallel mode to the shift register. Subsequent to the trailing edge of the acknowledge clock, the data output is low impedance and the first data bit can be sampled (**see figure 4**).

With every shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented when the master receiver switches the data line to "low" during the ninth clock (acknowledge master). Any number of memory locations can thus be read one after the other. At address 256, an overflow to address 0 is initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into the "1" state. During write, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word. After the 27th and last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control.

The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage, the erase/write process extends over max. 20 ms, or more typically, 10 ms. In the case of data word input without write request (write request is defined as data bit in data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

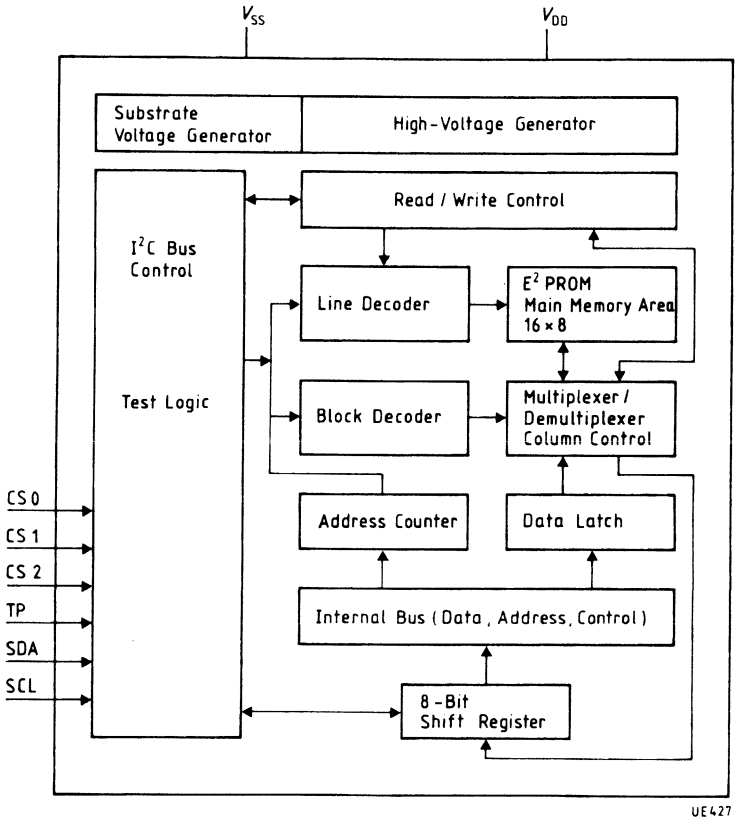
Important: Switch-On Mode and Chip Reset

After the supply voltage V_{DD} has been connected, the data output will be in high-impedance mode. As a rule, **the first operating mode** to be entered, should be the **read process of a word address**. As a result of the built-in "power on reset" circuit, programming requests will not be accepted immediately after the supply voltage has been switched on.

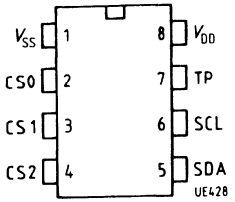
Total Erase

Enter the control word CS/E, load the address register with address 0 and the data register with FF (hex) to erase the entire contents of the memory. Switch input CS2 to "open" immediately prior to generating the stop condition. The subsequent stop condition triggers a total erase. Upon termination of "total erase", CS2 must be reconnected to either 0 V or $\geq$ 4.5 V.

Block Diagram



Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{SS}	Ground
2	CS0	Chip select
3	CS1	Chip select
4	CS2	Chip select $0 \leq V_I \leq 0.2$ V; $4.5 \leq V_I \leq V_{DD}$, open condition for erase of the complete memory
5	SDA	Data line
6	SCL	Clock line
7	TP	Test pin
8	V_{DD}	Supply voltage

Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage range	V_{DD}	– 0.3	6	V
Input voltage range	V_I	– 0.3	6	V
Power dissipation	P_V		130	mW
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		100	K/W
Junction temperature	T_j		85	°C

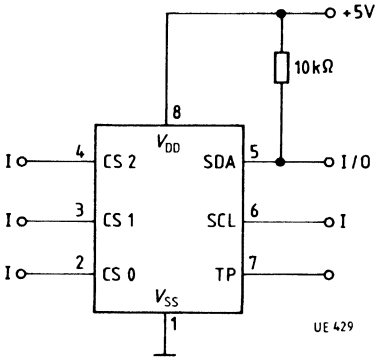
Operating Range

Supply voltage	V_{DD}	4.75	5.25	V
Ambient temperature	T_A	0	70	°C

Characteristics
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD}	4.75	5.0	5.25	V
Supply current (V_{DD} = 5.25 V)	I_{DD}			20	mA
Inputs					
Input voltages SDA/SCL	V_{IL}			1.5	V
Input voltages SDA/SCL	V_{IH}	3.0		V_{DD}	V
Input currents ($V_{IH} = V_{DDmax}$)	I_{IH}			10	µA
Output					
Output current SDA (V_{QL} = 0.4 V)	I_{QL}			3.0	mA
Leakage current ($V_{QH} = V_{DDmax}$)	I_{QH}			10	µA
Inputs					
Input voltages CS0/CS1/CS2	V_{IL}			0.2	V
Input voltages CS0/CS1/CS2	V_{IH}	4.5		V_{DD}	V
Input current CS0/CS1/CS2	I_{IH}			100	µA
Clock frequency	f_{SCL}			100	kHz
Reprogramming duration (erase and write)	t_{prog}		10	20	ms
Input capacity	C_I			10	pF
Total erase (CS2 = open)	t_{GL}			20	ms

Test Circuit



Application Circuit

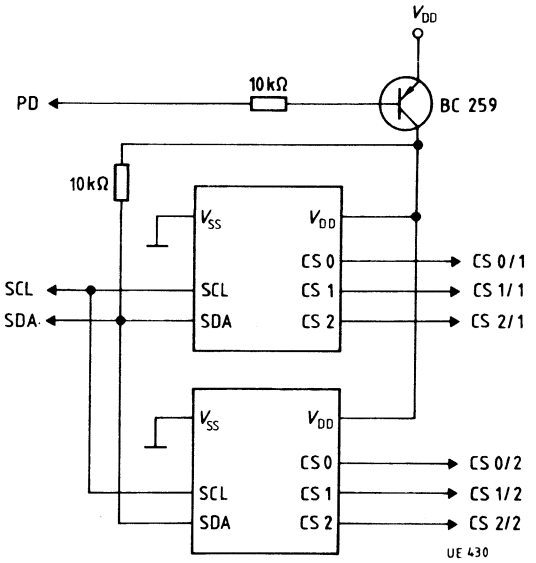
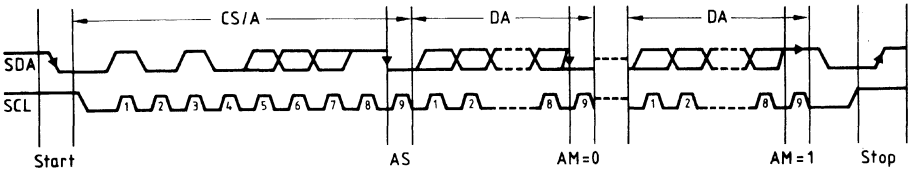


Figure 1
Operation States of the I²C Bus

Read Access Short Form



Reprogramming

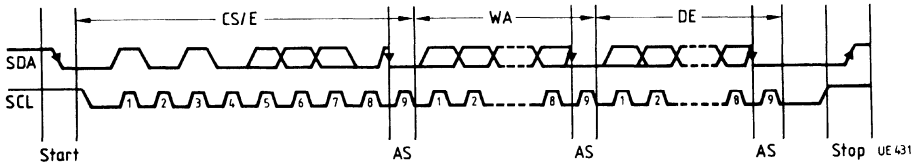
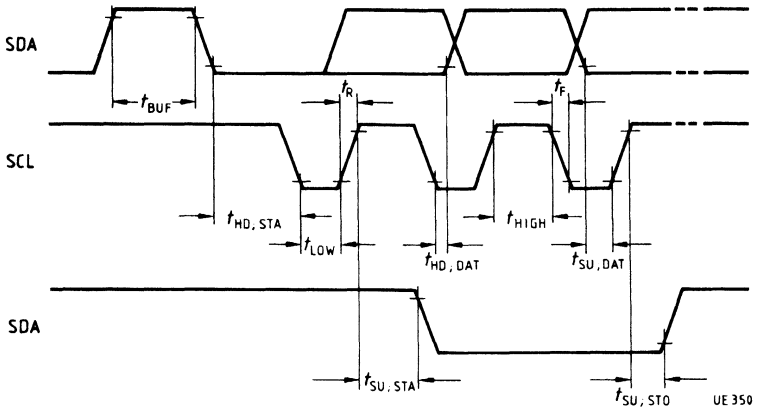


Figure 2

Timing Conditions for the I²C Bus (high-speed-mode)



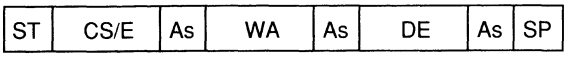
Parameter	Symbol	Limit Values		Unit
		min.	max	
Minimum time the bus must be free before a new transmission can start	t_{BUF}	4.7		µs
Start condition hold time	$t_{HD;STA}$	4.0		µs
Clock LOW period	t_{LOW}	4.7		µs
Clock HIGH period	t_{HIGH}	4.0		µs
Start condition set-up time, only valid for repeated start code	$t_{SU;STA}$	4.7		µs
Data set-up time	$t_{SU;DAT}$	250		ns
Rise time of both the SDA and SCL line	t_R		1	µs
Fall time of both the SDA and SCL line	t_F		300	ns
Stop condition set-up time	$t_{SU;STO}$	4.7		µs
Hold time data	$t_{HD;DAT}$	0*		

*Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

Figure 3

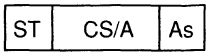
Programming

Control word input



(the reprogramming starts after this stop condition)

Check for program end



1. when As = 1 programming is not finished
2. when As = 0 programming is finished

Program interruption by

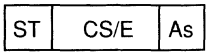
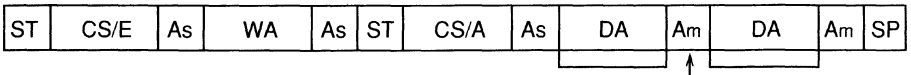


Figure 4

Read

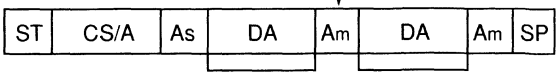
Control word input read
a) complete (with word address input)



n bytes Last byte

Automatic incrementation of the word address

b) shortened:
Bit 0 . . . 7 the last adapted word address keep unchanged



n bytes Last byte

Autoincrement Am = 0
before stop condition Am = 1

Control Word Table

Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	through memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	through memory
WA	A7	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0/1	through master

Control Word Input Key

CS/E	Chip select for data input into memory
CS/A	Chip select for data output out of memory
WA	Memory word address
DE	Data word for memory
DA	Data word read out of memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS0, CS1, CS2	Chip select bits
A0 to A7	Memory word address bits

SIEMENS

Nonvolatile Memory 4-Kbit E²PROM with I²C Bus

SDA 2546

Preliminary Data

MOS IC

Features

- Word-organized reprogrammable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 512 x 8 bit organization
- Supply voltage 5 V
- Serial 2-line bus for data input and output (I²C bus)
- Reprogramming mode, 10 ms erase / write cycle
- Reprogramming by means of on-chip control (without external control)
- The end of the programming cycle can be checked
- Data retention in excess of 10 years
- More than 10^4 reprogramming cycles per address

Type	Ordering Code	Package
SDA 2546	Q67100-H8616	P-DIP-8

Circuit Description

I²C Bus Interface

The I²C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a data line SDA and a clock line SCL. The data line requires an external pull-up resistor to V_{DD} (open drain output stages).

The possible operational states of the I²C bus are shown in **figure 1**. In the quiescent state, both lines SDA and SCL are high, i.e. the output states are disabled. As long as SCL remains "1", information changes on the data bus indicate the start or the end of a data transfer between two components. The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" a stop condition. During a data transfer the information on the data bus will only change when the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I²C bus system, the device can operate as a receiver, and as a transmitter (slave receiver / listener, or slave transmitter / talker). Between the trailing edge of the eighth transmission pulse and a ninth acknowledge clock pulse, the device sets the SDA line to low as a reception confirmation, if the chip select conditions have been met. During the output of data, the data output of the memory becomes high, during the ninth clock pulse (acknowledge master).

Control Functions of the I^2C Bus

The device is controlled by the controller (master) via I^2C bus in two operating modes: real cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes to the bus after the start condition. Each byte has to be followed by an acknowledge bit. During a memory read, at least eight additional clock pulses are required to accept the data from the memory, before the stop condition may follow. In the programming case, the active programming process is only started by the stop condition after data input.; **see figure 3.**

The chip select word includes the chip select bit CS. Thus is possible to parallel two memory devices. Chip select is obtained when the control bits logically correspond to the condition selected at the select input CS. The most significant bits A8 and A9 are inputs with the chip select words CS/E.

Checking the End of the Programming Cycle and Breaking off the Programming Cycle

Addressing the chip by the input of CS/E during active reprogramming terminates the programming cycle. If the chip is addressed by entering CS/A, this will be ignored. Only when the programming cycle has terminated will the chip react on CS/A. With this procedure the end of the programming cycle can be checked, **see figure 3**.

Memory Read

After the input of the two control words CS/E and WA, the resetting of the start condition and the input of a third control word CS/A, the memory is set ready to read. During acknowledge clock no. 9, the memory information is transferred in parallel to the internal data register. Subsequent to the trailing edge of the acknowledge clock, the data output is low-impedance and the first data bit can be sampled,**see figure 3.**

With each shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented through the master receiver acknowledge, so that any number of memory locations can be read one after the other. At address 512, an overflow to address 0 is not initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into "1" state. During the write process, "0" states are generated according to the information in the internal data register, i. e. according to the third input control word.

After the 27th and the last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control and can be terminated by addressing the device via SCL and SDA.

The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage the erase / write process is max 20 ms, or typically, 10 ms. For the input of a data word without write request (write request is defined as data bit in the data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

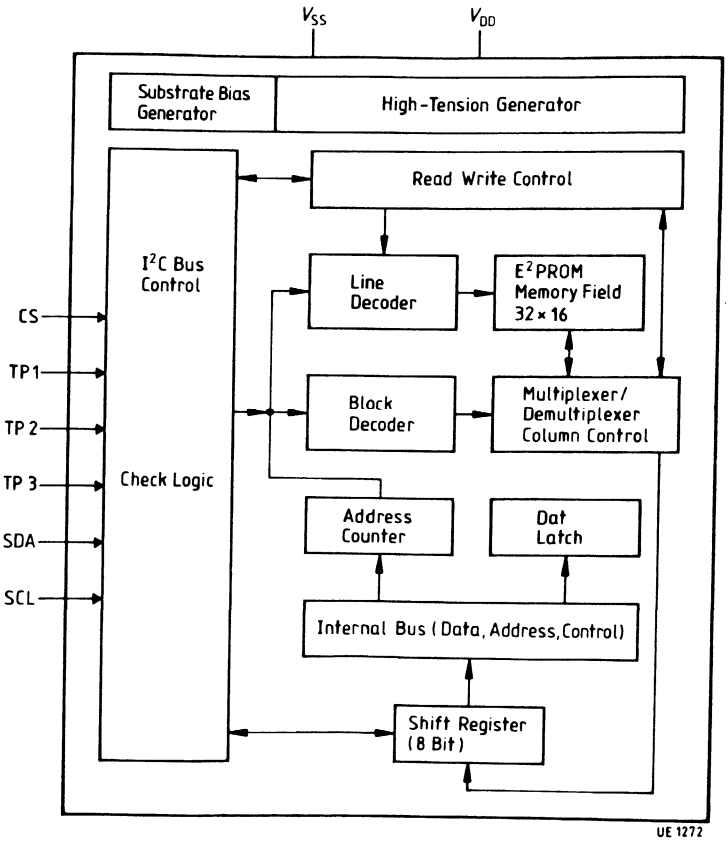
Switch-On and Chip Reset

After the supply voltage V_{DD} has been connected, the data output willbe in the high impedance mode. As a rule, the first operating mode to be entered should be the read process f of a word addressSubsequent to the data output and to the stop condition, the internal control logic is reset. In case of a subsequent active programming operation, however, the stop condition will not reset the control logic.

Chip Erase

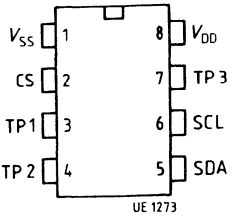
To erase the entire memory the control word CS/E is entered, the address register is loaded with address 0 and the data register with FF (hex), respectively. Immediately prior to generating the stop condition, the input TP2 is connected from 0 to 5 V. The subsequent stop condition initiates the chip erase. As soon as the erase procedure has terminated, TP2 is again connected to 0 V.

Block Diagram



Pin Configuration

(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{SS}	Ground
2	CS	Chip select
3	TP1	to V_{SS}
4	TP2	0 V normal function, TP2 = 5 V condition for the erase of the complete memory
5	SDA	Data line
6	SCL	Clock line
7	TP3	open
8	V_{DD}	Supply voltage

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage range	V_{DD}	– 0.3	6	V
Input voltage range	V_I	– 0.3	6	V
Power dissipation	P_D		130	mW
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		100	K/W
Junction temperature	T_j		85	°C

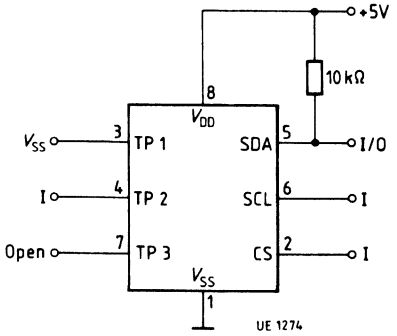
Operating Range

Supply voltage	V_{DD}	4.75	5.25	V
Ambient temperature	T_A	0	70	°C

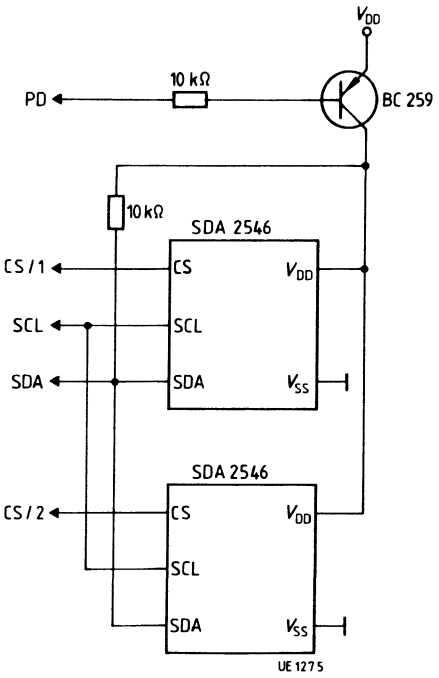
Characteristics
$T_A = 25\ ^\circ C$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{DD}	4.75	5.0	5.25	V	
Supply current	I_{DD}			20	mA	$V_{DD} = 5.25$ V
Inputs						
Input voltages SDA/SCL	V_{IL}			1.5	V	
Input voltages SDA/SCL	V_{IH}	3.0		V_{DD}	V	
Input currents SDA/SCL	I_{IH}			10	µA	$V_{IH} = V_{DD}$
Outputs						
Output current SDA	I_{QL}			3.0	mA	$V_{QL} = 0.4$ V
Leakage current SDA	I_{QH}			10	µA	$V_{QH} = V_{DD\,max}$
Inputs						
Input voltages CS/TP 1/TP 2	V_{IL}			0.2	V	
Input voltages CS/TP1/TP2	V_{IH}	4.5		V_{DD}	V	
Input currents CS/TP1/TP2	I_{IH}			100	µA	$V_{DD} = 5.25$ V
Clock frequency	f_{SCL}			100	kHz	
Reprogramming duration	t_{PROG}		10	20	ms	erase and write
Input capacity	C_I			10	pF	
Chip erase duration	t_{er}			20	ms	TP 2 = 5 V

Test Circuit



Application Circuit



Diagrams

Figure 1

Operational States of the I²C Bus

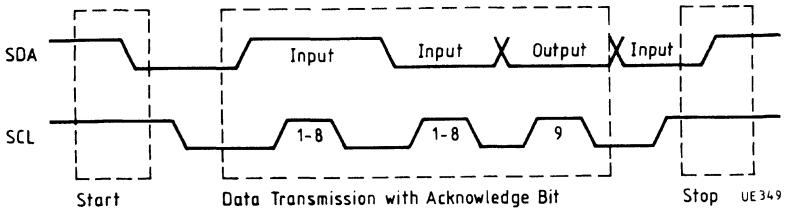
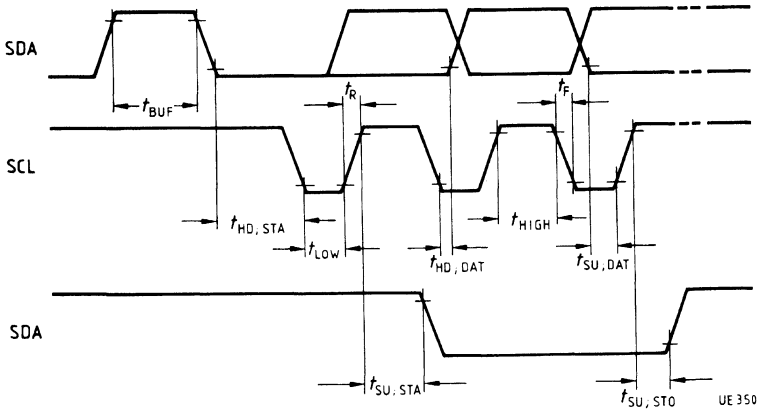


Figure 2

Timing Conditions for the I²C Bus (high-speed mode)



Timing Conditions

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Minimum time the bus must be free before a new transmission can start	t_{BUF}	4.7		µs
Start condition hold time	$t_{HD;STA}$	4.0		µs
Clock LOW period	t_{LOW}	4.7		µs
Clock HIGH period	t_{HIGH}	4.0		µs
Start condition set-up time, only valid for repeated start code	$t_{SU;STA}$	4.7		µs
Data set-up time	$t_{SU;DAT}$	250		ns
Rise time of both the SDA and SCL line	t_R		1	µs
Fall time of both the SDA and SCL line	t_F		300	ns
Stop condition set-up time	$t_{SU;TPO}$	4.7		µs

Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL. All values refer to V_{IH} and V_{IL} level.

Figure 3

Programming

Control word input

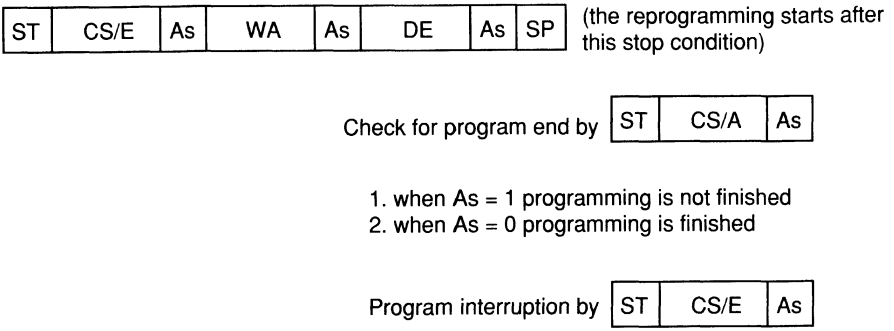
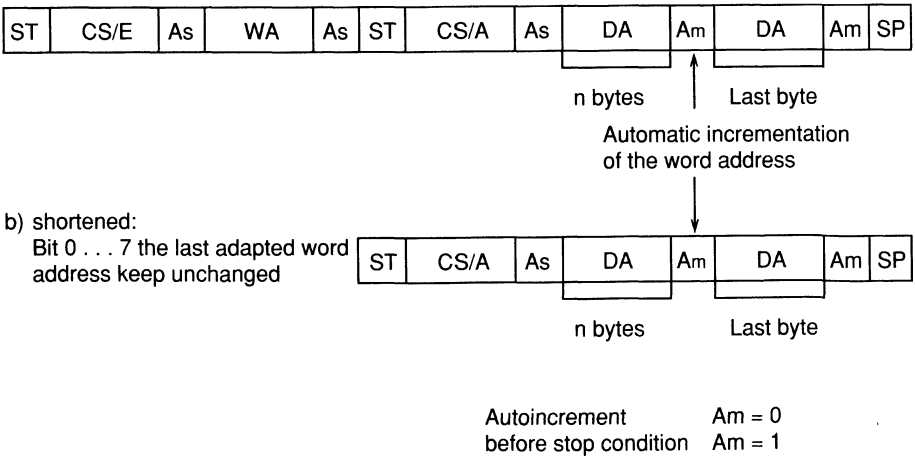


Figure 4

Read

Control word input read
a) complete (with word address input)



Control Word Table

Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	0	A8	CS	0	0	through memory
CS/A	1	0	1	0	–	–	CS	1	0	through memory
WA	A7	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0/1	through master

Control Word Input Key

CS/E	Chip select for data input memory (with the word-address-bit A8)
CS/A	Chip select for data output of memory
WA	Memory word address
DE	Data word for memory
DA	Data word read out of memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS	Chip select bits
A0 to A8	Memory word address bits

SIEMENS

Nonvolatile Memory 8-Kbit E²PROM with I²C Bus

SDA 2586

Preliminary Data

MOS IC

Features

- Word-organized reprogrammable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 1024 x 8 bit organization
- Supply voltage 5 V
- Serial 2-line bus for data input and output (I²C bus)
- Reprogramming mode, 10 ms erase / write cycle
- Reprogramming by means of on-chip control (without external control)
- The end of the programming cycle can be checked
- Data retention in excess of 10 years
- More than 10^4 reprogramming cycles per address

Type	Ordering Code	Package
SDA 2586	Q67100-H8617	P-DIP-8

Circuit Description

I²C Bus Interface

The I²C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a data line SDA and a clock line SCL. The data line require an external pull-up resistor to V_{DD} (open drain output stages).

The possible operational states of the I²C bus are shown in **figure 1**. In the quiescent state, both lines SDA and SCL are high, i.e. the output stages are disabled. As long as SCL remains "1", information changes on the data bus indicate the start or the end of a data transfer between two components. The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" a stop condition. During a data transfer, the information on the data bus will only change when the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I²C bus system, the device can operate as a receiver, and as a transmitter (slave receiver / listener, or slave transmitter / talker). Between a start and a stop condition, the information is always transmitted in byte-organized form. Between the trailing edge of the eighth transmission pulse and a ninth acknowledge clock pulse, the device sets the SDA line to low as a reception confirmation, if the chip select conditions have been met. During the output of data, the data output of the memory becomes high in impedance during the ninth clock pulse (acknowledge master).

The signal timing required for the operation of the I²C bus is summarized in **figure 2**.

Control Functions of the I²C Bus

The device is controlled by the controller (master) via the I²C bus in two operating modes: read cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes to the bus after the start condition. Each byte has to be followed by an acknowledge bit. During a memory read, at least eight additional clock pulses are required to accept the data from the memory, before the stop condition may follow. In the programming instance, the active programming process is only started by the stop condition after data input; **see figure 3**.

The chip select word includes the chip select bit CS. Thus it is possible to parallel two memory devices. Chip select is obtained when the control bits logically correspond to the condition selected at the select input CS. The two most significant bits A8 and A9 are inputs with the chip select words CS/E.

Checking the End of the Programming Cycle and Breaking off the Programming Cycle

Addressing the chip by the input of CS/E during active reprogramming terminates the programming cycle. If the chip is addressed by entering CS/A, this will be ignored. Only when the programming cycle has terminated will the chip react on CS/A. With this procedure the end of the programming cycle can be checked, **see figure 3**.

Memory Read

After the input of the two control words CS/E and WA, the resetting of the start condition and the input of a third control word CS/A, the memory is set ready to read. During acknowledge clock No. 9, the memory information is transferred in parallel to the internal data register. Subsequent to the trailing edge of the acknowledge clock the data output is low-impedance and the first data bit can be sampled, **see figure 4**. With each shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented through the master receiver acknowledge, so that any number of memory locations can be read one after the other. At address 1024, an overflow to address 0 is initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into "1" state. During the write process, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word.
After the 27th and the last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control and can be terminated by addressing the device via SCL and SDA.
The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage the erase / write process is max. 20 ms, or typically, 10 ms. For the input of a data word without write request (write request is defined as data bit in the data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

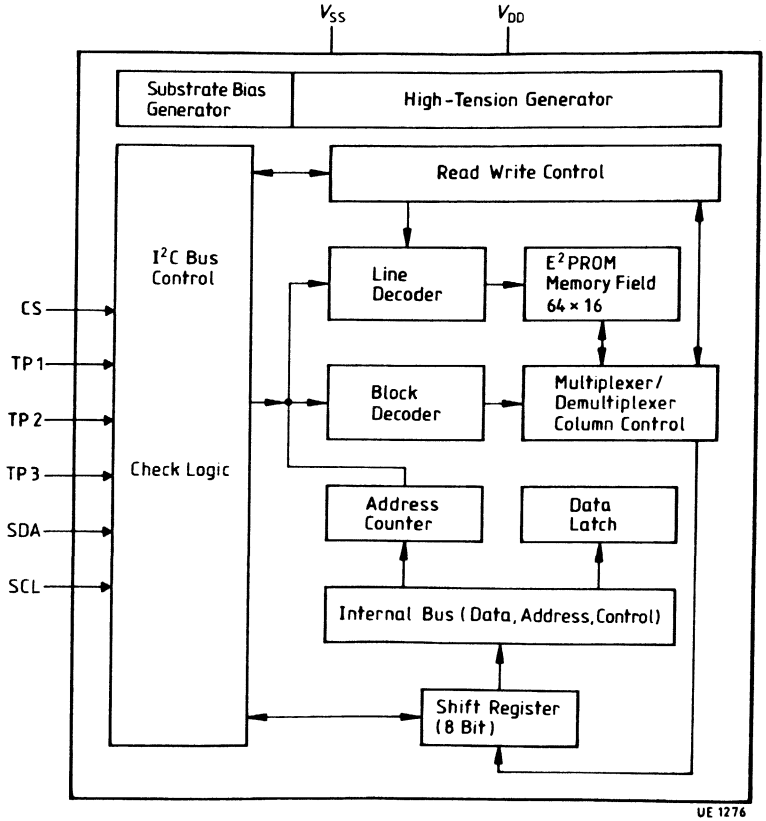
Switch-On and Chip Reset

After the supply voltage V_{DD} has been connected, the data output will be in the high impedance mode. As a rule, the first operating mode to be entered should be the read process of a word address. Subsequent to the data output and to the stop condition, the internal control logic is reset. In the case of a subsequent active programming operation, however, the stop condition will not reset the control logic.

Chip Erase

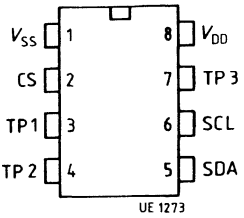
To erase the entire memory the control word CS/E is entered, the address register is loaded with address 0 and the data register with FF (hex), respectively. Immediately prior to generating the stop condition, the input TP2 is connected from 0 to 5 V. The subsequent stop condition initiates the chip erase. As soon as the erase procedure has terminated, TP2 is again connected to 0 V.

Block Diagram



Pin Configuration

(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{SS}	Ground
2	CS	Chip select
3	TP1	to V_{SS}
4	TP2	0 V normal function, TP2 = 5 V condition to erase of the entire memory
5	SDA	Data line
6	SCL	Clock line
7	TP3	open
8	V_{DD}	Supply voltage

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage range	V_{DD}	– 0.3	6	V
Input voltage range	V_i	– 0.3	6	V
Power dissipation	P_D		130	mW
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system air)	R_{thSA}		100	K/W
Junction temperature	T_j		85	°C

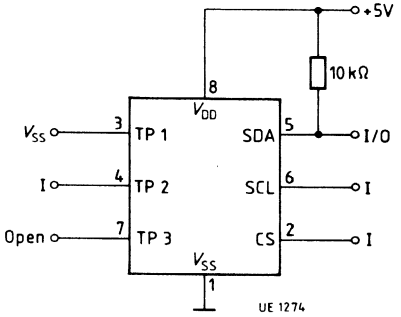
Operating Range

Supply voltage	V_{DD}	4.75	5.25	V
Ambient temperature	T_A	0	70	°C

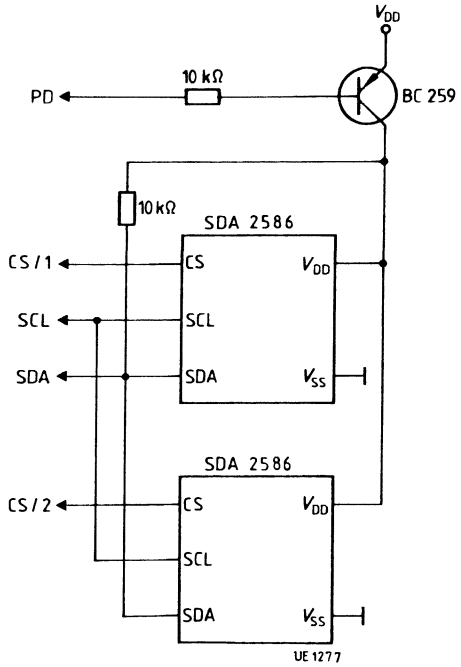
Characteristics
$T_A = 25\ ^\circ C$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{DD}	4.75	5.0	5.25	V	
Supply current	I_{DD}			20	mA	$V_{DD} = 5.25$ V
Inputs						
Input voltages SDA/SCL	V_{IL}			1.5	V	
Input voltages SDA/SCL	V_{IH}	3.0		V_{DD}	V	
Input currents SDA/SCL	I_{IH}			10	µA	$V_{IH} = V_{DD}$
Outputs						
Output current SDA	I_{QL}			3.0	mA	$V_{QL} = 0.4$ V
Leakage current SDA	I_{QH}			10	µA	$V_{QH} = V_{DD\,max}$
Inputs						
Input voltages CS/TP 1/TP 2	V_{IL}			0.2	V	
Input voltages CS/TP1/TP2	V_{IH}	4.5		V_{DD}	V	
Input currents CS/TP1/TP2	I_{IH}			100	µA	$V_{DD} = 5.25$ V
Clock frequency	f_{SCL}			100	kHz	
Reprogramming duration	t_{PROG}		10	20	ms	erase and write
Input capacity	C_I			10	pF	
Chip erase duration	t_{er}			20	ms	TP 2 = 5 V

Test Circuit



Application Circuit



Diagrams

Figure 1
Operational States of the I²C Bus

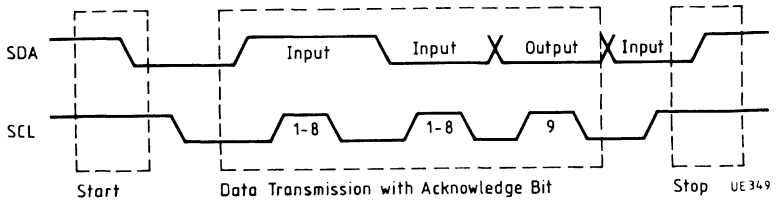
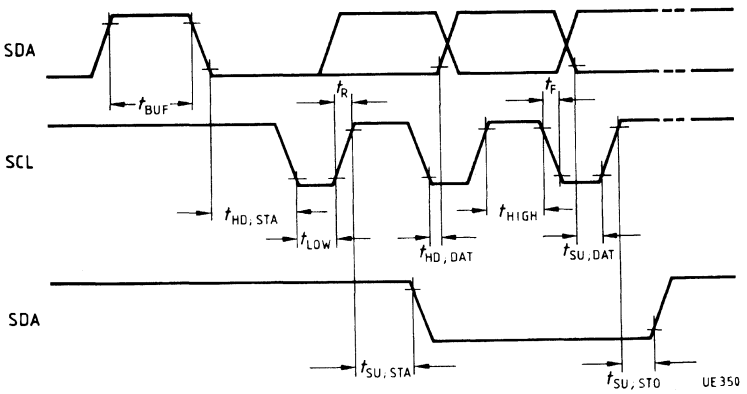


Figure 2
Timing Conditions for the I²C Bus (high-speed mode)



Timing Conditions

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Minimum time the bus must be free before a new transmission can start	t_{BUF}	4.7		µS
Start condition hold time	$t_{HD;STA}$	4.0		µS
Clock LOW period	t_{LOW}	4.7		µS
Clock HIGH period	t_{HIGH}	4.0		µS
Start condition set-up time, only valid for repeated start code	$t_{SU;STA}$	4.7		µS
Data set-up time	$t_{SU;DAT}$	250		nS
Rise time of both the SDA and SCL line	t_R		1	µS
Fall time of both the SDA and SCL line	t_F		300	µS
Stop condition set-up time	$t_{SU;TPO}$	4.7		µS

Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

All values refer to V_{IH} and V_{IL} level.

Figure 3

Programming

Control word input

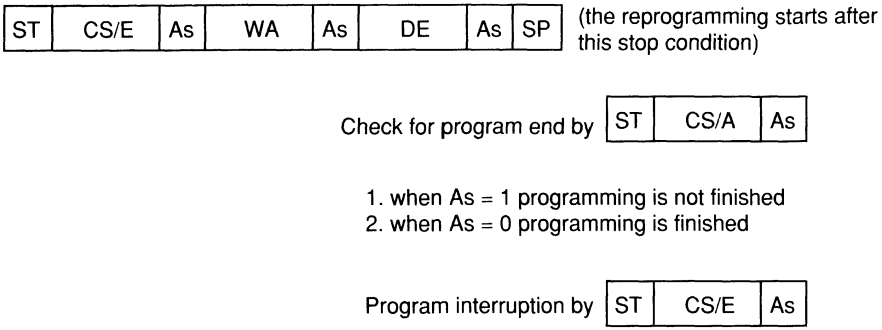
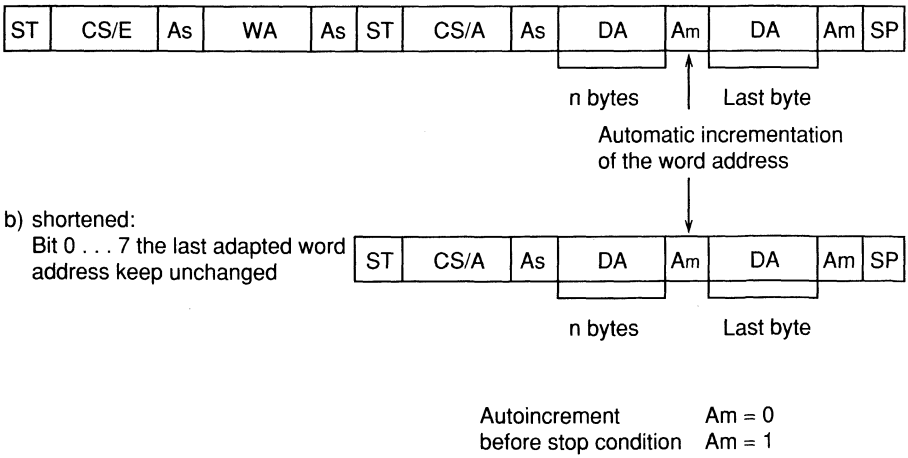


Figure 4

Read

Control word input read
a) complete (with word address input)



Control Word Table

Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	A9	A8	CS	0	0	through memory
CS/A	1	0	1	0	–	–	CS	1	0	through memory
WA	A7	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0/1	through master

Control Word Input Key

CS/E	Chip select for data input memory (with word-adress bit A8 and A9)
CS/A	Chip select for data output of memory
WA	Memory word address
DE	Data word for memory
DA	Data word read out for memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS	Chip select bits
A0 to A9	Memory word address bits

SIEMENS

GHz PLL with I²C Bus and Four Chip Addresses

SDA 3302

Preliminary Data

Bipolar IC

Features

- 1 chip system for MPU control (I²C bus)
- 4 programmable chip addresses
- Short rise time for fast channel switch operations and improved loop stability
- Charge pump output with switch off option
- Software compatible with SDA 3202 series
- 3 high current band switch outputs (20 mA)
- 4 high current port buffers
- Oxis III technology

Type	Ordering Code	Package
SDA 3302-2	Q67000-A5027	P-DIP-18
SDA 3302-X	Q67000-H5023	P-DSO-20
SDA 3302-X6	Q67000-H5018	P-DSO-16
SDA 3302-4	Q67000-A5040	P-DSO-14

Together with a VCO (tuner) the SDA 3302 device, with four hardware-switched chip addresses, forms a digitally programmable phase-locked loop for use in television sets with PLL frequency-synthesis tuning.

The PLL permits crystal-controlled setting of the frequency of the tuner oscillators between 16 and 1300 MHz in increments of 62.5 kHz, and in increments of 125 kHz in the TV-Sat band with a 2.4-GHz prescaler 1/2. The tuning process is controlled by a microprocessor on an I²C bus. The new oscillator contains a sinusoidal signal which reduces the moiré noise considerably.

Operating voltage V_S = 5 V

Circuit Description

Tuning Section (refer to block diagram)

UHF/VHF
REF

The tuner signal is coupled in capacitively on the UHF/VHF input and amplified. The reference input REF should be blocked to ground using a capacitor of low series inductance. The signal is then applied to and an asynchronous divider with a fixed ratio of P = 8, and an adjustable divider N = 256 through 32767 and then compared in a digital phase/frequency detector to a reference frequency f_{REF} of 7.8125 kHz. The latter is derived from a balanced, low-impedance 4-MHz crystal oscillator (pin Q1, Q2),

Q1, Q2

whose output signal is divided by Q = 512.

PD, UD

The phase detector has two outputs UP and DOWN that drive the two current sources $I+$ and $I-$ of a charge pump. If the negative edge of the divided VCO signal appears before the negative edge of the reference signal, the $I+$ current source pulsates for the duration of the phase difference. In the reverse case the $I-$ current source pulsates. When the two signals are in phase, the charge-pump output (PD) goes high-impedance (PLL is locked). The current pulses are integrated to form a tuning voltage for the VCO by an active lowpass filter (internal amplifier an external transistor at the UD output and an external RC circuitry). The charge-pump output can also be sent high-impedance when control bit TO = 1. Here it should be noted, however, that the tuning voltage can alter over a longish period in the high-impedance state as a result of self-discharge in the peripheral circuitry. The GUT can be disconnected internally by the control bit OS to enable external adjustments.

By means of a control bit 5I the pump current can be switched between two values by software. This switchover permits alteration of the control response of the PLL in a locked-in state. In this way different tuner responses in the different TV bands can be compensated for example.

P0-P2

The software-switched outputs (P0, P1, P2) can be used for direct band selection (20-mA current output).

P4-P7

P4, P5, P6 and P7 are open-collector outputs for a variety of different purposes. The test bit T1 = 1 switches the test signals f_{REF} (4 MHz/512) and Cy (divided input signal) to P6 and P7.

CAU

Four different chip addresses can be set by appropriate wiring of pin CAU.

Circuit Description (cont 'd)

I²C Bus Interface

SCL, SDA

Data are exchanged between the processor and the PLL on the I²C bus. The timing is produced by the processor (input SCL), while pin SDA works as an input or output depending on the direction of the data (open collector; external pullup resistor). Both inputs have hysteresis and a lowpass characteristic, which enhances the noise immunity of the I²C bus.

The data from the processor are applied to an I²C bus controller and filed in registers according to their function. When the bus is free, both lines are in the marking state (SDA, SCL are high). Each telegram begins with a start condition and ends with the stop condition. Start condition: SDA goes low while SCL remains high; stop condition: SDA goes high while SCL remains high. All further data exchanges occur while SCL is low and are accepted by the controller with the positive clock edge.

For what follows, refer to the table of logic allocations.

All telegrams are transmitted byte by byte, followed by a ninth clock pulse, during which the controller puts the SDA line on low (acknowledge condition). The first byte consists of seven address bits, with which the processor selects the PLL from a number of peripheral devices (chip select). The eighth bit is always low. In the data portion of the telegram the first bit of the first or third data byte determines whether a divider ratio or control information follows. In each case the byte following the first byte must be of the same data type (or a stop condition).

V_S, GND

When the supply voltage is applied, a power-on reset circuit prevents the PLL from putting the SDA line on low, which would block the bus.

Circuit Description (cont 'd)

Logic Allocations

	MSB								A = acknowledge
Address byte	1	1	0	0	0	MA1	MA0	0	A
Progr. divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Progr. divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control info. byte 1	1	5I	T1	T0	1	1	1	OS	A
Control info. byte 2	P7	P6	P5	P4	X	P2	P1	P0	A

Divider Ratio:

$N = 16384 \times n14 + 8192 \times n13 + 4096 \times n12 + 2048 + n11 + 1024 \times n10 + 512 \times n9 + 256 \times n8 + 128 \times n7 + 64 \times n6 + 32 \times n5 + 16 \times n4 + 8 \times n3 + 4 \times n2 + 2 \times n1 + n0$

Band Selection:

P2-P0 = 1 open-collector output is active

Port Outputs:

P7-P4 = 1 open-collector output is active

Pump-Current Switchover:

5I = 1 high current

VD-Disconnection:

OS = 1 V_D is disabled

Test Mode:

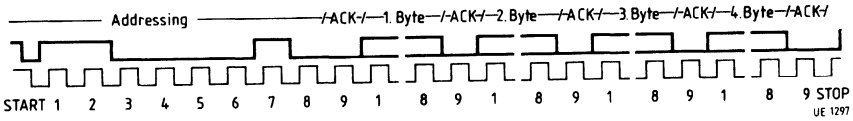
T1, T0 = 0,0 normal mode
T1 = 1 P6 = f_{REF}, P7 = Cy
T0 = 1 tristate charge pump is high-impedance

Circuit Description (cont 'd)

Chip-Address Switching

MA1	MA0	Voltage on CAU
0	0	(0-0.1)V_S
0	1	open
1	0	(0.4-0.6)V_S
1	1	(0.9-1)V_S

Pulse Diagram

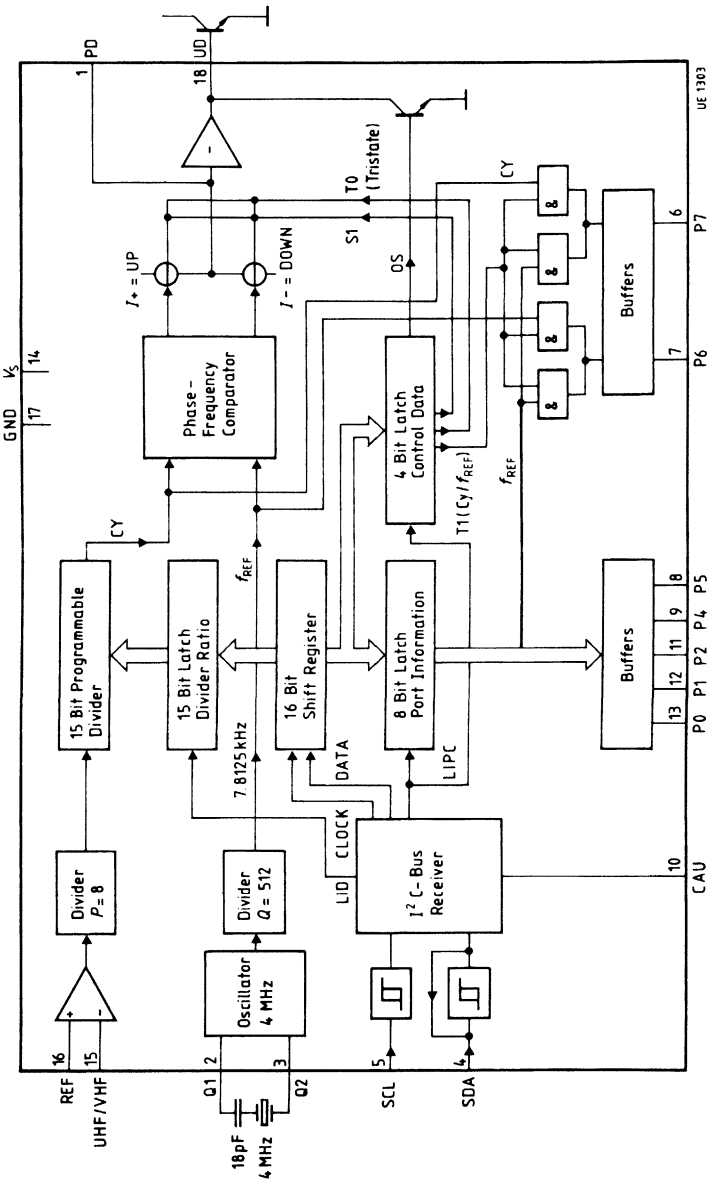


Telegram Examples

Start-Addr-Dr1-Dr2-Cw1-Cw2-Stop
Start-Addr-Cw1-Cw2-Dr1-Dr2-Stop
Start-Addr-Dr1-Dr2-Cw1-Stop
Start-Addr-Cw1-Cw2-Dr1-Stop
Start-Addr-Dr1-Dr2-Stop
Start-Addr-Cw1-Cw2-Stop
Start-Addr-Dr1-Stop

Start = start condition
Addr = addressing
Dr1 = divider ratio 1st byte
Dr2 = divider ratio 2nd byte
Cw1 = control word 1st byte
Cw2 = control word 2nd byte
Stop = stop condition

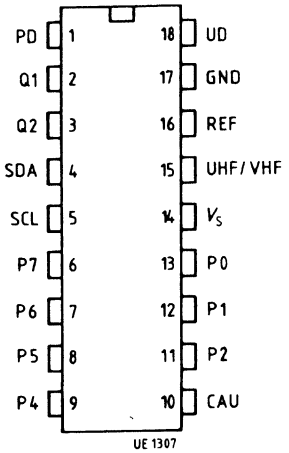
Block Diagram



Pin Configuration
(top view)

P-DIP-18

SDA 3302



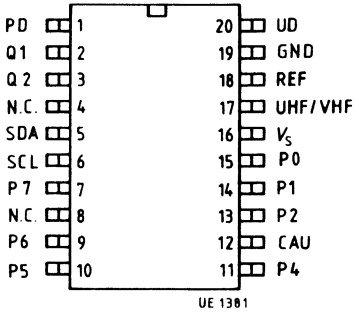
Pin Definitions and Functions

Pin No.	Symbol	Function
1	PD	Active-filter input/charge-pump output
2	Q1	Crystal
3	Q2	Crystal
4	SDA	Data input/output for I^2C bus
5	SCL	Clock input for I^2C bus
6	P7	Port output (open collector)
7	P6	Port output (open collector)
8	P5	Port output (open collector)
9	P4	Port output (open collector)
10	CAU	Chip-address switchover
11	P2	Port output (open collector)
12	P1	Port output (open collector)
13	P0	Port output (open collector)
14	V_S	Supply voltage
15	UHF/VHF	Signal input
16	REF	Amplifier reference input
17	GND	Ground
18	UD	Output active filter

Pin Configuration
(top view)

P-DSO-20

SDA 3302-X



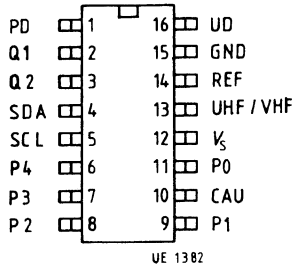
Pin Definitions and Functions

Pin No.	Symbol	Function
1	PD	Active-filter input/charge-pump output
2	Q1	Crystal
3	Q2	Crystal
4	N.C.	Not connected
5	SDA	Data input/output for I^2C bus
6	SCL	Clock input for I^2C bus
7	P7	Port output (open collector)
8	N.C.	Not connected
9	P6	Port output (open collector)
10	P5	Port output (open collector)
11	P4	Port output (open collector)
12	CAU	Chip-address switchover
13	P2	Port output (open collector)
14	P1	Port output (open collector)
15	P0	Port output (open collector)
16	V_S	Supply voltage
17	UHF/VHF	Signal input
18	REF	Amplifier reference input
19	GND	Ground
20	UD	Active-filter output

Pin Configuration
(top view)

P-DSO-16

SDA 3302-X6



Pin Definitions and Functions

Pin No.	Symbol	Function
1	PD	Active-filter input/output-pump output
2	Q1	Crystal
3	Q2	Crystal
4	SDA	Data input/output for I^2C bus
5	SCL	Clock input for I^2C bus
6	P4	Port output (open collector)
7	P3	Port output (open collector)
8	P2	Port output (open collector)
9	P1	Port output (open collector)
10	CAU	Chip-address switchover
11	P0	Port output (open collector)
12	V_S	Supply voltage
13	UHF/VHF	Signal input
14	REF	Amplifier reference input
15	GND	Ground
16	UD	Output active filter

Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.3	6	V	
Output PD	V_1	– 0.3	V_S	V	
Crystal Q1	V_2	– 0.3	V_S	V	
Crystal Q2	V_3	– 0.3	V_S	V	
Bus input/output SDA	V_4	– 0.3	6	V	
Bus input SCL	V_5	– 0.3	6	V	
Port output P7	V_6	– 0.3	16	V	
Port output P6	V_7	– 0.3	16	V	
Port output P5	V_8	– 0.3	16	V	
Port output P4	V_9	– 0.3	16	V	
Chip-address switchover	V_{10}	– 0.3	V_S	V	
Port output P2	V_{11}	– 0.3	16	V	open collector
Port output P1	V_{12}	– 0.3	16	V	open collector
Port output P0	V_{13}	– 0.3	16	V	open collector
Signal input UHF/VHF	V_{15}	– 0.3	0.3	V	for V_S = 0 V
Reference input REF	V_{16}	– 0.3	0.3	V	for V_S = 0 V
Output active filter UD	V_{18}	– 0.3	V_S	V	
Bus output SDA	I_{4L}	– 1	5	mA	open collector
Port output P6	I_{7L}	– 1	20	mA	open collector
Port output P5	I_{8L}	– 1	20	mA	open collector
Port output P4	I_{9L}	– 1	20	mA	open collector
Port output P2	I_{11L}	– 1	20	mA	open collector
Port output P1	I_{12L}	– 1	20	mA	open collector
Port output P0	I_{13L}	– 1	20	mA	open collector
Chip temperature	T_C		125	°C	
Storage temperature	T_{stg}	– 40	125	°C	
Thermal resistance (system-air)	$R_{th\,SA}$		80	K/W	

Operating Range

Supply voltage	V_S	4.5	5.5	V	
Ambient temperature	T_A	– 20	80	°C	
Input frequency	f_{15}	16	1300	MHz	at 25 °C
Crystal frequency	$f_{2,3}$		4	MHz	
Programmable divider factor	N	256	32767		

Characteristics

V_S = 5 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Current consumption	I_S		35		mA	V_S = 5 V	1
Crystal-oscillator frequency	$f_{2,3}$	3.99975	4.000	4.00025	MHz	series capacitance 18 pF; f_{xtal} = 4 MHz	1
Oscillator level*	$V_{2,3}$		800		mV_{pp}		
Margin from 1st* and 2nd harmonic			20		dB		

Input Sensitivity UHF/VHF* in mV_{rms} at 50 Ω

	a_{15}	– 27/10		3/315	dBm/*	f_{15} = 70-500 MHz	2
	a_{15}	– 27/10		3/315	dBm/*	f_{15} = 1000 MHz	2
	a_{15}	– 20/22		3/315	dBm/*	f_{15} = 1100 MHz	2

Band-Select Outputs P0-P2 (switch with open collector)

Reverse current	I_{13H}			10	µA	V_{13H} = 13.5 V	3
Residual voltage	V_{13L}			0.5	V	I_{13L} = 20 mA	3

Port Outputs P4-P7 (switch with open collector)

Reverse current	I_{9H}			10	µA	V_{9H} = 13.5 V	4
Residual voltage	V_{9L}			0.5	V	I_{9L} = 1.7 mA	4

Phase-Detector Output PD (V_S = 5 V)

Pump current	I_{1H}	± 90	± 220	± 300	µA	5I = HIGH; V_1 = 2 V	
Pump current	I_{1H}	± 22	± 50	± 75	µA	5I = LOW; V_1 = 2 V	
Output voltage	V_{1L}	1.0		2.5	V	locked	

Output Active Filter UD (T0 = 1)

Output current	$-I_{18}$	500			µA	V_{18} = 0.8 V; I_{IH} = 90 µA	
Output voltage	V_{18}			100	mV	V_{1L} = 0 V	
Output voltage	V_{18}			500	mV	O_S = 1	

Chip-Address Switchover

Input current	I_{1OH}			50	µA	V_{1OH} = 5 V	5
Input current	$-I_{1OH}$			50	µA	V_{1OH} = 0 V	5

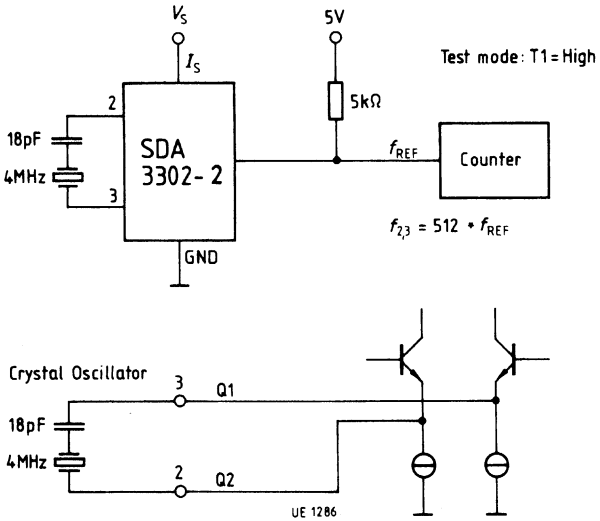
*Design note: no 100% final inspection

Characteristics (cont 'd)
V_S = 5 V; T_A = 25 °C

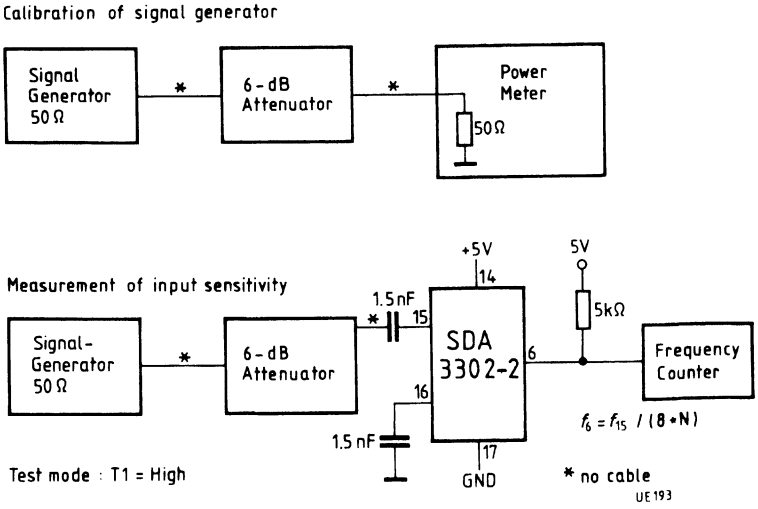
Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions	Test Circuit
Bus Inputs SCL, SDA							
Input voltage	V_{5H} V_{5L}	3		5.5 1.5	V V		6 6
Input current	I_{5H}			10	µA	$V_{5H} = V_S$	6
Input current	$-I_{5L}$			20	µA	V_{5L} = 0 V	6
Output SDA (open collector)							
Reverse current	I_{4H}			10	µA	V_{4H} = 5.5 V	6
Output voltage	V_{4L}			0.4	V	I_{4L} = 3 mA	6
Edges SCL, SDA							
Rise time	t_R			1	µs		6
Fall time	t_F			0.3	µs		6
Shift Clock SCL							
Frequency	f_5	0		100	kHz		6
H-pulse width	t_{5H}	4			µs		6
L-pulse width	t_{5L}	4.7			µs		6
Start							
Setup time	t_{SUSta}	4.7			µs		6
Hold time	t_{HDSta}	4			µs		6
Stop							
Setup time	t_{SUSto}	4.7			µs		6
Bus free	t_{BUF}	4.7			µs		6
Data Exchange							
Setup time	t_{SUDat}	0.25			µs		6
Hold time	t_{HDDat}	0			µs		6
Input hysteresis* SCL, SDA			300		mV		
Lowpass cutoff* frequency SCL, SDA			500		kHz		

*Design note: no 100% final inspection

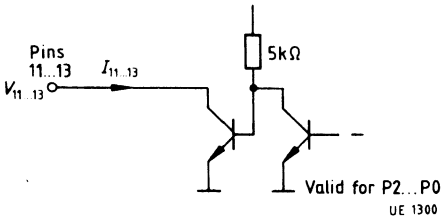
Test Circuit 1



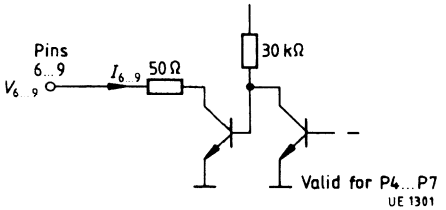
Test Circuit 2



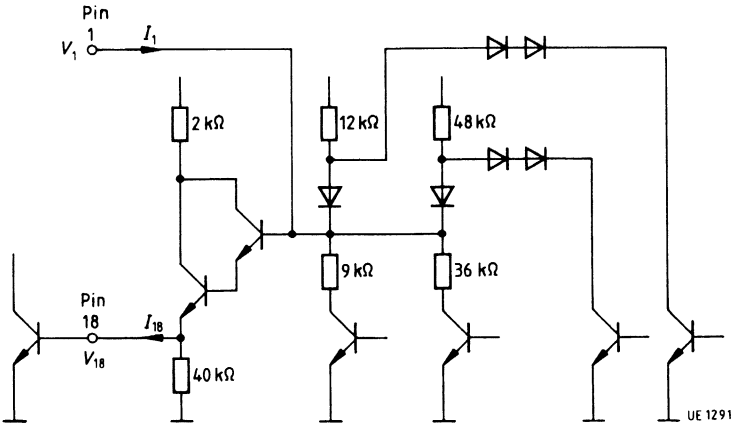
Test Circuit 3



Test Circuit 4

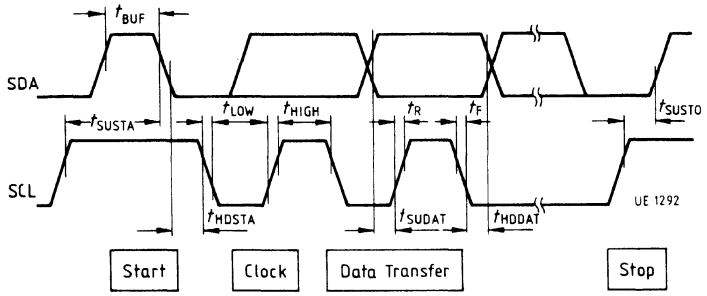


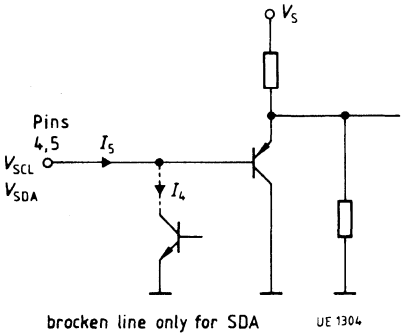
Test Circuit 5



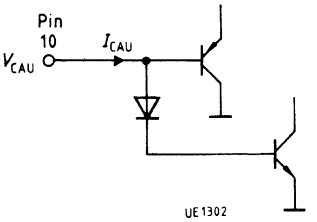
Test Circuit 6

I²C Bus Timing Diagram

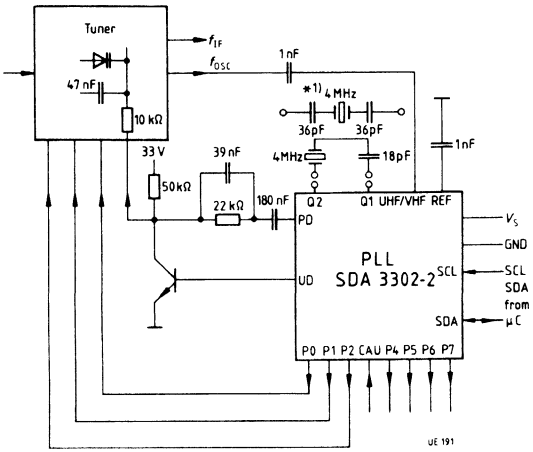




Test Circuit 7

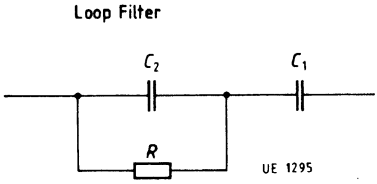


Application Circuit



*) This configuration of the load capacitances improves the balance of this crystal oscillator and thus reduces crosstalk

Application Circuit



Calculation of loop filter

Loop bandwidth: $\omega_R = \sqrt{(I_p \times K_{vco}) / (C_1 \times P \times N)}$

Attenuation: $\xi = 0.5 \times \omega_R \times R \times C_1$

P = prescaler
N = programmable divider
I_p = pump current
K_{vco} = tuner slope
R, C_1 = loop filter

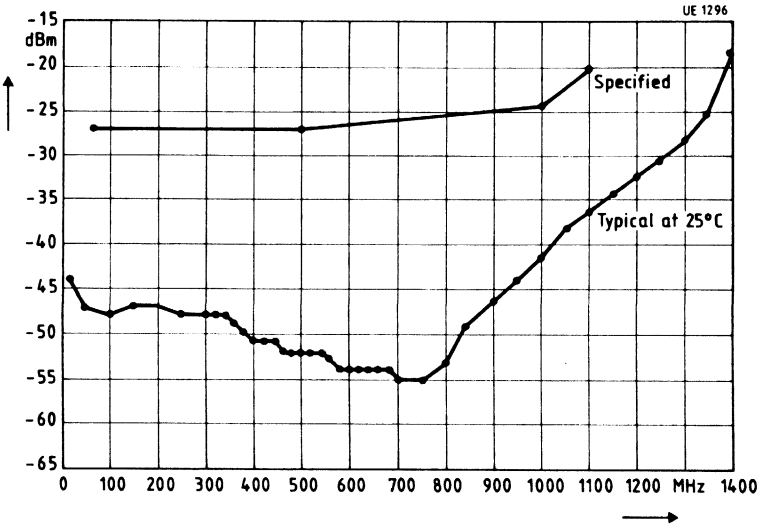
Example for channel 47:

P = 8, N = 11520, I_p = 100 µA; K_{vco} = 18.7 MHz/V, R = 22 kΩ,
C_1 = 180 nF; ω_R = 336 Hz, f_r = 54 Hz, ξ = 0.67

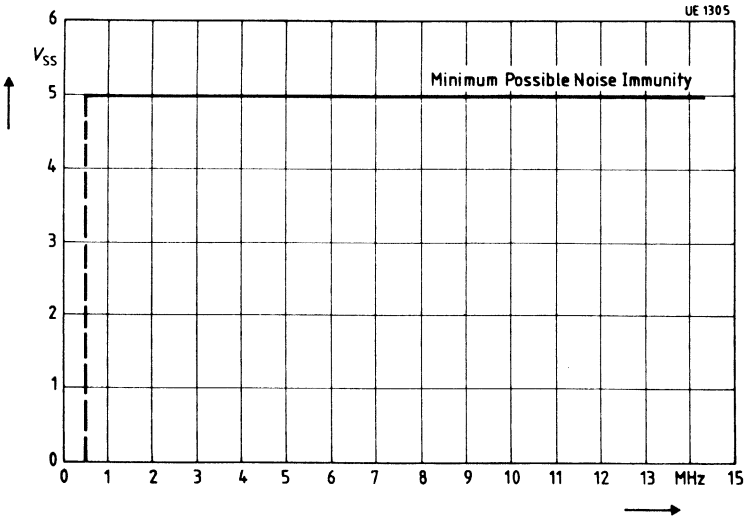
Standard dimensioning: $C_2 = C_{1/5}$

Note: The high-impedance port outputs and CAU can be blocked against external noise with a capacitor of 1 nF.

Input Sensitivity of SDA 3302



I^2C Bus Noise Immunity of SDA 3302



The sinusoidal noise pulses are applied via a coupling capacitance of 33 pF to SCL and SDA inputs.

SIEMENS

Nonvolatile Memory 2-Kbit E²PROM with I²C Bus and 1 K Write Protection

SDA 3526-1

Preliminary Data

MOS IC

Features

- Word-organized programmable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 256 x 8 bit organization
- Supply voltage 5 V
- Serial 2-line bus for data input and output (I²C bus)
- Reprogramming mode, 10 ms erase / write cycle
- Reprogramming by means of on-chip control (without external control)
- Check for end of programming process
- Programming disabled for adresses 128 . . . 255 (write protection mode)
- Data retention > 10 years
- More than 10^4 reprogramming cycles per address

Type	Ordering Code	Package
SDA 3526-1	Q67100-H5013	P-DIP-8

Circuit Description

I²C Bus Interface

The I²C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a serial data line SDA and a serial clock line SCL. The data line requires an external pull-up resistor to V_{DD} (open drain output stage).

The possible operational states of the I²C bus are shown in **figure 1**. In the quiescent state, both lines SDA and SCL are high, i. e. the output stage of the data line is disabled. As long as SCL remains "1", information changes on the data bus indicate the start or the end of data transfer between two components.

The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" is a stop condition. During a data transfer the information on the data bus will only change while the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I²C bus system, the memory component can operate as a receiver and as a transmitter (slave receiver or slave transmitter). Between a start and stop condition, information is always transmitted in byte-organized form. Between the trailing edge of the eighth clock pulse and a ninth acknowledge clock pulse, the memory component sets the SDA line to low as a confirmation of reception, if the chip select conditions have been met. During the output of data, the data output of the memory is high in impedance during the ninth clock pulse (acknowledge master).

The signal timing required for the operation of the I²C bus is summarized in **figure 2**.

Control Functions of the I²C Bus

The memory component is controlled by the controller (master) via the I²C bus in two operating modes: read-out cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes and an additional acknowledge clock pulse to the bus after the start condition. During a memory read, at least nine additional clock pulses are required to accept the data from the memory and the acknowledge master, before the stop condition may follow. In the case of programming, the active programming process is only started by the stop condition after data input (**see figure 3**).
The chip select word contains the 3 chip select bits CS0, CS1 and CS2, thus allowing 8 memory chips to be connected in parallel. Chip select is achieved when the three control bits logically correspond to the selected conditions at the select inputs.

Check for End of Programming or Abortion of Programming Process

If the chip is addressed during active reprogramming by entering CS/E, the programming process is terminated. If, however, it is addressed by entering CS/A, the entry will be ignored. Only after programming has been terminated will the chip respond to CS/A. This allows the user to check whether the end of the programming process has been reached (**see figure 3**).

Memory Read

After the input of the first two control words CS/E and WA, a resetting of the start condition and the input of the third control word CS/A, the memory is set ready to read. During acknowledge clock nine, the memory information is transferred in parallel mode to the shift register. Subsequent to the trailing edge of the acknowledge clock, the data output is low impedance and the first data bit can be sampled (**see figure 4**).

With every shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented when the master receiver switches the data line to "low" during the ninth clock (acknowledge master). Any number of memory locations can thus be read one after the other. At address 256, an overflow to address 0 is initiated. With the stop condit-ion, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into the "1" state. During write, "0" states are generated according to the information in the internal data register, i. e. according to the third input control word. After the 27th and last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control.
The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage, the erase/write process extends over max. 20 ms, or more typically, 10 ms. In the case of data word input without write request (write request is defined as data bit in data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

Important: Switch-On Mode and Chip Reset

After the supply voltage V_{DD} has been connected, the data output will be in high impedance mode. As a rule, **the first operating mode** to be entered, should be the **read process of a word address**. As a result of the built-in "power on reset" circuit, programming requests will not be accepted immediately after the supply voltage has been switched on.

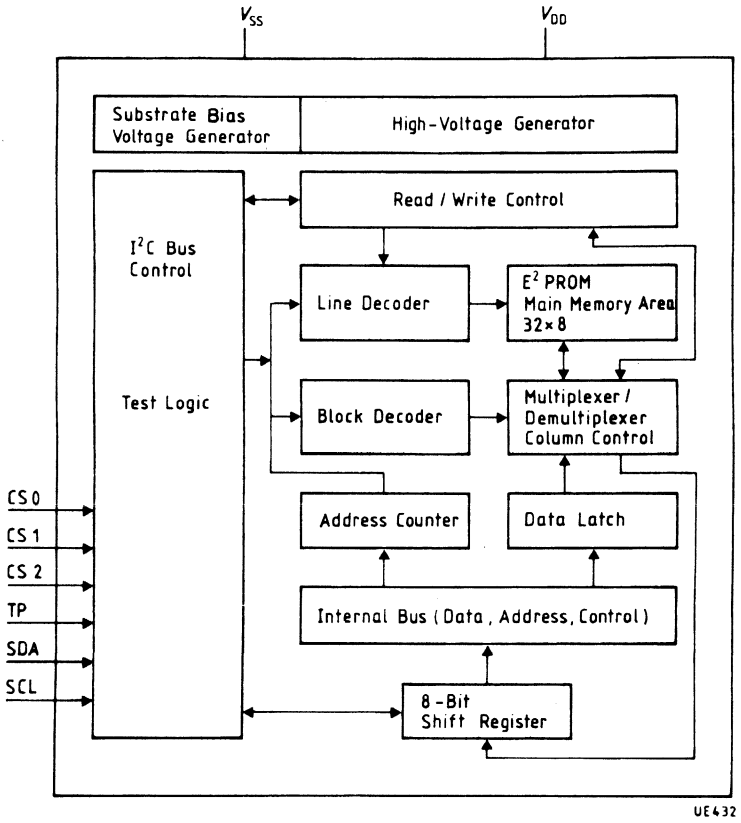
Total Erase

Enter the control word CS/E, load the address register with address 0 and the data register with FF (hex) to erase the entire contents of the memory. Switch input CS2 to "open" immediately prior to generating the stop condition. The subsequent stop condition triggers a total erase. Upon termination of "total erase", CS2 must be reconnected to either 0 V or $\geq$ 4.5 V.

Programming Disabled for Addresses 128 . . . 255 (CS0 open)

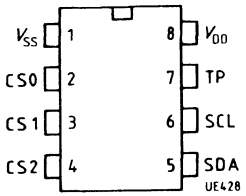
When pin 2 is not connected, i. e. when CS0 is floating, this means that:
1) memory reprogramming is disabled for addresses 128 . . . 255.
2) the chip can only be addressed with chip select bit CS0 = 0 of control word CS/E or CS/A.

Block Diagram



Pin Configuration

(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{SS}	Ground
2	CS0	Chip select $0 \leq V_I \leq 0.2$ V; $4.5 \leq V_I \leq V_{DD}$, open,programming disabled condition . (addresses 128...255)
3	CS1	Chip select
4	CS2	Chip select $0 \leq V_I \leq 0.2$ V; $4.5 \leq V_I \leq V_{DD}$, open total erase condition
5	SDA	Data line
6	SCL	Clock line
7	TP	Test pin
8	V_{DD}	Supply voltage

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{DD}	– 0.3	6	V
Input voltage	V_I	– 0.3	6	V
Power dissipation	P_D		130	mW
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system air)	$R_{th\,SA}$		100	K/W
Junction temperature	T_j		85	°C

Operating Range

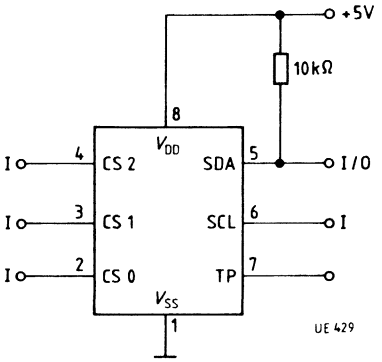
Supply voltage	V_{DD}	4.75	5.25	V
Ambient temperature	T_A	0	70	°C

Characteristics

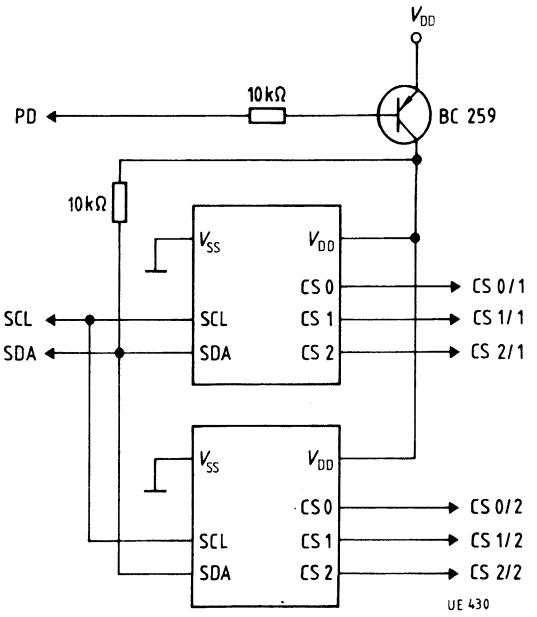
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{DD}	4.75	5.0	5.25	V	
Supply current	I_{DD}			20	mA	V_{DD} = 5.25 V
Inputs						
Input voltages SDA/SCL	V_{IL}			1.5	V	
Input voltages SDA/SCL	V_{IH}	3.0		V_{DD}	V	
Input currents SDA/SCL	I_{IH}			10	µA	$V_{IH} = V_{DD}$
Outputs						
Output current SDA	I_{QL}			3.0	mA	V_{QL} = 0.4 V
Leakage current SDA	I_{QH}			10	µA	$V_{QH} = V_{DD}$max
Inputs						
Input voltages CS0/CS1/CS2	V_{IL}			0.2	V	
Input voltages CS0/CS1/CS2	V_{IH}	4.5		V_{DD}	V	
Input currents CS0/CS1/CS2	I_{IH}			100	µA	V_{DD} = 5.25 V
Clock frequency	f_{SCL}			100	kHz	
Reprogramming duration	t_{PROG}		10	20	ms	erase and write
Input capacity	C_I			10	pF	
Total erase	t_{GL}			20	ms	CS2 = open

Test Circuit



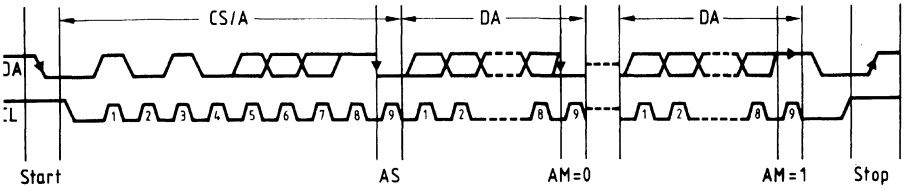
Application Circuit



Diagrams

Figure 1

Operation States of the I²C Bus
Read Access Short Form



leprogramming

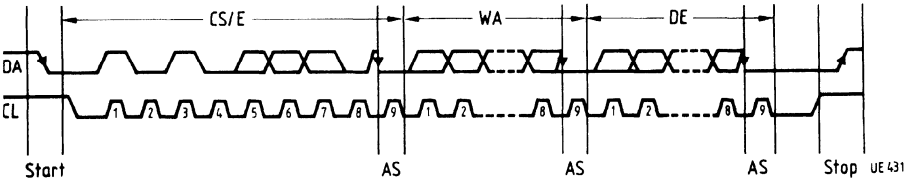
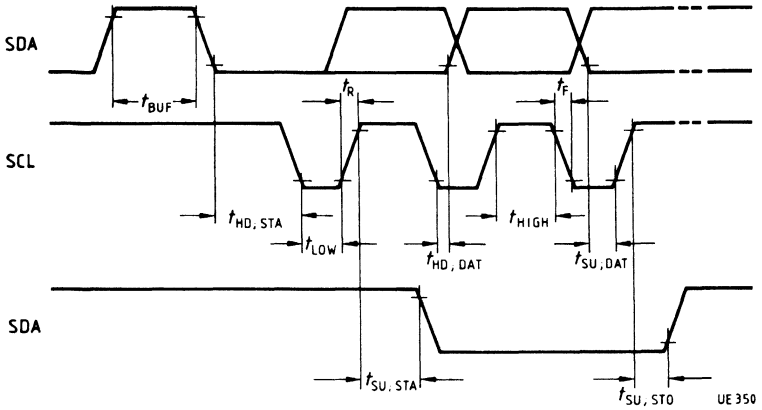


Figure 2

Timing Condition for I²C Bus (high-speed mode)



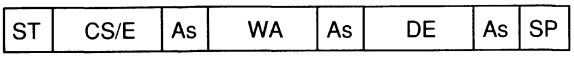
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Minimum time the bus must be free before a new transmission can start	t_{BUF}	4.7		µs
Start condition hold time	$t_{HD; STA}$	4.0		µs
Clock LOW period	t_{LOW}	4.7		µs
Clock HIGH period	t_{HIGH}	4.0		µs
Start condition set-up time, only valid for repeated start code	$t_{SU; STA}$	4.7		µs
Data set-up time	$t_{SU; DAT}$	250		ns
Rise time of both the SDA and SCL line	t_R		1	µs
Fall time of both the SDA and SCL line	t_F		300	ns
Stop condition set-up time	$t_{SU; STO}$	4.7		µs
Hold time data	$t_{HD; DAT}$	0*		

*Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

Figure 3

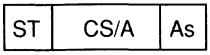
Programming

Control word input



(the reprogramming starts after this stop condition)

Check for program end by



1. when As = 1 programming is not finished
2. when As = 0 programming is finished

Program interruption by

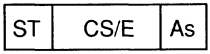
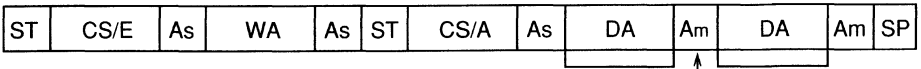


Figure 4

Read

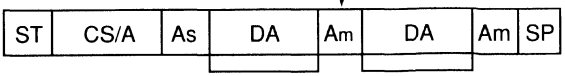
Control word input read
a) complete (with word address input)



n bytes Last byte

Automatic incrementation of the word address

b) shortened:
Bit 0 . . . 7 the last adapted word address keep unchanged



n bytes Last byte

Autoincrement Am = 0
before stop condition Am = 1

Control Word Table

Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	through memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	through memory
WA	A7	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0/1	through master

Control Word Input Key

CS/E	Chip select for data input memory
CS/A	Chip select for data output out of memory
WA	Memory word address
DE	Data word for memory
DA	Data word read out of memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS, CS1, CS2	Chip select bits
A0 to A7	Memory word address bits

SIEMENS

Nonvolatile Memory 2-Kbit E²PROM with I²C Bus and 2 K Write Protection

SDA 3526-2

Preliminary Data

MOS IC

Features

- Word-organized programmable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 256 × 8 bit organization
- Supply voltage 5 V
- Serial 2-line bus for data input and output (I²C bus)
- Reprogramming mode, 10 ms erase/write cycle
- Reprogramming by means of on-chip control (without external control)
- Check for end of programming process
- Programming disabled for addresses 0 . . . 255 (write protection mode)
- Data retention > 10 years
- More than 10^4 reprogramming cycles per address

Type	Ordering Code	Package
SDA 3526-2	Q67100-H5012	P-DIP-8

Circuit Description

I²C Bus Interface

The I²C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a serial data line SDA and a serial clock line SCL. The data line requires an external pull-up resistor to V_{DD} (open drain output stage).

The possible operational states of the I²C bus are shown in **figure 1**. In the quiescent state, both lines SDA and SCL are high, i. e. the output stage of the data line is disabled. As long as SCL remain "1", information changes on the data bus indicate the start or the end of data transfer between two components.

The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" is a stop condition. During a data transfer the information on the data bus will only change while the clock line SCL is "0".The information on SDA is valid as long as SCL is "1".'

In conjunction with an I²C bus system, the memory component can operate as a receiver and as a transmitter (slave receiver or slave transmitter). Between a start and stop condition, information is always transmitted in byte-organized form. Between the trailing edge of the eighth clock pulse and a ninth acknowledge clock pulse, the memory component sets the SDA line to low as a confirmation of reception, if the chip select conditions have been met. During the output of data, the data output of the memory is high in impedance during the ninth clock pulse (acknowledge master).

Control Functions of the I^2C Bus

The memory component is controlled by the controller (master) via the I^2C bus in two operating modes: read-out cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes and an additional acknowledge clock pulse to the bus after the start condition. During a memory read, at least nine additional clock pulses are required to accept the data from the memory and the acknowledge master, before the stop condition may follow. In the case of programming, the active programming process is only started by the stop condition after data input (**see figure 3**).
The chip select word contains the 3 chip select bits CS0, CS1 and CS2, thus allowing 8 memory chips to be connected in parallel. Chip select is achieved when the three control bits logically correspond to the selected conditions at the select inputs.

Check for End of Programming or Abortion of Programming Process

If the chip is addressed during active reprogramming by entering CS/E, the programming process is terminated. If, however, it is addressed by entering CS/A, the entry will be ignored. Only after programming has been terminated will the chip respond to CS/A. This allows the user to check whether the end of the programming process has been reached **(see figure 3).**

Memory Read

After the input of the first two control words CS/E and WA, a resetting of the start condition and the input of the third control word CS/A, the memory is set ready to read. During acknowledge clock nine, the memory information is transferred in parallel mode to the shift register. Subsequent to the trailing edge of the acknowledge clock, the data output is low impedance and the first data bit can be sampled (**see figure 4**).

With every shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented when the master receiver switches the data line to "low" during the ninth clock (acknowledge master). Any number of memory locations can thus be read one after the other. At address 256, an overflow to address 0 is initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into the "1" state. During write, "0" states are generated according to the information in the internal data register, i. e. according to the third input control word. After the 27th and last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control.
The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage, the erase/write process extends over max. 20 ms, or more typically, 10 ms. In the case of data word input without write request (write request is defined as data bit in data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

Important: Switch-On Mode and Chip Reset

After the supply voltage V_{DD} has been connected, the data output will be in high-impedance mode. As a rule, **the first operating mode** to be entered, should be the **read process of a word address.** As a result of the built-in "power on reset" circuit, programming requests will not be accepted immediately after the supply voltage has been switched on.

Total Erase

Enter the control word CS/E, load the address register with address 0 and the data register with FF (hex) to erase the entire contents of the memory. Switch input CS2 to "open" immediately prior to generating the stop condition. The subsequent stop condition triggers a total erase. Upon termination of "total erase", CS2 must be reconnected to either 0 V or $\geq$ 4.5 V.

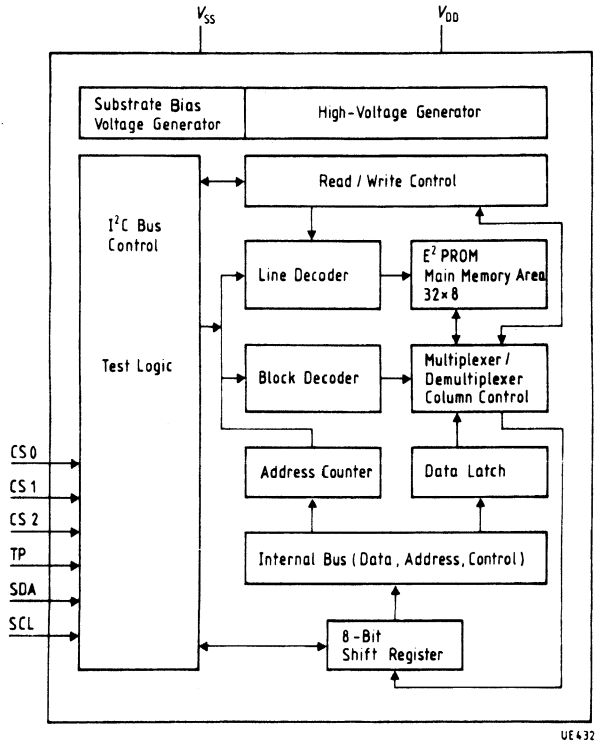
Programming Disabled for Addresses 0 . . . 255 (CS0 open)

When pin 2 is not connected, i. e. when CS0 is floating, this means that:

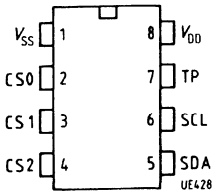
1) memory reprogramming is disabled for addresses 0 . . . 255.

2) the chip can only be addressed with chip select bit CS0 = 0 of control word CS/E or CS/A.

Block Diagram



Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{SS}	Ground
2	CS0	Chip select $0 \leq V_I \leq 0.2$ V; $4.5 \leq V_I \leq V_{DD}$ open, programming disabled condition (addresses 0 ... 255)
3	CS1	Chip select
4	CS2	Chip select $0 \leq V_I \leq 0.2$ V; $4.5 \leq V_I \leq V_{DD}$ open, total erase condition
5	SDA	Data line
6	SCL	Clock line
7	TP	Test pin
8	V_{DD}	Supply voltage

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage range	V_{DD}	– 0.3	6	V
Input voltage range	V_I	– 0.3	6	V
Power dissipation	P_D		130	mW
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		100	K/W
Junction temperature	T_j		85	°C

Operating Range

Supply voltage	V_{DD}	4.75	5.25	V
Ambient temperature	T_A	0	70	°C

Characteristics

T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{DD}	4.75	5.0	5.25	V	
Supply current	I_{DD}			20	mA	V_{DD} = 5.25 V

Inputs

Input voltages SDA/SCL	V_{IL}			1.5	V	
Input voltages SDA/SCL	V_{IH}	3.0		V_{DD}	V	
Input currents SDA/SCL	I_{IH}			10	µA	$V_{IH} = V_{DD}$

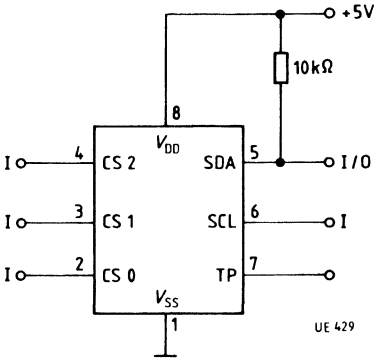
Outputs

Output current SDA	I_{QL}			3.0	mA	V_{QL} = 0.4 V
Leakage current SDA	I_{QH}			10	µA	$V_{QH} = V_{DD}$max

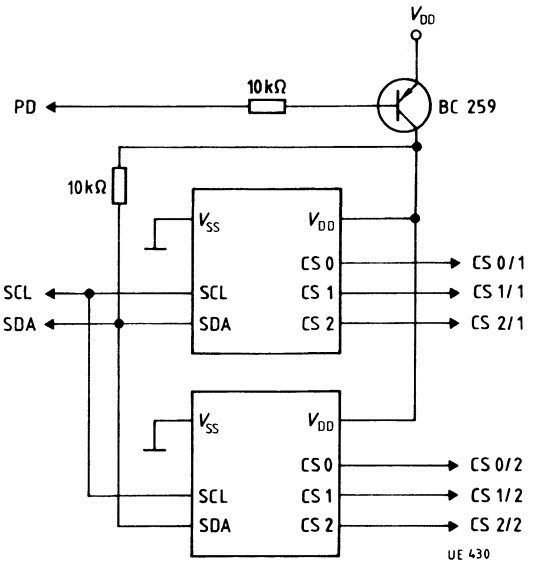
Inputs

Input voltages CS0/CS1/CS2	V_{IL}			0.2	V	
Input voltages CS0/CS1/CS2	V_{IH}	4.5		V_{DD}	V	
Input currents CS0/CS1/CS2	V_{IH}			100	µA	V_{DD} = 5.25 V
Clock frequency	f_{SCL}			100	kHz	
Reprogramming duration	t_{PROG}		10	20	ms	Erase and write
Input capacity	C_I			10	pF	
Total erase	t_{GL}			20	ms	CS2 = open

Test Circuit



Application Circuit



Diagrams

Figure 1
Operational States of the I^2C Bus
Read Cycle Shortened

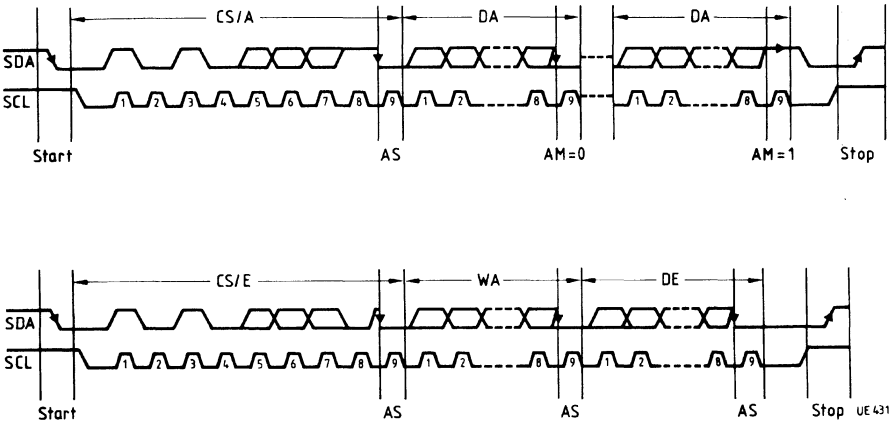
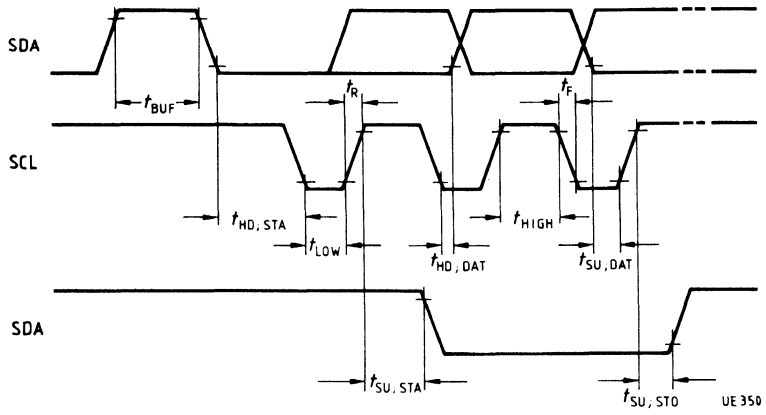


Figure 2
Timing Conditions for the I^2C Bus



Absolute Maximum Ratings

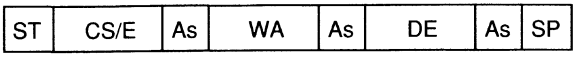
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Minimum time the bus must be free before a new transmission can start	t_{BUF}	4.7		µs
Start condition hold time	$t_{HD;STA}$	4.0		µs
Clock LOW period	t_{LOW}	4.7		µs
Clock HIGH period	t_{HIGH}	4.0		µs
Start condition set-up time, only valid for repeated start code	$t_{SU;STA}$	4.7		µs
Data set-up time	$t_{SU;DAT}$	250		ns
Rise time of both the SDA and SCL line	t_R		1	µs
Fall time of both the SDA and SCL line	t_F		300	ns
Stop condition set-up time	$t_{SU;STO}$	4.7		µs
Hold time data	$t_{HD;DAT}$	0*)		

*) Note that a transmitter must internally provide at least a hold time to bridge the undefined region max. 300 ns) of the falling edge of SCL.

Figure 3

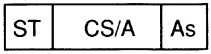
Programming

Control word input



(the reprogramming starts after this stop condition)

Check for program end by



1. when As = 1 programming is not finished
2. when As = 0 programming is terminated

Program interruption by

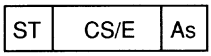
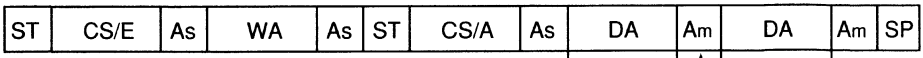


Figure 4

Read

Control word input read
a) complete (with word address input)

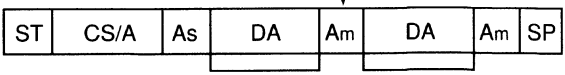


n bytes

Last byte

Automatic incrementation of the word address

b) shortened:
Bit 0 . . . 7 the last selected word address remain unchanged



n bytes

Last byte

Autoincrement before stop condition Am = 0
Am = 1

Control Word Table

Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	through memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	through memory
WA	A7	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0/1	through master

Control Word Input Key

CS/E	Chip select data input into memory
CS/A	Chip select for data output out of memory
WA	Memory word address
DE	Data word for memory
DA	Data word read out of memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS0, CS1, CS2	Chip select bits
A0 to A7	Memory word address bits

SIEMENS

Prescaler 1: 64 / 1: 256 for 1.3 GHz

SDA 4212

Bipolar IC

Features

- Pin programmable prescaler ratio of 1:64 or 1:256
- Symmetrical push-pull input
- Low harmonic wave
- Minimal current consumption of 23 mA

Type	Ordering Code	Package
SDA 4212	Q67000-A8049	P-DIP-8
SDA 4212-X	Q67000-A8145	P-DSO-8

Circuit Description

The SDA 4212 has been designed for application in television receivers operating according to the frequency synthesis tuning principle. The component includes a preamplifier and an ECL prescaler stage with symmetrical ECL push-pull outputs. It can be operated with a prescaler ratio of 1:64 or 1:256.
The component has been designed for a max. input frequency of 1.3 GHz.

The preamplifier of the component has been designed with symmetrical push-pull inputs. During the asymmetrical drive of one of the inputs, the other input has to be decoupled to ground by a capacitor (approx. 1.5 nF) of low series inductance.

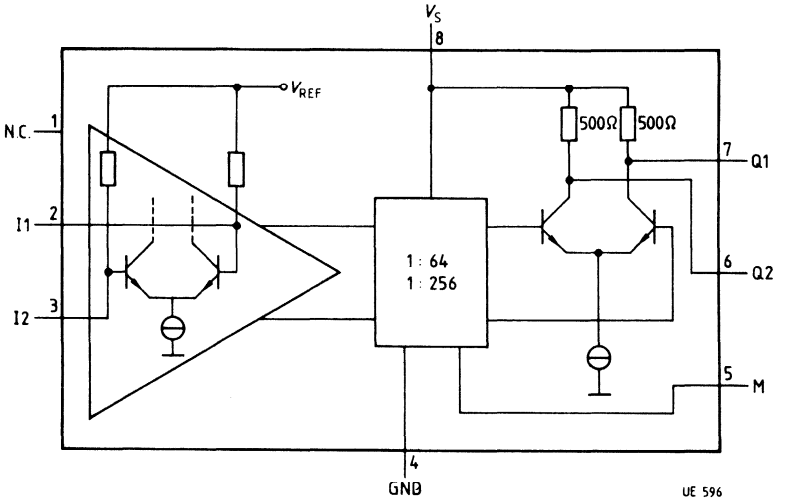
The prescaler stage of the component is comprised of several status controlled master slave flipflops. Their prescaler ratio can be set with the switch-over input M as follows:

M to V_S = 1:64
M to ground = 1:256

The symmetrical push-pull outputs of the prescaler include an internal resistor of 500 Ω each. The DC voltage level at the outputs is connected to the supply voltage V_S (output "High" = V_S). Typical output deviation is 1.0 V_{pp}.

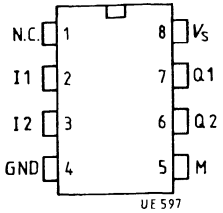
The typical output modulation is 0.6 V_{pp}.

Block Diagram

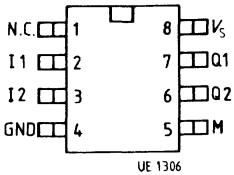


Pin Configuration
(top view)

P-DIP-8



P-DSO-8



Pin Definitions and Functions

Pin No.	Symbol	Function
1	N.C.	Not connected
2	I 1	Input
3	I 2	Input
4	GND	Ground
5	M	Switch-over input M for prescaler ratio
6	Q2	Output
7	Q1	Output
8	V_S	Supply voltage

Absolute Maximum Ratings

Parameter	Symbol	Limit Values			Remarks
		min.	max.	Unit	
Supply voltage	V_S	– 0.3	6	V	
Input voltage (pin 2, pin 3)	V_I		2.5	V_{PP}	
Output voltage (pin 6, pin 7)	V_Q		V_S	V	
Output current (pin 6, pin 7)	$-I_Q$		10	mA	
Input voltage (pin 5)	V_M	– 0.3	V_S	V	
Junction temperature	T_j		125	°C	
Storage temperature	T_{stg}	– 55	125	°C	
Thermal resistance (system-air)	$R_{th\ SA}$		105	K/W	P-DIP-8 package
Overload resistance (ESD protection single discharge of 100 pF capacitor through a1.5 kΩ resistor to each pin)	V_{MOS}	– 2000	2000	V	not required pins float: pin 4 and pin 8 always to ground

Operating Range

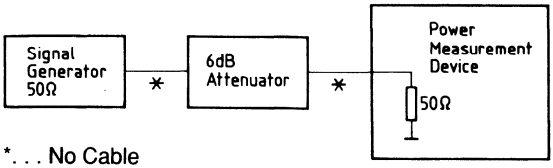
Supply voltage	V_S	4.5	5.5	V	
Input frequency	f	70	1300	MHz	
Ambient temperature	T_A	0	80	°C	

Characteristics
V_S = 5 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Current comsumption	I_S		23.5	29.5	mA	inputs decoupled outputs n.c.; M n.c.	
Input level ("input sensitivity")	V_I	– 26/11		3/315	dBm/mV	70 MHz	1
		– 27/10		3/315	dBm/mV	80 MHz	1
		– 30/7		3/315	dBm/mV	120 MHz	1
		– 32/5.5		3/315	dBm/mV	250 MHz	1
		– 27/10		3/315	dBm/mV	600 MHz	1
		– 27/10		3/315	dBm/mV	1000 MHz	1
		– 22/18		3/315	dBm/mV	1100 MHz	1
		– 15/40		3/315	dBm/mV	1200 MHz	1
		– 9/80		3/315	dBm/mV	1300 MHz	1
Output volt. deviation	V_Q	0.4	0.6		V_{PP}	$C_L \leq 15$ pF; $f \leq 1000$ MHz	1
		0.8	0.9		V_{pp}	$C_L \leq 15$ pF; $f \leq 1$ GHz	1
DC voltage offset of outputs	ΔV_Q			100	mV		3
M-input current "LOW" (prescaler ratio 1:256)	I_M		2	100	µA	M = ground	1
M-input current "HIGH" (prescaler ratio 1:64)	I_M		0	50	µA	M = V_S	1
M-input voltage "HIGH"	V_{MH}	3.0			V		1
M-input voltage "LOW"	V_{ML}			0.2	V		1
Amplitude of the 3rd harmonic at output (referenced to 1st harmonic)	A_3		– 30		dB	f = 700-900MHz;	1,4
			– 35		dB	M = V_S	2,4

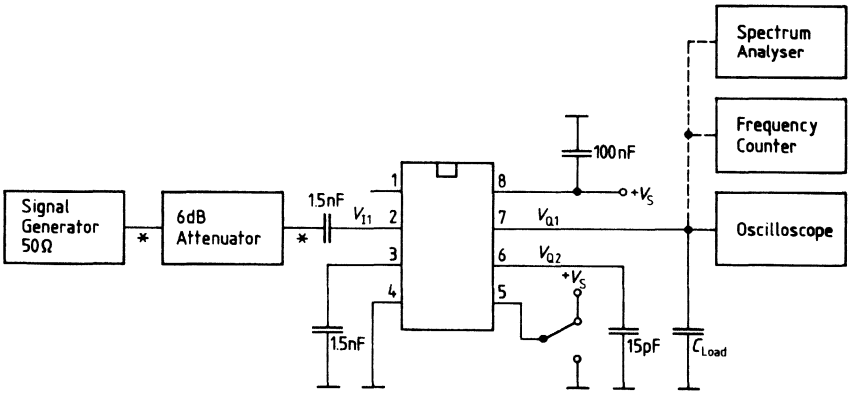
Test Circuit 1

Calibration of Signal Generator



*. . . No Cable

Measurement Configuration for Input Sensivity and Output Voltage Deviation

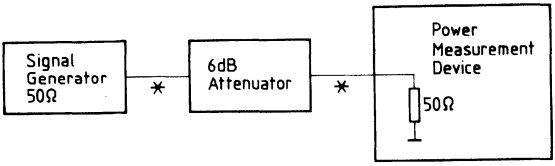


*. . . No Cable

C_{Load}+capacities of the measurement devices = 15 pF (for measurement of the output voltage deviation)

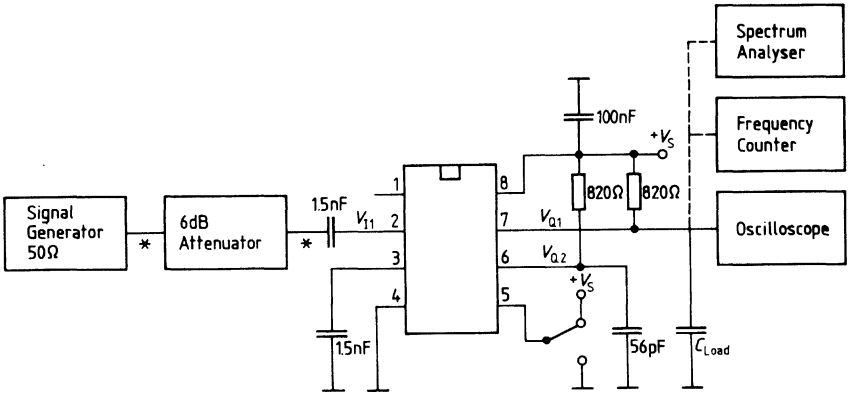
Test Circuit 2

Calibration of Signal Generator



*. . . No Cable

Measurement Configuration for Input Sensivity and Output Voltage Deviation

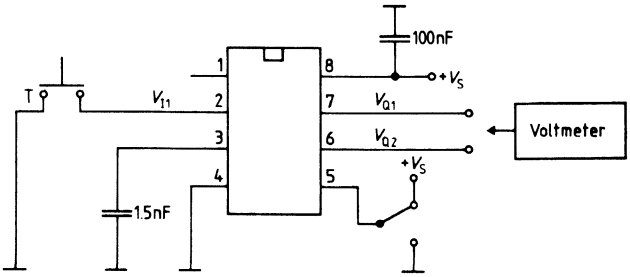


*. . . No Cable

C_{Load}+capacities of the measurement devices = 15 pF (for measurement of the output voltage deviation)

Test Circuit 3

DC Voltage Offset Measurement of Outputs



Note: press key T until outputs turn over

SIEMENS

Data Slicer for Teletext

SDA 5231-2

Preliminary Data

Bipolar IC

Features

- Crystal-stable data clock regeneration for a bit rate of 6.9375 MHz
- Separation and regeneration of teletext information
- Separation of the horizontal and vertical synchronization signals
- Phase-locked coupling of 6-MHz oscillator with comp. video
- Optional adjustment to 1 V or 2.5 V comp. video level
- Processing of externally separated teletext data
- Output of negative and positive synchronous signals to television set

Type	Ordering Code	Package
SDA 5231-2	Q 67000-A 5006	P-DIP-28

The SDA 5231-2 has been designed to separate teletext signals from TV signals for a microcontroller-operated I^2C bus concept. The video processor meets the requirements for teletext data clock regeneration and synchronization of the TV set during teletext operation. At the same time, the video signals (CVBS) provided by the television set are evaluated for the teletext decoder.

Functional Description

The SDA 5231-2 is used in an I^2C bus controlled teletext system. Its function is the processing of the teletext informations, the system clock generation and the switching of HV synchronization signals.

The SDA 5231-2 can also be used to process the data line 16 (VPS).

a) **Signal Processing**

The analog signal is processed at the amplitude filter (clamping of the video input signal and separation of the sync impulse) and by means of the data slicing level. The data slicer compensates the attenuation of the data signal due to mistuning and a non linear frequency response the IF-amplifier.

As in case of sync impulse separation, an adaptive circuit is used for separating the data, i.e. the clipping level is always in the middle of the sync impulse and/or the data signal, independent of the signal amplitude.

Both the clipping level and the control voltage for the AGC (Automatic Gain Control) are generated while bit synchronization takes place at the beginning of the teletext line and are stored until the teletext line has been fully scanned.

b) **Synchronization of Data Clock**

Clock synchronization is obtained by means of a phase detector + a phaseshifter.
A control voltage proportional to the phase difference between the free running oscillator and the incoming data bits is generated by the phase detector. A small time constant is used during bit synchronization, for the rest of the time a 10 times larger constant is used.

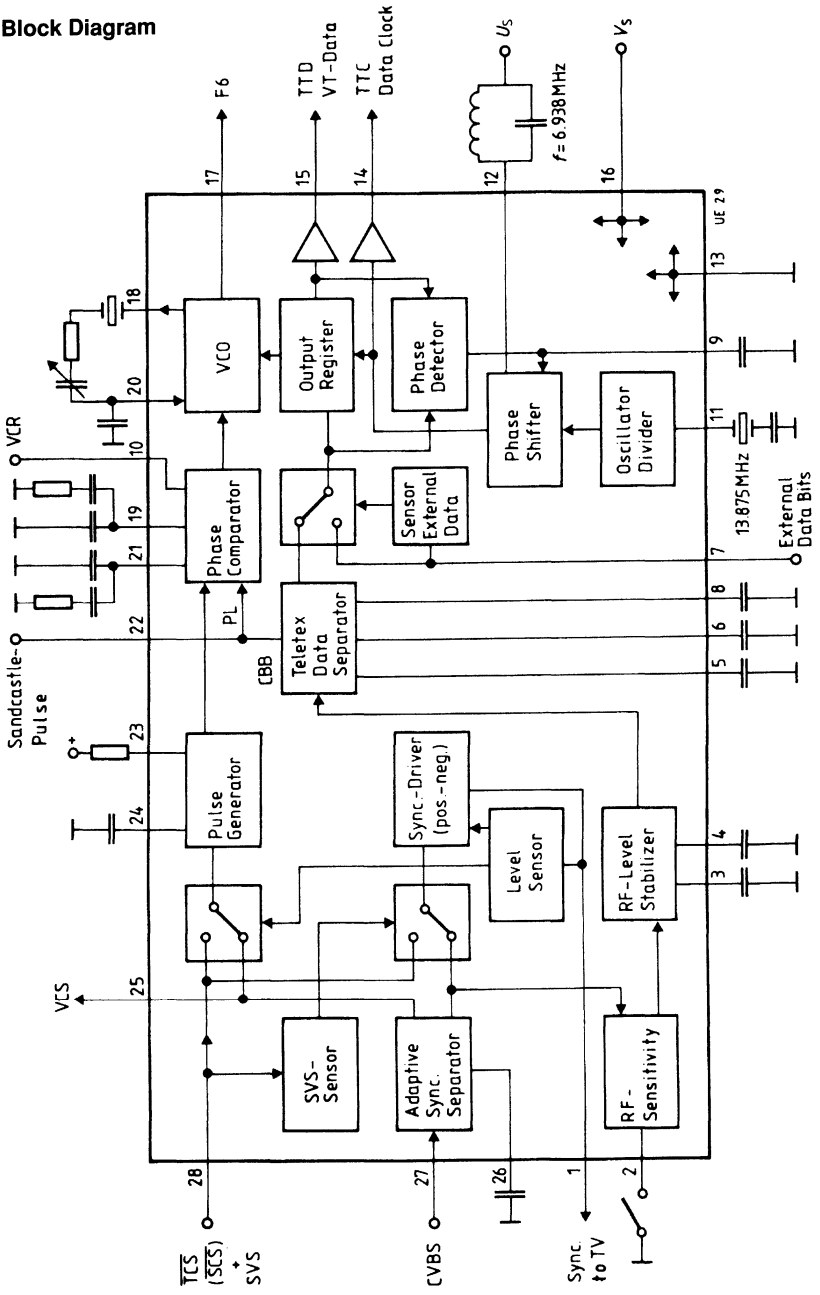
c) **Generation of 6-MHz System Clock**

The teletext processor generates a picture pixel raster from the 6-MHz system clock. Thus, synchronization of the 6-MHz clock with the CVBS line frequency is necessary for any mixed-mode with teletext.
By shortening all sync pulses to approximately 2 µs, interference from synchronization frame pulses can be avoided by means of a mono flop. The SANDCASTLE derived from the 6-MHz clock signal is synchronized in a phase-locked loop to the shortened sync pulse. A shorter time constant is used during synchronization. If the CVBS signal is noisy or during after-hours operation, 2 points are important: Data acquisition has to be stopped, and the 6-MHz VCO must oscillate with its nominal frequency. For this purpose the teletext processor controls the VCS signal and switches off the signal component PL of the SANDCASTLE signal, if the CVBS signal is noisy or non-existent.

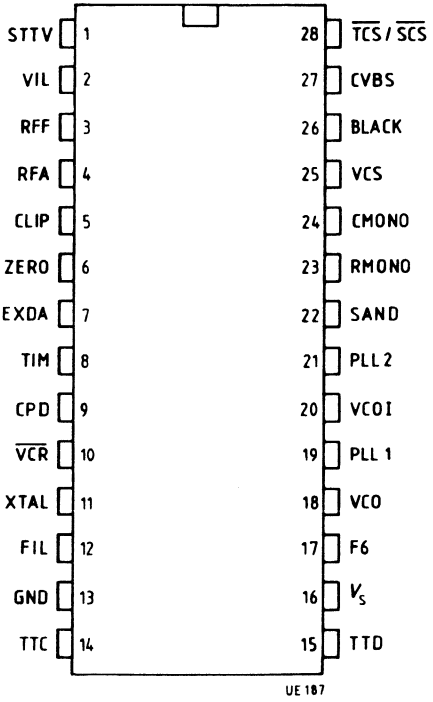
d) **Operating-Mode Switch**

Operation Mode	**Switch by**	**System Clock Sync to**	**Usage**
CVBS	Pin 28 = NC	CVBS	i.e. sub-titles
TCS	$V_{28} < 6.1$ V	CVBS	After-hours synchronization interlace/non-interlace mode
SCS	Pin 1 = NC	SCD	Slave-Mode i.e. external synchronization

Block Diagram



Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function	Description
1	STTV	Sync -output	**Sync-Output:** positive or negative synchronous signal to synchronize the TV set. Connection of load resistor to pin 1 (1.2 kΩ) against V_S = negative synchronous signal. Connection of load resistor to pin 1 against ground = positive synchronous signal.
2	VIL	Level selection	**CVBS Input Level Selection:** with LOW the gain is adjusted to a 1 V level and with an open input to 2.5 V level.
3	RFF	RF-filter	**RF-Level Stabilizer:** capacitor for filter time constant
4	RFA	RF-amplitude	**RF-Level Stabilizer:** capacitor for internal amplitude-dependent control voltage
5	CLIP	Clipping level	Input capacitor for **Clipping Level** of adapted **Data Separation**
6	ZERO	Zero level	Input capacitor for **Zero Level** of adapted **Data Separation**
7	EXDA	External teletext data	Data input for **External Teletext Data** (already separated)
8	TIM	Time characteristics	Capacitor for **Time Characteristics** of adapted **Data Separation**
9	CPD	Clock phase detector	**Clock Phase Detector:** connection for input capacitor
10	$\overline{\text{VCR}}$	Video tape recorder mode	**Video Tape Recorder Mode:** switch-over to short horizontal hold-time constant
11	XTAL	Crystal	**13.875 MHz Crystal Connection:** frequency for double teletext data rate
12	FIL	Filter connection	**Filter Connection** for 6.9375 MHz data clock
13	GND	Ground	**Ground** (0 V)
14	TTC	TTC-output	**TTC Output**
15	TTD	TTD-output	**TTD Output**
16	V_S	V_S	**Supply Voltage** +
17	F6	F6-output	**F6 Output:** 6-MHz clock (signal with negligible harmonic wave)
18	VCO	VCO-output	**6-MHz VCO Output** for frequency-determining resonant circuit
19	PLL1	PLL-low-pass-filter	**PLL-Low-Pass-Filter** with small time-constant by async. operation (filter 2)

Pin Definitions and Functions(cont'd)

Pin No.	Symbol	Function	Description
20	VCOI	VCO-input	**6-MHz VCO input** for frequency-determining resonant circuit
21	PLL2	PLL-low-pass-filter	**PLL-Low-Pass-Filter** with bigger time-constant for standard operation
22	SAND	Sandcastle pulse	**Sandcastle Pulse**
23	RMONO	R-Monoflop	**Chronology Resistor** of the monoflops
24	CMONO	C-Monoflop	**Chronology Capacitor** of the monoflops
25	VCS	VCS-output	**VCS-Output:** synchronous signal separated from comp. video
26	BLACK	Black level input capacitor	**Black Level Input Capacitor** for the adapted synchronous pulse separator
27	CVBS	CVBS-input	**CVBS Input Signal** via coupling capacitor with 1 V signal level when pin 2 is connected to ground
28	$\overline{\text{TCS}}$/ $\overline{\text{SCS}}$	$\overline{\text{TCS}}$-, ($\overline{\text{SCS}}$)-input	**Synchronous Signal-Input** $\overline{\text{TCS}}$ during text playback (or $\overline{\text{SCS}}$, when pin 1 is open)

Absolute Maximum Ratings
T_A = 25 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	$V_{16/13}$		13.2	V
Storage temperature range	T_{stg}	– 40	125	°C
Output current VCS	$-I_{25H}$		5	mA
Output current TTD	$-I_{15H}$		10	mA
Output current TTC	$-I_{14H}$		10	mA
Output current F6	$-I_{17H}$		10	mA
Output current Sync.	$\pm I_1$		5	mA
Thermal resistance (system-air)	$R_{th\ SA}$		50	K/W

Operating Range

Supply voltage	$V_{16/13}$	10.8	13.2	V
Ambient temperature in operation	T_A	0	70	°C

Characteristics
T_A = 25°C; V_S = 12 V ± 10%

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply current	I_S	53	70	100	mA

CVBS Input, pin 27

Input signal level					
Pin 2 to ground	V_{27}	0.7	1	1.4	V
Pin 2 open	V_{27}	1.75	2.5	3.5	V
Synchronous signal amplitude	$V_{27\,sync}$	0.1		1	V
Teletext data level					
Pin 2 to ground	$V_{27\,VTD}$	0.3	0.46	0.7	V
Pin 2 open	$V_{27\,VTD}$	0.75	1.15	1.75	V
Generator resistor	$R_{G\,27}$			250	Ω

Adaptation to CVBS Level

Input voltage					
V_{27} = 1 V when	$V_{2/13\,L}$	0		0.8	V
V_{27} = 2.5 V when	$V_{2/13\,H}$	2.0		5.5	V
Input current	$-I_{2L}$	0		150	µA
	I_{2H}	0		1.3	mA

Teletext Data

Output signal TTD	v_{15}	2.5	3.5	4.5	V
Transition times	t_r, t_f	20	30	45	ns
Max. permissible capacitative load	$C_{15/13}$			40	pF
Data clock signal TTC	v_{14}	2.5	3.5	4.5	V
Transition times	t_r, t_f	20	30	45	ns
Max. permissible capacitative load	$C_{14/13}$			40	pF
Time deviation with respect to TTD	t_d	– 20	0	20	ns
DC voltage at outputs	$V_{14,15/13}$		4		V

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Synchronous Pulse Separation VCS (Signal at teletext decoder)					
Output voltage	$V_{25\,L}$ $V_{25\,H}$	0 2.4		0.4 5.5	V V
Output current	$I_{25\,L}$ $-I_{25\,H}$			0.5 1.5	mA mA
Delay with respect to CVBS sync	t_d		0.5		µs
Sync Output Driver (Signal at TV set)					
Output voltage TCS operation Comp. video operation	 V_1 V_1		 0.45	 1	 V V
Positive synchronous signal DC voltage load resistor to ground		 1.4			 V
Output current	$-I_1$			3	mA
Negative synchronous signal DC voltage load resistor to V_S	$V_{1/13}$		 10.1		 V
Output current	I_1			3	mA
6-MHz Clock F6					
F6-output signal (negligible harmonic content)	V_{17}	1	2	3	V
Transition times	t_r, t_f	20		40	ns
Max. permissible capacitative load	$C_{17/13}$			40	pF
DC voltage at output	$V_{17/13}$	4		8.5	V
Synchronisation Selection SVS					
Input current during TCS operation V_{28} = 0 ... 6.1 V CVBS[1)] CVBS V_{28} = 10 ... V_S	 $-I_{28}$ $-I_{28}$ I_{28}	 40 – 5	 70	 100 15 5	 µA µA µA
TCS Operation					
Input voltage Load resistor at pin 1 Load resistor at pin 1	 $V_{28\,L}$ $V_{28\,H}$	 0 2	 	 0.8 6.1	 V V

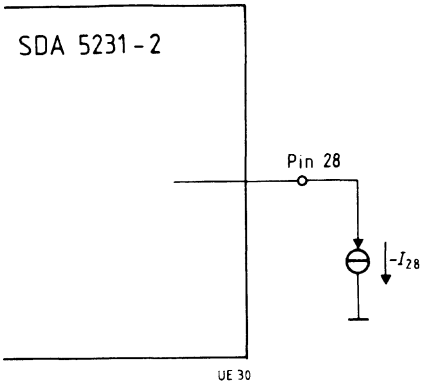
Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
SCS Operation					
Input voltage Pin 1 open Pin 1 open	 $V_{28\,L}$ $V_{28\,H}$	 0 3.5		 1.5 6.1	 V V
Line synchronous pulse width TCS operation SCS operation	 t_p t_p		 2 3		 µs µs
VCR Operation					
Input voltage during VCR operation Standard operation	 $V_{10\,/\,13\,L}$ $V_{10\,/\,13\,H}$	 0 2		 0.8 V_S	 V V
Input current	I_{10}	– 10	0	10	µA
Sandcastle Pulse Input					
Phase locked mode input voltage PL Input voltage PL	 $V_{22\,/\,13\,L}$ $V_{22\,/\,13\,H}$	 0 3.9		 3 5.5	 V V
PL-low-time for free-wheeling oscillator	t_{pL}	100			ms
Reset pulse for data separation Input voltage CBB Input voltage CBB	 $V_{22\,/\,13\,L}$ $V_{22\,/\,13\,H}$	 0 1		 0.5 5.5	 V V
Input current	I_{22}	– 10		10	µA
Input for External Data (current source driving)					
Internal data processing Input current[2] Voltage I_7 = – 10 to + 100 µA	 I_7 V_7	 – 10	 0	 100	 µA
External data processing Input current for LOW[2] for HIGH[2] Voltage I_7 = – 25 to – 1000 µA	 $I_{7\,L}$ $I_{7\,H}$ V_7	 – 175 – 1000 7	 – 40 – 500 8	 – 25 – 325	 µA µA V

[1] **Remarks:** Test circuit 1
[2] Test circuit 2

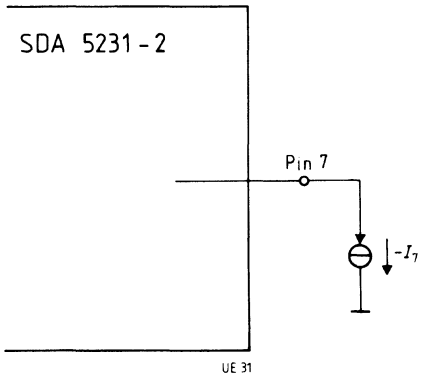
Test Circuits

Test Circuit 1



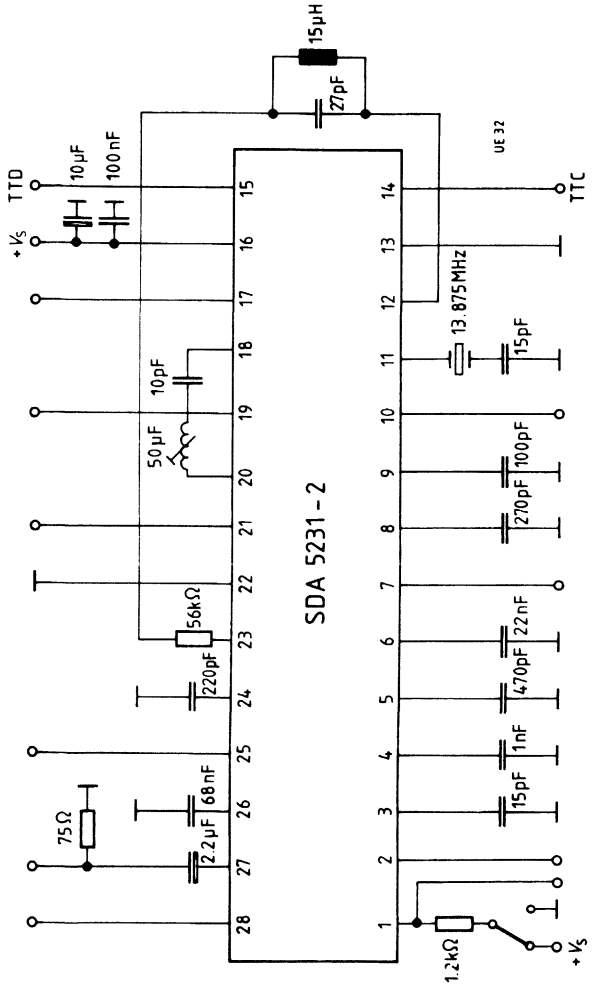
During CVBS operation the output current of pin 28 shall not exceed 15 µA (the pin 12 of the decoder SDA 5242-3 is high-impedance connected).

Test Circuit 2

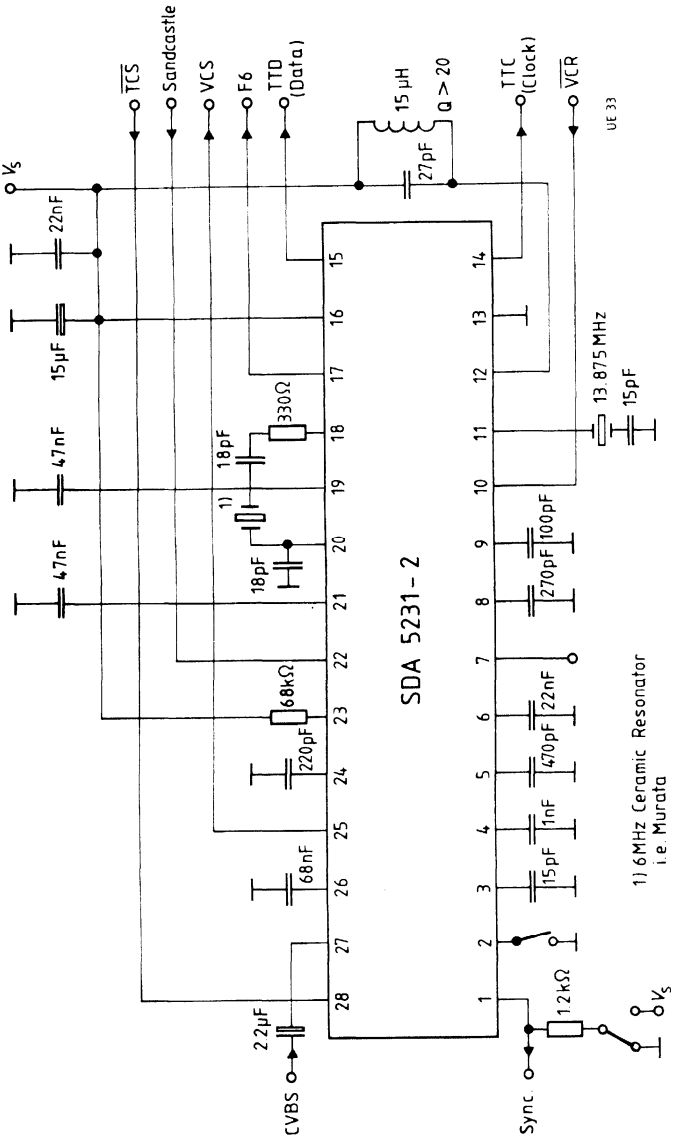


The output current of pin 7 cannot be higher than 10 µA if the processing of the teletext data (wich is in CVBS) must occur.

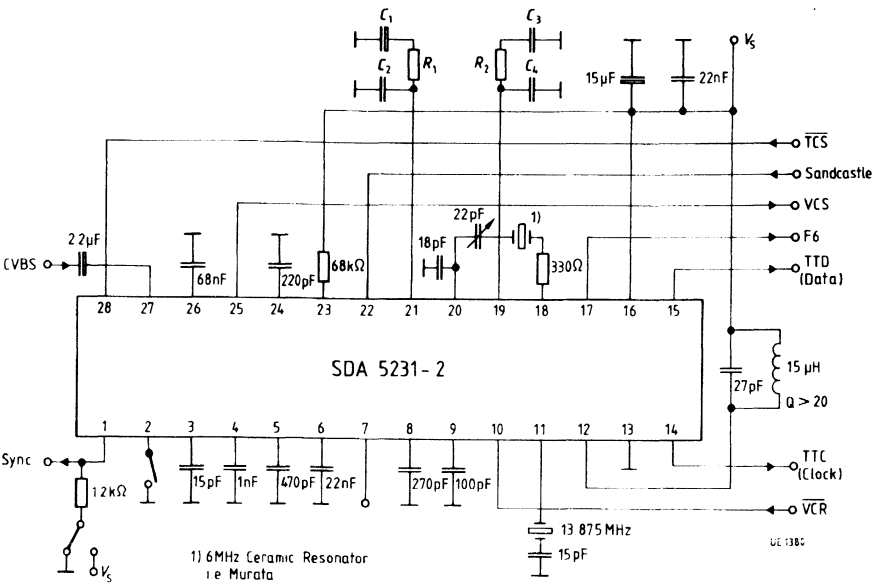
Test Circuit 3



Application Circuit Crystal

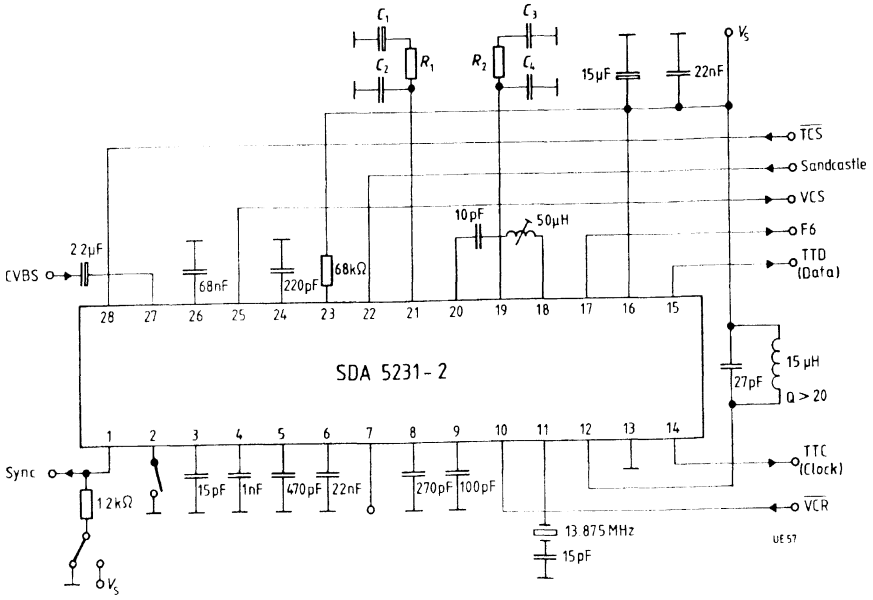


Application Circuit Ceramic Resonator



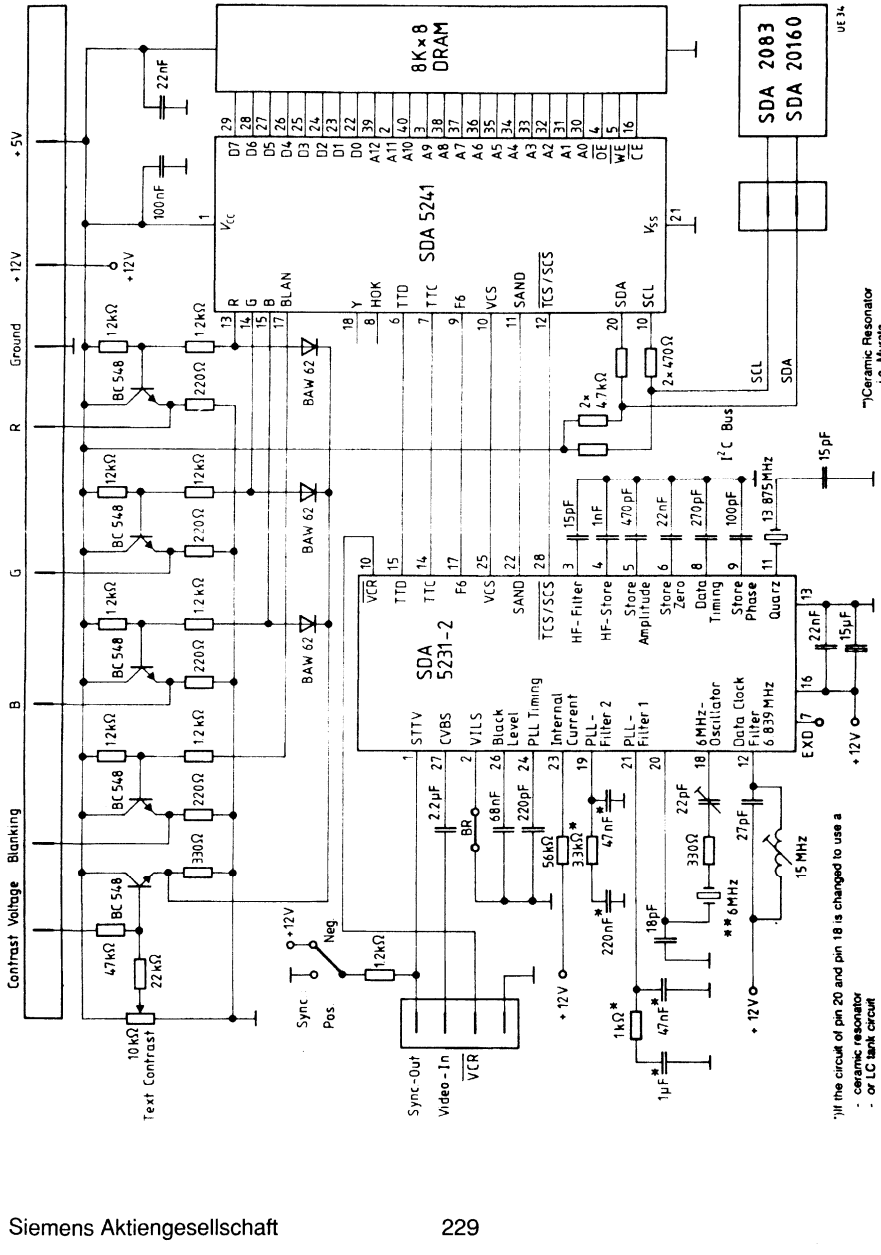
Loop Filter Components	Standard Application	Optimized PLL Behaviou
C_1	47 µF	47 µF
C_2	47 nF	4.7 µF
C_3	47 nF	2.2 µF
C_4	47 nF	220 nF
R_1	82 kΩ	82 Ω
R_2	3.3 kΩ	390 kΩ

Application Circuit LC-Tank-Circuit

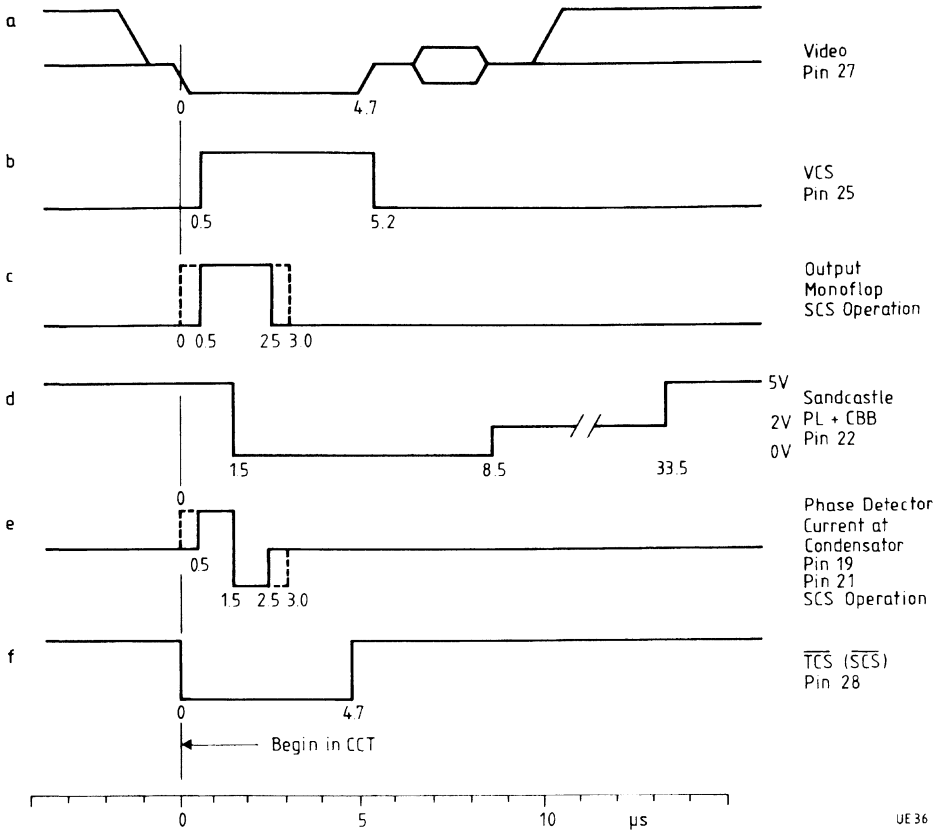


Loop Filter Components	Standard Application	Optimized PLL Behaviour
C_1	1 µF	10 µF
C_2	47 nF	1 µF
C_3	220 nF	330 nF
C_4	47 nF	33 nF
R_1	1 kΩ	560 Ω
R_2	3.3 kΩ	3.3 kΩ

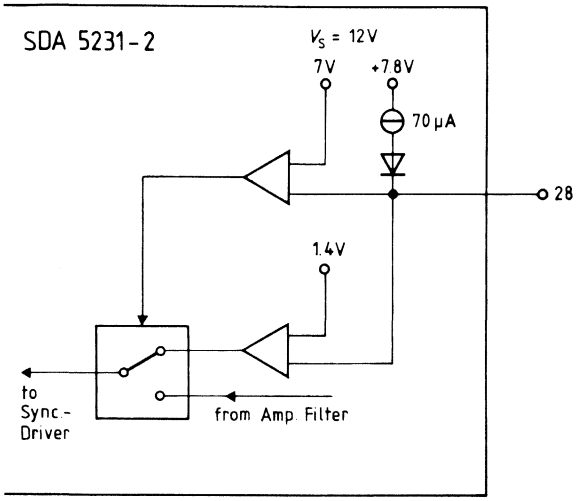
Application Circuit with SDA 5241



Pulse Diagrams

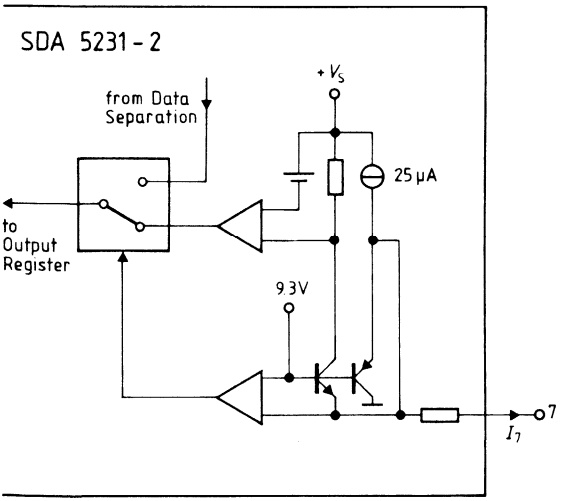


Pin 28



TCS Operation: $V_{28} < 6.1V$ UE37

Pin 7



External Data Processing: $I_7 > 25\ \mu A$ UE38

SIEMENS

Teletext Processor — SDA 5243-2

Preliminary Data — **MOS IC**

Features

- Microcomputer controlled via I^2C bus (includes full memory access)
- Uses standard 8 K × 8 static, 8 K × 8 dyn. or two 8 K × 4 dyn. RAMs
- Can store 8 teletext pages and acquire 4 pages simultaneously
- 12 × 10 dot matrix for characters and graphic
- Extra display row for status messages
- Acquisition during the vertical blanking interval or for cable text during all lines
- 60-Hz recognition and display without additional hardware
- Field detection for noninterlace display
- STATUS information for asynchronous operation

Type	Ordering Code	Package
SDA 5243-2	Q 67100-H5031	P-DIP-40

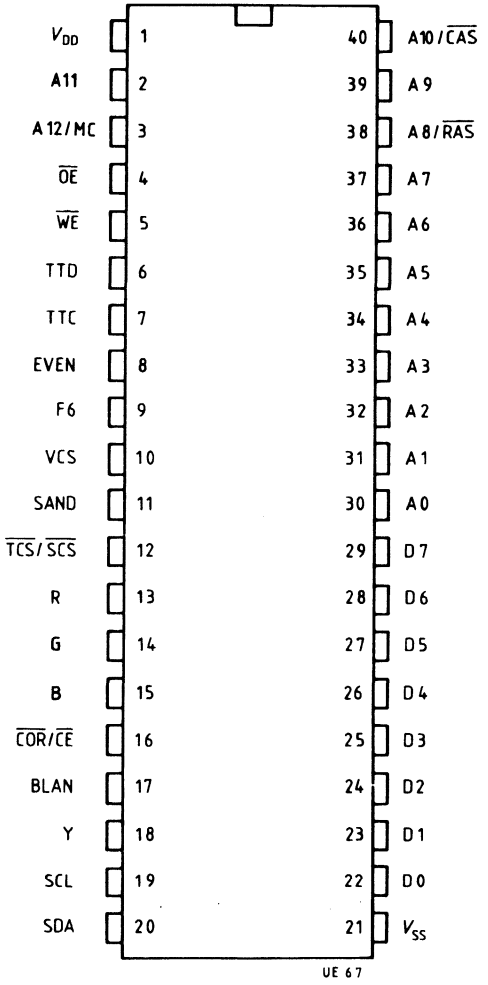
Functional Description

The Teletext Processor SDA 5243-2 contains six function blocks (**see block diagram**):

- Control with timing and system clock
- Data acquisition
- Memory interface
- Character generator
- I^2C bus
- Refresh generator and synchronisation

Teletext data and clock signals from the data slicer SDA 5231-2 are transferred to the TT-processor via pins TTD and TTC. The required data are selected in the acquisition section and stored in the external RAM via the memory interface. The data read from the RAM passes through the memory interface to the character generator, where they are transformed into corresponding R, G, B signals for the video output stages. Further output signals produced include a blanking signal BLAN, a contrast reducing signal $\overline{COR}$ and a text signal Y for an external printer. 14 registers can be written and 1 register can be written and read over via the I^2C bus (**diagram 5 and 6**).

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function	Description
1	V_{DD}	+ 5 V	
2, 3	A11, A12/MC	RAM Address/ Mux-Control	When pin 3 connected to V_{SS} Address multiplex
4	$\overline{OE}$	Output Enable	RAM control signal (active low)
5	$\overline{WE}$	Write Enable	RAM control signal (active low)
6	TTD	Teletext Data	From data slicer SDA 5231-2
7	TTC	Teletext Clock	6.9375 MHz from data slicer SDA 5231-2
8	EVEN	EVEN Field	Field status output
9	F6	System Clock	6 MHz from data slicer SDA 5231-2
10	VCS	Video Composite Synch	Sync signal from SDA 5231-2. Derived from video signal
11	SAND	SANDCASTLE	Three-level signal for SDA 5231-2 for synchronization of F6 and colour burst blanking
12	$\overline{TCS}$/ $\overline{SCS}$	Text Composite Synch/Scan Composite Synch	Synchronization output during text reproduction or synch input for vertical display timing
13, 14, 15	RGB	Red, Green, Blue	Open-drain-video output signal for TV output stages
16	$\overline{COR}/\overline{CE}$	Contrast Reduction Chip Enable	Open-drain-video output signal for contrast reduction; otherwise chip enable for quasi-static memory with 8 bit organization. I^2C bus programmable
17	BLAN	Blanking	Blanking signal open drain output
18	Y	Character foreground	Open-drain-video output signal for black/white display or printer
19	SCL	Serial clock	I^2C bus clock input
20	SDA	Serial data	Bidirectional I^2C bus data port
21	V_{SS}	Ground	
22–29	D0-D7	RAM Data	Tristate bidirectional data port
30–40	A0-A10	RAM Address	Operation with static and dynamic memories with 8-bit organization
38, 40	$\overline{RAS}$, $\overline{CAS}$	Address control	Multiplex operation for memories having 4-bit organization (active low), when pin 3 is shorted to V_{SS}.

Circuit Description

Data Acquisition

The SDA 5243-2 meets all the requirements of the present teletext standard.

Data arriving at the TTD pin are accepted as teletext data as soon as the start code (**diagram 1**) appears within the data entry window. All bytes are checked for odd parity errors and 1-bit errors are corrected in the bytes with hamming protection. The parity check for the data bytes can be disabled for reception of 8-bit data without parity. The following acquisition features are available:

- Automatic data font changeover to one of 6 languages by transmitted control bits, an independent selection of language groups via the I²C bus (**diagrams 7 and 9**) is possible.
- Data reception during lines 2 through 22 (or 315 to 335) in each half frame.
- Data reception in all lines of a full frame by switching over to full-channel operation. In full-channel operation it has to be observed that the automatic erase function is only partially available, hence all lines of every page must be transmitted in sequence or the whole page erased by software.
- Memory control for storage of up to 8 pages of teletext; 4 pages are sought simultaneously and when received are transferred into the selected memory bank.
- In the "don't care" mode, pages can be sought whose page numbers are not precisely known by inserting a don't care bit in place of the unknown number. This causes a search for all numbers between 0HEX and FHEX at the indicated location, (**diagram 5, register 3**).
- Capability of receiving supplementary information (ghost rows) which can be processed in a microcomputer. This allows reception of 24 virtual lines per page in addition to the normal text lines, and 2 Kbytes of memory are needed to store one page (**diagram 2b**).
- The transmitted clock time is directly written into the page memory selected for display on the TV screen.
- Automatic erasing of stored pages for standard teletext.
- Erasure of single pages by software command.
- Rolling page number during search.

Features

The character generator provides 192 alphanumeric characters and 2 x 64 graphics symbols in a raster comprising 12 horizontal and 10 vertical points. The various display possibilities can be selected by means of 32 control characters contained in the text (**diagrams 7-10**).

6 languages are automatically selected by the transmitted page header control bits C12, C13, and C14 (**diagram 3,** line 25, byte 7) in standardized 7-bit operation. In addition the capability exists in 8-bit operation to select nearly all characters independently of the control bits (**diagram 7**) using the I²C bus Register 0.

Teletext signals R, G, B, Y, Blank, and $\overline{\text{COR}}$ are available at the open-drain outputs. The $\overline{\text{COR}}$ signal allows a software-controlled contrast reduction for mixed mode operation. The Y signal reproduces only the teletext character plane without colour information and does not have a flash function.

Diagram 11 shows the active display area.

Additional Features include

- User-controllable character-height doubling with top/bottom selection.
- Status information above or below the main text.
- Insertion of all control, graphics or alphanumeric characters in the 24 standard rows and in one extra status row is possible via the I²C bus. By doing so the selected position of the character can be made visible by means of a cursor.

Timing

The internal system clock is derived from the 6-MHz clock F6 provided by the data slicer SDA 5231-2. The input F6 is AC coupled internally.

Vertical synchronization with the video signal occurs via the VCS input. The noise content of the VCS signal is reduced by integration. If the signal is too noisy or no synchronization can be achieved for other reasons the data acquisition is disabled.

The quality status of the VCS signals (VCSOK) is stored in I²C bus register 11B (**see diagram 6**). The microcontroller can interrogate the signal quality-bit.

If reg 0 bit d3 is set to 0, SDA 5243-2 is switched automatically to "free run" if signal-quality is too bad to synchronize the display-PLL without jitter. With bit d3=1 the free run-function is disabled and the PLL is always synchronized to CVBS-signal; but jitter will increase in bad conditions.

If reg 0 d3=1 bit d0 of register 11B indicates only the signal quality of the last line read in before reading I²C bus.

In the other case signal quality of the whole last field is indicated.

A detection circuit in the SDA 5243-2 recognizes the field frequency of the recieved VCS signal (50 Hz or 60 Hz) and the result is stored in I²C bus register 11B (**see diagram 6**).

The $\overline{\text{TCS}}$/$\overline{\text{SCS}}$ pin can be defined as an input via the I²C bus. 17 µs after the start of a line an internal signal is used to sample the input sync signal. (Refer to **diagrams 12 and 12 a**). The input signal has low distorsion and low noise in this mode.

The first change from "high" level to "low" level detected by this sampling process initiates the external vertical synchronization of this device.

To reduce the hardware expense for the synchronization of the display part by i.e. 60-Hz signals (NTSC) the vertical external synchronization of the integrated circuit can also be done via I²C bus through the VCS input (**see application circuit 3 b**).

In this case, the bit VCSTOSCS in I²C bus register 1, bit d7 (**see diagram 5**) must be set to 1. There is no requirement for an external switch including inversion for the $\overline{\text{SCS}}$ input. At the same time the 6-MHz clock signal F6 and due to this the internal system clock are always synchronized to the input signal. This does not depend on the signal quality of the input signal. Furthermore, the noise components of the sync signals are reduced by integration.

When the $\overline{\text{TCS}}$/$\overline{\text{SCS}}$ pin is switched as an output it deliners a synch signal (interlaced or non-interlaced) for the TV deflection circuit (**see application circuit 3 a**).

The SAND output delivers a three-level signal which contains the phase-lock signal PL and the colorburst blanking signal FBB. The PL signal synchronizes the 6-MHz clock in the SDA 5231-2. If for any reason, synchronization is not possible, the PL component of the SAND signal is not available in the output signal.

The field recognition output EVEN changes its state once per field. Using this signal it is possible to realize non-interlaced displays. The synchronization of the display can be derived from the acquisition or the display related circuits in the device. (e.g. in the after hour operation mode.)

The display locked synchronization mode can be selected by means of the I²C bus bit "VCS to SCS" set to (ref.: Register 1, G7 d/ = 1) or the I²C bus bits "external synchronization" (ref.: Register 1, bit d0 = d1 set to 1). Otherwise the display synchronization is locked to the acquisition circuit. The line or timing relation of the EVEN output signal can be seen from timing diagram 4. The detector for the first field can be switched off via the I²C bus bit Register 0 bit d2. The EVEN output will remain in "low" status after the detector is switched off.

Memory Interface

The following memory types can be connected to the SDA 5243-2 without additional external components:

- Static RAMs with nk × 8[1]) organization
- Dynamic RAMs with nk × 8[1]) organization
- Pairs of dynamic RAMs both with nk × 4[1]) organization and multiplexed address control. When this memory is used, pin 3 must be connected to V_{SS}

[1]) n ≤ 8

The refresh for the dynamic memory occurs automatically during colorburst blanking. The circuit configurations for the different memory types are shown in the **application circuits 1 and 2.**

Organization of the Page Memory

The external page memory is subdivided into 8 CHAPTERs of 1 Kbyte each, which are numbered 0 through 7.

The CHAPTERs are selected via the I²C bus register 8 (**diagram 6**). The ACTIVE CHAPTER-bits A0 to A2 in register 8 directly control the address pins A10 to A12, where A12 switches between BANK 0 (CHAPTER 0-3) and BANK 1 (CHAPTER 4-7).

Bytes within a chapter are selected via the I²C bus with lines (I²C bus register 9) and columns (I²C bus register 10, **diagram 6**). The line and column addresses are automatically converted in the memory interface into the corresponding 10-bit RAM address (A0 to A9).

Each CHAPTER contains 23 lines with 40 columns each for storing the normal teletext data (**diagram 2 a**). In addition it contains lines 0, 24 and 25. Line 0 is the page header. Line 24 is used to display status information from the control computer to the user. Line 25 contains information for the control computer and 14 bytes free for optional use.

In the ghost-row mode the visible lines are stored in CHAPTERS 0-3 and corresponding virtual lines in CHAPTERS 4-7. **Diagram 2 b** shows in which CHAPTER line a virtual line is stored.

On switch-on reset, the memories (not the dyn. 8 K × 8 RAMs) are erased except for CHAPTER 0, line 0, column 7, where "alpha-white" (0000 0111) is written. During operation, erasing is possible via I²C bus, but the erasing cycle requires up to 22 ms per page memory. As soon as the control bit C4 for one of the four pages being looked for is transmitted, this page is automatically erased. The actual state of C4 is stored in line 25 (**diagram 3**).

The write and read cycle both require 500 ns. The timing for the memory interface is given in the characteristics and in the **timing diagram 5**.

I²C bus

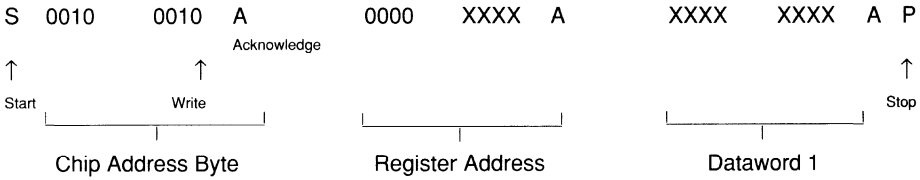
Organization of the I²C bus registers | 00 10 001 R/$\overline{W}$ | Component address

When the supply voltage is connected, a switch-on-reset is performed. The bus lines SDA and SCL are released. Registers 0-4 and 7-11 are set to 0000 0000, registers 5 and 6 to 0000 0011.

The device functions as slave-transmitter and slave-receiver. Registers R0 to R10 can be written only, register R11 can be written and read (**diagrams 5 and 6**).

Each reserved bit must be set to "0".

Write



Read

In several registers, an auto-increment of the register or column address occurs after each byte is written. For example, when register 1 is addressed, the data in register 1, register 2 and the column selected by register 2 in register 3 are written, and an auto-increment of the column addresses 0-6 takes place in R3, i.e. 9 data bytes can follow directly after the register address 1.

The bits are numbered in the reverse order of the I²C bus data.

Register 0 Register Address 0000 0000 "Pin function switch"

Bit	Function	Comment
d7-d4		reserved
d3	0 = normal operation 1 = no free run	no self synchronization in worse signal conditions
d2	0 = EVEN-pin active 1 = EVEN pin = 0 V	
d1	0 = pin 16 is $\overline{COR}$ output 1 = pin 16 is $\overline{CE}$ output	no automatical erasing of dyn. 8 K = 8 RAMs during power-on reset
d0	0 = register 11 A is selected 1 = register 11 B is selected	

After a write in register 0, the register address is increased to 1.

Register 1 Register Address 0000 0001 "Setting the operational mode"

Bit	Function	Comment
d7	0 = normal operation 1 = VCS T0 SCS	for 60 Hz display mode
d6	0 = acquisition of 7 bit and parity bit 1 = acquisition of 8 bit datawords	parity check of TTX data no parity check
d5	0 = acquisition ON, 1 = acquisition OFF	
d4	1 = enable GHOST ROWS	reception of lines 25 to 30
d3	0 = DEW 2–22, 1 = full channel operation	DEW = data entry window for line 2-22
d2	1 = TCS ON	$\overline{TCS}$/$\overline{SCS}$ pin is sync output
d1/d0	00 = 312/313 lines – MIX-mode	with interlace
d1/d0 d1/d0	01 = 312/313 lines – TEXT-mode 10 = 312/312 lines – TERMINAL-mode	without interlace without interlace is inhibited in news flashes and subtitles
d1/d0	11 = external synchronization	$\overline{TCS}$/$\overline{SCS}$ pin is an input

After a write in register 1, the register address is increased to 2.

Register 2 Register Address 0000 0010 "Page Mode Selection"

Bit	Function	Comment
d7		not used
d6	0 = page memory 0-3 1 = page memory 4-7	BANK selection
d5/d4	00 = page memory 0 or 4	register 3 selection, ACQCCT0
d5/d4	01 = page memory 1 or 5	register 3 selection, ACQCCT1
d5/d4	10 = page memory 2 or 6	register 3 selection, ACQCCT2
d5/d4	11 = page memory 3 or 7	register 3 selection, ACQCCT3
d3	1 = TB 0 = normal operation	test bit
d2-d0	addressing of columns 0-6 in register 3	with address auto-increment

After a write to register 2 the register address is increased to 3.

Register 3 Register Address 0000 0011 "Page Request Data"

This register contains 7 columns. The column address last written to register 2 is accessed. After every data word the column address in register 2 is auto-incremented and the next data word is written to the next column address.

Column Address 000 to 110

Bits d5-d7 are not evaluated.

Column Address	Bit d4	Bit d3	Bit d2	Bit d1/d0
	1 = do care			
000	magazine number	$\overline{\text{HOLD}}$ *)	magazine number	
001	tens position	page number tens position		
010	units position	page number units position		
011	tens position	0	0	hour tens
100	units position	hour units		
101	tens position	0	minute tens	
110	units position	minute units		

*) $\overline{\text{HOLD}}$ = 0 Page contents are not updated.
During an uninterrupted access to register 3 the HOLD function is automatically performed.

Each page data acquisition controller ACQCCT 0-3 contains one register 3 **(diagram 5).** If more than one register 3 is programmed to acquire the same page, the page data acquisition with the lowest number has priority.

No auto-increment to register address 4.

Register 4 Register Address 0000 0100 "Display Chapter"

The address of register 4 has to be transmitted via the I^2C bus (no auto-increment from register 3).

Bit 3-7 are not evaluated.

Bits 0-2 is address of the page memory (No. 0 to 7) for display.

After a write to register 4 the register address is auto-incremented to 5.

Register 5 Register Address 0000 0101 "Display Control Normal, Inside and Outside Box"

Bit	Function	Comment
d7	0 = only foreground colors outside* 1 = foreground and background colors outside	has priority over "TV image outside"
d6	0 = only foreground colors inside* 1 = foreground and background colors inside	has priority over "TV image inside"
d5	0 = normal contrast 1 = contrast reduction outside	
d4	1 = contrast reduction inside	
d3	1 = text outside	
d2	1 = text inside	
d1	1 = picture outside	Defaults to 1
d0	1 = picture inside	Defaults to 1

* Inside: inside a teletext box area.

* Outside: outside a teletext box.

After a write to register 5 the register address is auto-incremented to 6.

Register 6 Register Address 0000 0110 "Display Control News Flash Subtitle"

Function analogous to register 5, valid only for news flashes and subtitles controlled by transmitted control bits C5 or C6.

Function control as in register 5.

After a write to register 6 the register address is increased to 7.

Register 7 Register Address 0000 0111 "Display Mode"

Bit	Function	Comment
d7	1 = status information in row 0 0 = status information in row 24	
d6	1 = cursor "ON" for position addressed in registers 9 and 10 0 = cursor "OFF"	cursor blinking is possible by repeated switching of d6
d5	0 = reveal function activated	after conceal display control character
d4/d3	01 = double character height, only lines 0-11 visible 11 = double character height, only lines 12-23 visible X0 = normal image	
d2	1 = box on attribute enable in line 24	
d1	1 = box on attribute enable in line 1-23	a 0 in d1 inhibits the display of flash messages and subtitles
d0	1 = box on attribute enable in line 0	

No auto-increment to register 8.

Register 8 Register Address 0000 1000 "Active Chapter"

The address of register 8 has to be transmitted via the I^2C bus (no auto-increment from register 7).
The bits 4-7 have no function.

Bit 3 1 = erasing memory contents of the addressed page. The bit is not stored. Within one frame period, the blanking code 0010 0000 is written to all memory positions of line 0, column 0 to line 25, column 23.

Bit 0-2 the page memory address 0 ... 7 for I^2C bus access.

After a write to register 8 the register address is auto-incremented to 10.

Register 9 Register Address 0000 1001 "Active Row"

Bits 5-7 without function.

Bits 0-4 selection of rows 0-25 in page memory.

Auto-increment of row address. Row 23 is followed by row 0. Row 24 and 25 can only be selected directly.

After a write to register 9 the register address is auto-incremented to 10.

Register 10 Register Address 0000 1010 "Active Column"

Bits d6 and d7 without function.

Bits d0-d5 selection of columns 0-39 in page memory.

An auto-increment of the column address follows each write of a data byte to register 11. Column 39 followed by column 0 and an auto-increment of the line address in register 9.

After a write to register 10 the register address is auto-increment to 11.

Register 11 A Register Address 0000 1011 and Register 0, d0 = 0 "Active Data"

Data Bit	**d7**	**d6**	**d5**	**d4**	**d3**	**d2**	**d1**	**d0**
Alpha-numeric and control characters	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1

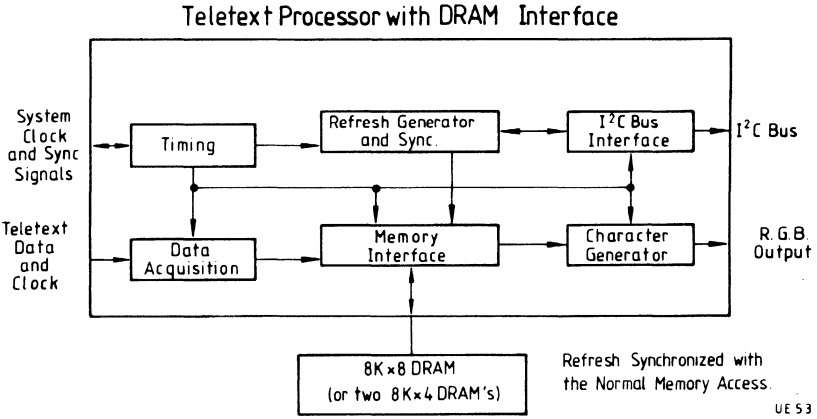
After writing a data byte, the column address is auto-incremented for the next data byte. After reading a data byte the position of the next byte to be read is automatically selected, if the last write command selected automatically the register 11, or if the last write command created an auto-increment from register 10 to register 11.

Register 11 B Register Address 0000 1011 and Register 0, d0 = 1 "Status Register"

B4	**Function**	
d7	0 = 50 Hz VCS signal available 1 = 60 Hz VCS signal available	
d6-d1	0	
d0	0 = VCS signal is interferred, self synchronization 1 = VCS is ok, external synchronization is possible	reg 0, d3=0
	0 = last VCS-line interferred 1 = VCS is ok or no sync-pulses found	reg 0, d3=0

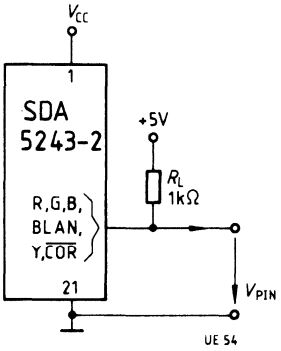
Write access to register 11 B is impossible, if write access with the address 11 B is attempted as a direct write access to the page memory by means of register 11A.

Block Diagram

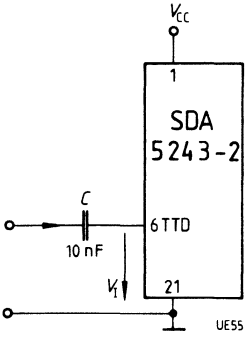


Test Circuits

Test Circuit 1



Test Circuit 2



Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{DD}	– 0.3	6	V
Voltage at: VCS, SAND, SDA, SCL, EVEN D0 to D7, A0 to A12, OE, WE	V_{IN}	– 0.3	V_{DD}	V
TTC, F6	V_{IN}	– 0.3	11	V
TCS/SCS TTD	V_{IN}	– 0.3	8.5	V
R, G, B, BLAN, Y, COR/CE	V_A	– 0.3	6.5	V
Ambient temperature	T_A	– 20	70	°C
Storage temperature	T_{stg}	– 20	125	°C
Power dissipation	P_D		1.1	W

Operating Range

Supply voltage	V_{DD}	4.5	5.5	V
Ambient temperature	T_A	0	70	°C

Characteristics

T_A = 25 °C (all voltages referenced to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit/ Timing Diagram
		min.	typ.	max.			
Supply voltage	V_{DD}	4.5	5	5.5	V		
Supply current	I_{DD}	80	130	190	mA	without load F6 = 6 MHz	
Inputs TTC and F6							
Input voltage	V_{IP}	– 0.3		10	V	min. and max. values	–/1
Input signal	$V_{I\,pp}$	1		7	Vpp		–/1
Input leakage current	I_I			20	µA	V_I = 0–10 V	
Input capacitance	C_I			7	pF		
Input frequency	f_{TTC}	4	6.9375	8	MHz		
Input frequency	f_{F6}	4	6.0	8	MHz		
Rise and fall times	t_r, t_f	10		80	ns		–/1
Input TTD							
Input signal	$V_{I\,pp}$	2		7	Vpp		2/2
Input leakage current	I_I			20	µA	V_I = 0–8 V	
Input capacitance	C_I			7	pF		
Rise and fall times	t_r, t_f	10		80	ns		2/–
Ext. coupling capacitor	C_{ext}		50		nF		
Input VCS							
L – input voltage	V_{IL}	0		0.8	V		
H – input voltage	V_{IH}	2		V_{DD}	V		
Input leakage current	I_I			10	µA	V_I = 5.5 V	
Input capacitance	C_I			7	pF		
Rise and fall times	t_r, t_f			500	ns		
Inputs SCL, In/Output SDA							
L – input voltage	V_{IL}	0		1.5	V		
H – input voltage	V_{IH}	3		V_{DD}	V		
Input leakage current	I_I			10	µA	V_I = 5.5 V	
Input capacitance	C_I			7	pF		
Input frequency	f_{SCL}			100	kHz		
Rise and fall times	t_r, t_f			2	µs		
Max. capacitor of bus	C_{max}			400	pF		
Fall time (acknowledgement)	t_f			0.2	µs	from 3 to 1 V	
SDA acknowledgement	V_{AL}	0		0.5	V	I_{AL} = 3 mA	

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit/ Timing Diagram
		min.	typ.	max.			
In/Output TCS/SCS							
Input signal SCS						TCS = high impedance	
L - input voltage	V_{IL}	0		1.5	V		
H - input voltage	V_{IH}	3.5		8	V		
Input capacitance	C_I			7	pF		
Input leakage current	I_I			10	µA	V_I = 8 V	
Rise and fall times	t_r, t_f			500	ns		
Output Signal TCS							
L - output voltage	V_{QL}	0		0.4	V	I_{QL} = 1.6 mA	
H - output voltage	V_{QH}	2.4		V_{DD} 5.5	V V	$-I_{QH}$ = 0.2 mA I_{QH} = 0.1 mA	
Load capacitance	C_L			50	pF		
Rise and fall times	t_r, t_f			100	ns	between 0.6 and 2.2 V	
RAM - Data Interface D0-D7							
(Tri-State port) L - input voltage	V_{IL}	0		0.8	V		
H - input voltage	V_{IH}	2		V_{DD}	V		
Input leakage	I_I			10	µA	V_I = 5.5 V	
Input capacitance	C_I			7	pF		
L - output voltage	V_{QL}	0		0.4	V	I_{QL} = 1.6 mA	
H - output voltage	V_{QH}	2.4		50	ns	$-I_{QH}$ = 0.2 mA	
Rise and fall times	t_r, t_f			50	ns	between 0.6 and 2.2 V, output active	
Load capacitance	C_L			120	pF		
Output EVEN							
L - output voltage	V_{QL}	0		0.4	V	I_{QL} = 1.6 mA	
H - output voltage	V_{QH}	2.4		V_{DD}	V	$-I_{QH}$ = 0.2 mA	
Rise and fall times	t_r, t_f			100	ns	between 0.6 and 2.2 V	
Load capacitance	C_L			50	pF		

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit Timing Diagram
		min.	typ.	max.			
Output SAND							
L - output voltage	V_{QL}	0		0.25	V	I_{QL} = 0.6 mA	
Intermediate level	V_{QM}	1.1		2.9	V	$\pm I_{QM}$ = 30 µA	–/3
H - output voltage	V_{QH}	4.0		V_{DD}	V	$-I_{QH}$ = 30 µA	
Rise time	t_{r1}			400	ns	between 0.4 and 1.1 V	
	t_{r2}			200	ns	between 2.9 and 4 V	
Fall time	t_f			50	ns	between 4 and 0.4 V	
Load capacitance	C_L			30	pF		
RAM - Address Outputs $\overline{OE}$, $\overline{WE}$, A0-A12, ($\overline{RAS}$), ($\overline{CAS}$), $\overline{CE}$*							
L - output voltage	V_{QL}	0		0.4	V	I_{QL} = 1.6 mA	
H - output voltage	V_{QH}	2.4		V_{DD}	V	$-I_{QH}$ = 0.2 mA	
Rise and fall times	t_r, t_f			50	ns	between 0.6 and 2.2 V	
Load capacitance	C_L			120	pF		
Outputs R, G, B, BLAN, Y, $\overline{COR}$							
Open-Drain-Outputs L - output voltage	V_{QL}	0 0		0.4 1	V V	I_{QL} = 2 mA I_{QL} = 5 mA	
H - output voltage	V_{QH}	4.9		V_{DD}	V	R_L = 1 kΩ to 5 V	
Fall time	t_f				ns	R_L = 1 kΩ to 5 V V_{pin} = 4.5 → 1.5 V	
Fall delay	t_d			20	ns	with R_L = 1 kΩ to 5 V at V_{pin} = 3 V	1/–
Output leakage	I_Q			20	µA	V_Q = 5 V	
Load capacitance	C_L			25	pF		

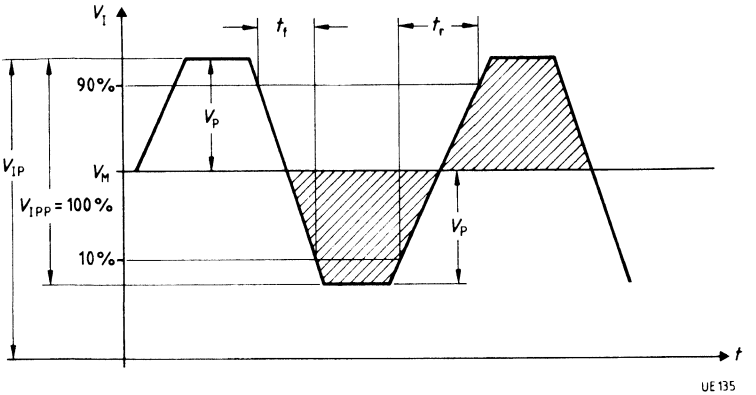
*) The pins in parenthesis are valid in multiplex operation (pin 3 at Vpp).

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test	Test Circuit/ Timing Diagram
		min.	typ.	max.			
Timing for Memory Interface							
Cycle time	t_{RC}, t_{WC}		500		ns		–/5a
Delay address to OE	t_{OE}	60			ns		–/5a
Address valid	t_{AH}	450	500		ns		–/5a
OE duration	t_{OEL}	320			ns		–/5a
Data setup time	t_{AC}			200	ns		–/5a
Data hold time to address	t_{DH}	0			ns		–/5a
WE delay	t_{WE}	40			ns		–/5a
WE duration	t_{WEL}	200			ns		–/5a
Data setup time	t_{DS}	100			ns		–/5a
Data hold time to address	t_{OH}	20			ns		–/5a
Addr. hold time after	t_{WR}	25			ns		–/5a
WE to tristate	t_{OHZ}			230	ns		–/5a
Tristate to WE	t_{ZDS}	80			ns		–/5a
Pulse duration CE	t_{CEL}	320			ns		–/5b
Cycle time CE	t_{CEC}	450			ns		–/5b
Pulse duration RAS	t_{RAL}	320			ns		–/5c
Pulse duration CAS	t_{CAL}	120			ns		–/5c
Cycle time RAS	t_{RAC}	450			ns		–/5c
Cycle time CAS	t_{CAC}	450			ns		–/5c
Delay WE/OE RAS	t_{RWL}		50		ns		–/5c

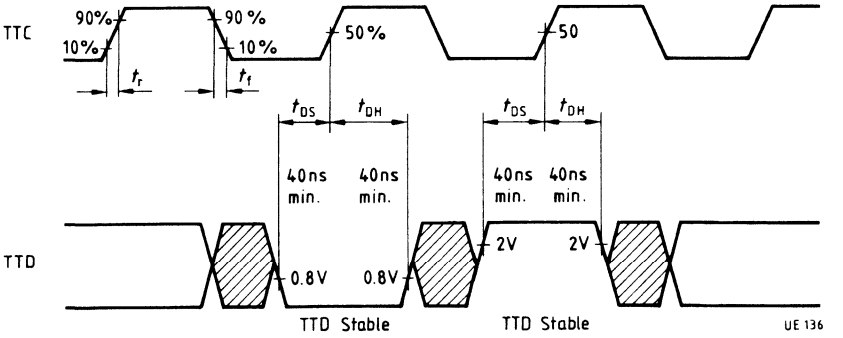
*) The pins in parenthesis are valid in multiplex operation (pin 3 at Vpp).

Timing Diagram 1

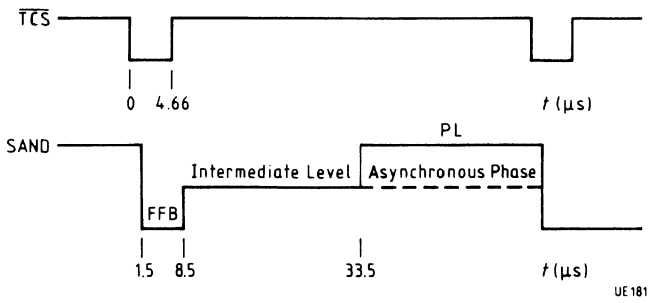


V_M = 50 % Line Giving Equal Areas

Timing Diagram 2



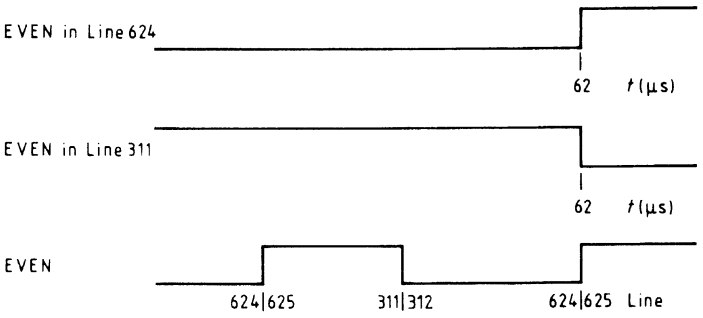
Timing Diagram 3



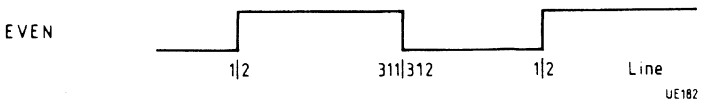
Timing Diagram 4a

EVEN Signal synchronized by the Aquisition Circuit

a) VCS with 50Hz Field Repetition Rate



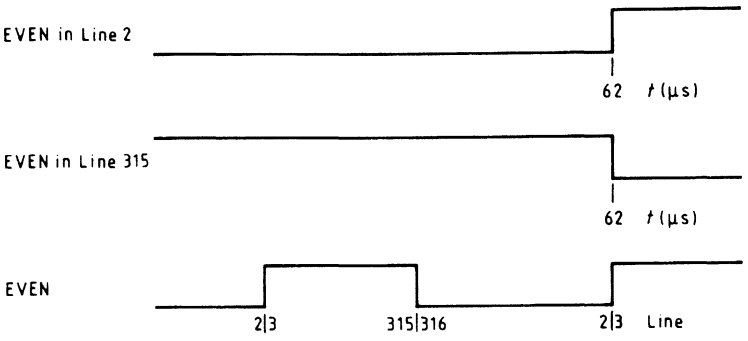
b) VCS with 60Hz Field Repetition Rate



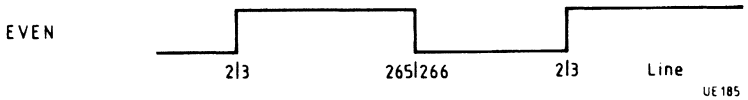
Timing Diagram 4b

EVEN Signal, synchronized by the Display Circuit:

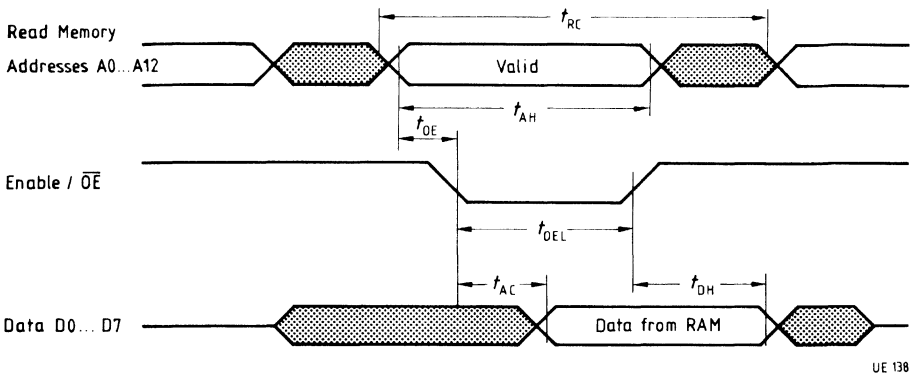
a) VCS with 50 Hz Field Repetition Rate

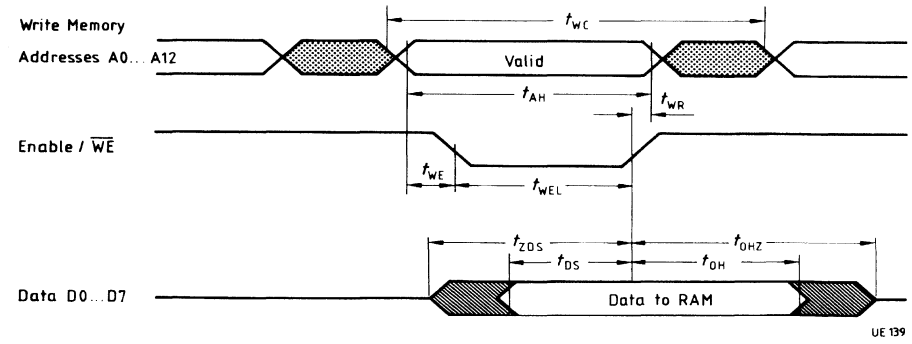


b) VCS with 60 Hz Raster alternating Frequency



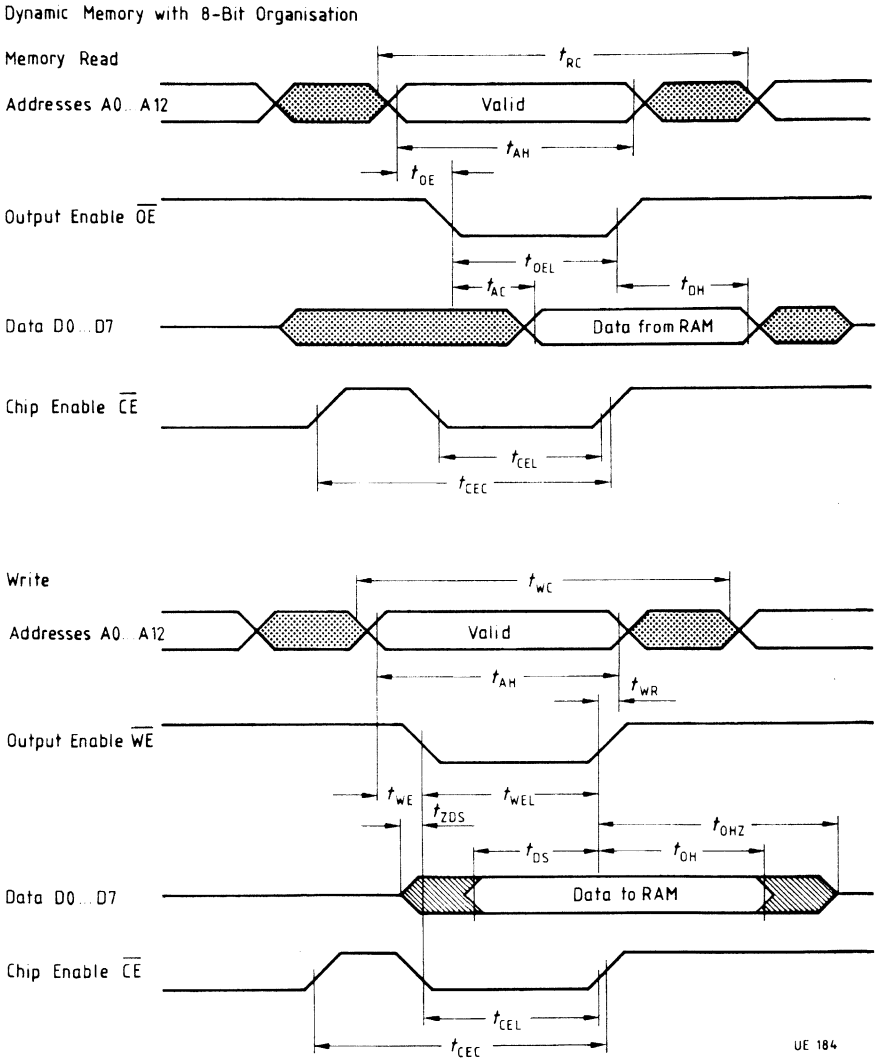
Timing Diagram 5a
Memory Interface Timing





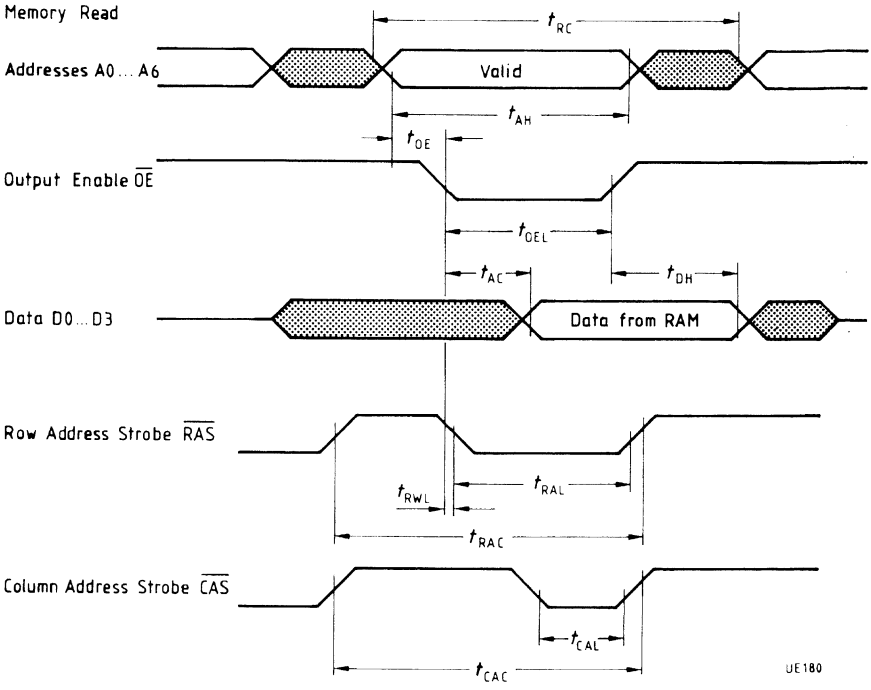
Timing Diagram 5b

Memory Interface Timing



Timing Diagram 5c
Memory Interface Timing

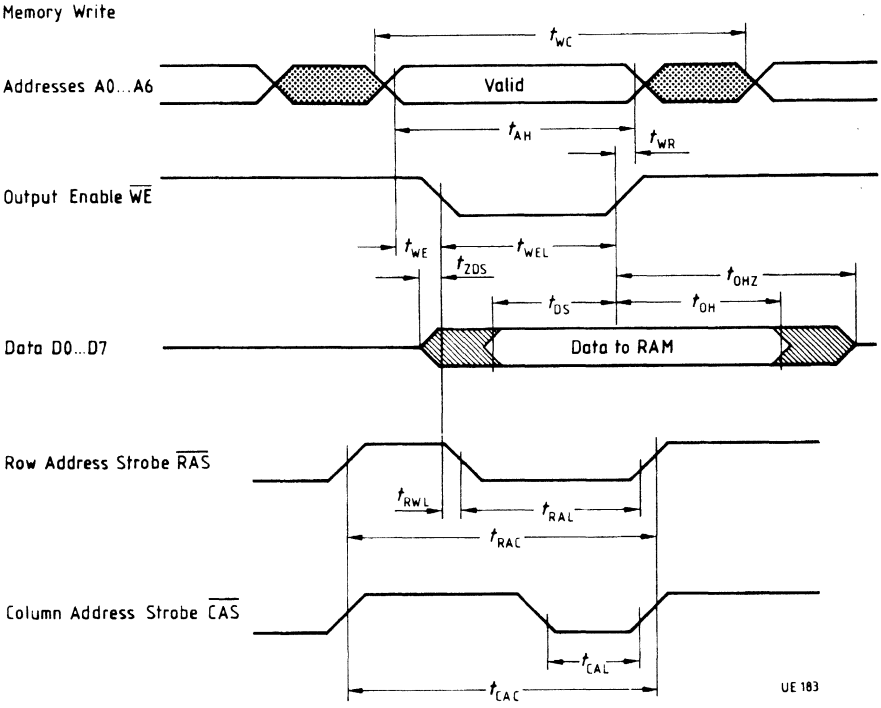
Dynamic RAM with 4-Bit Organisation



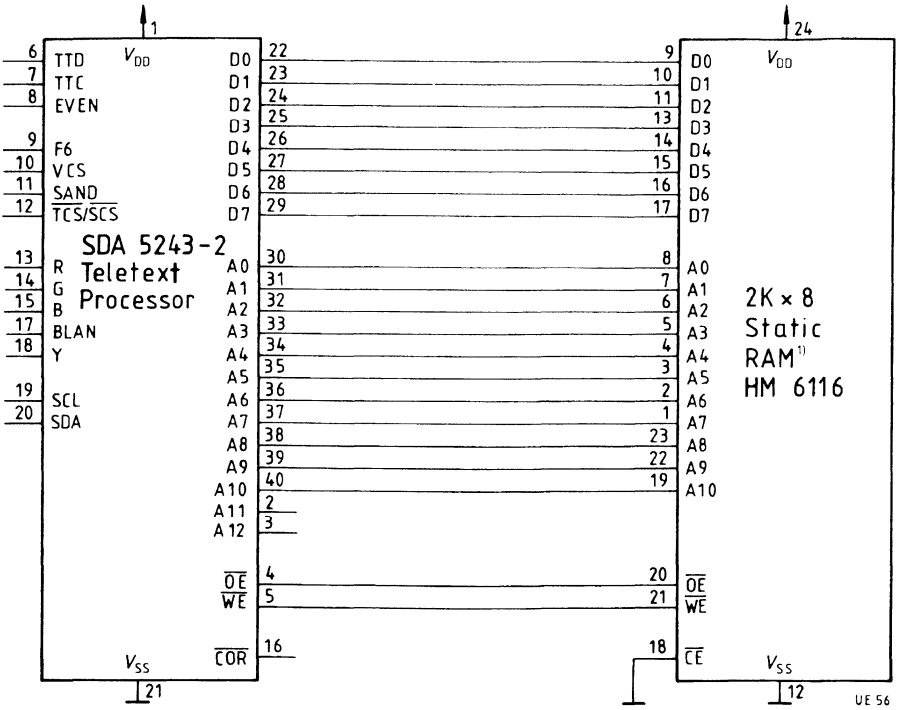
Timing Diagram 5d

Memory Interface Timing

Dynamic RAM with 4-Bit Organisation

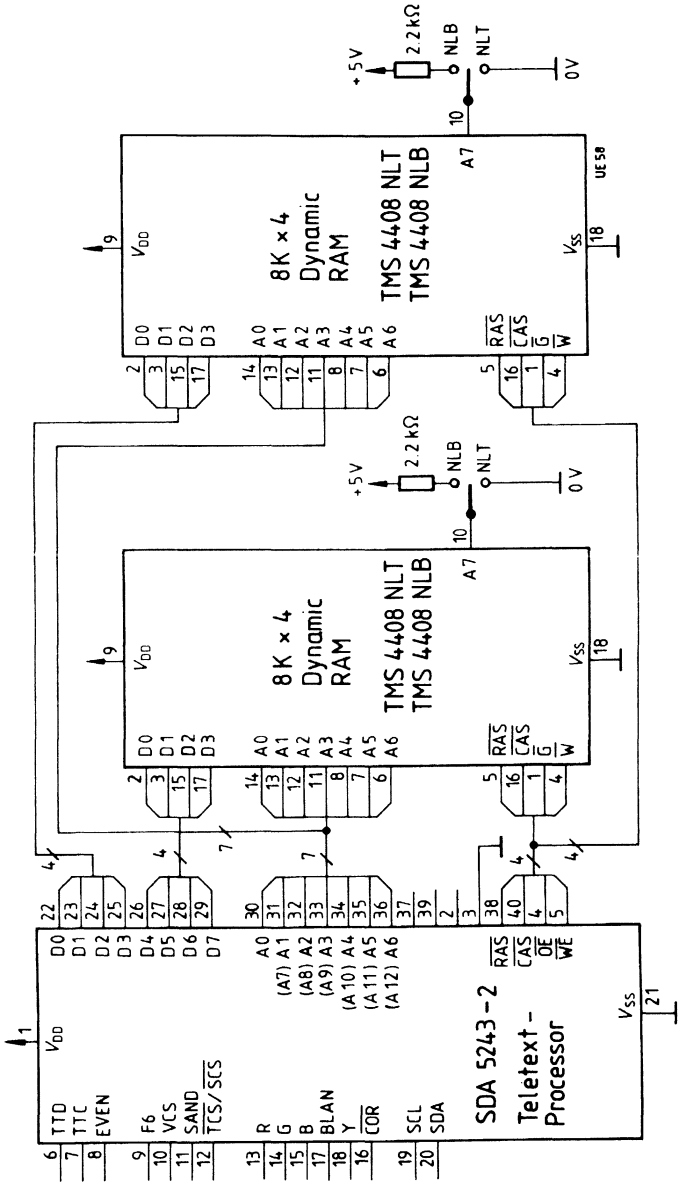


Application Circuit 1

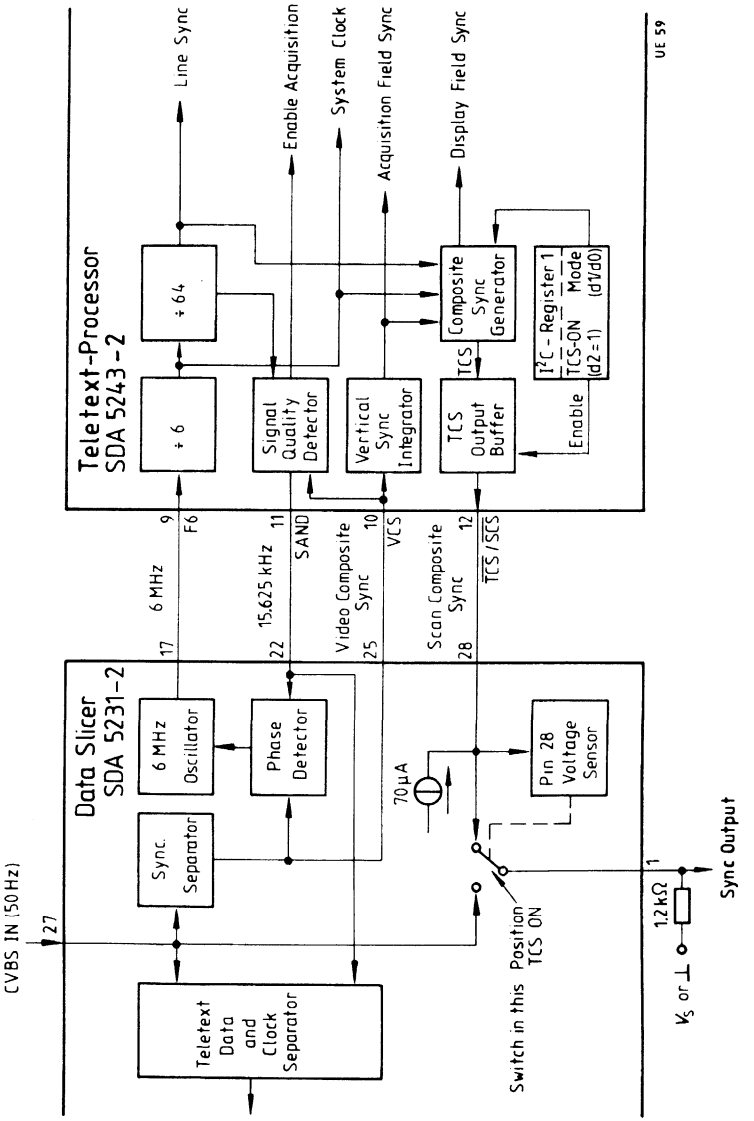


1) Memories up to 8K × 8 can be addressed using A11 and A12. Connection as 8K × 8 Dyn RAM

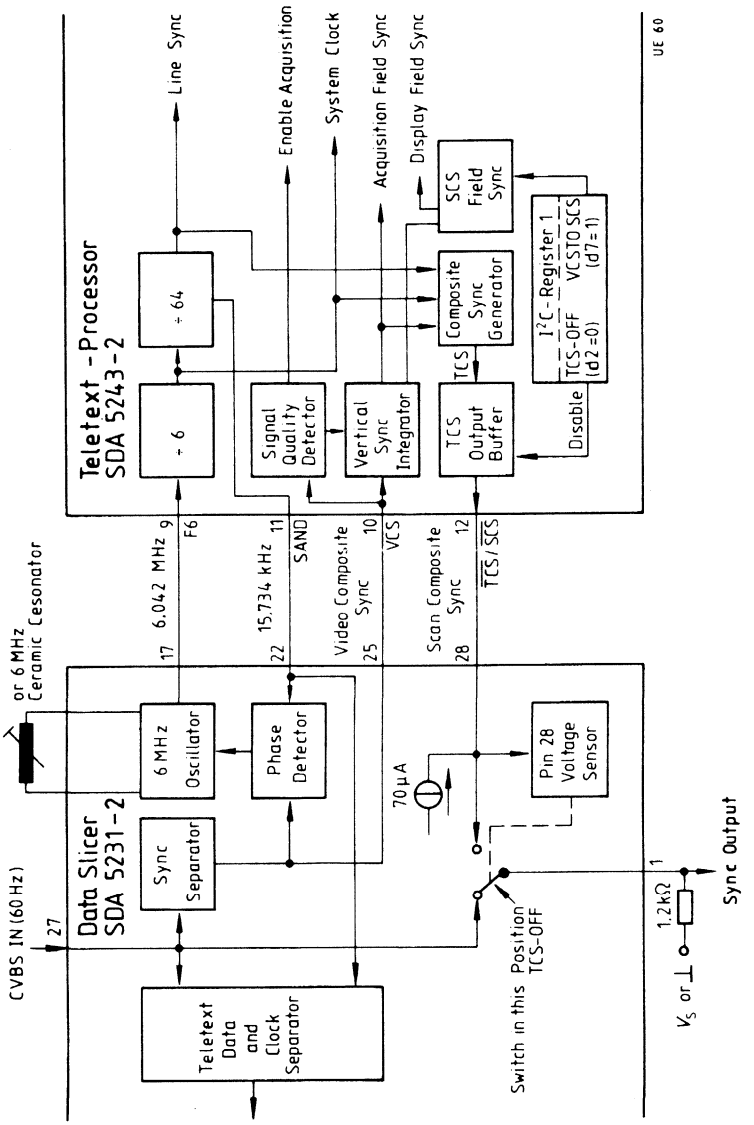
Application Circuit 2



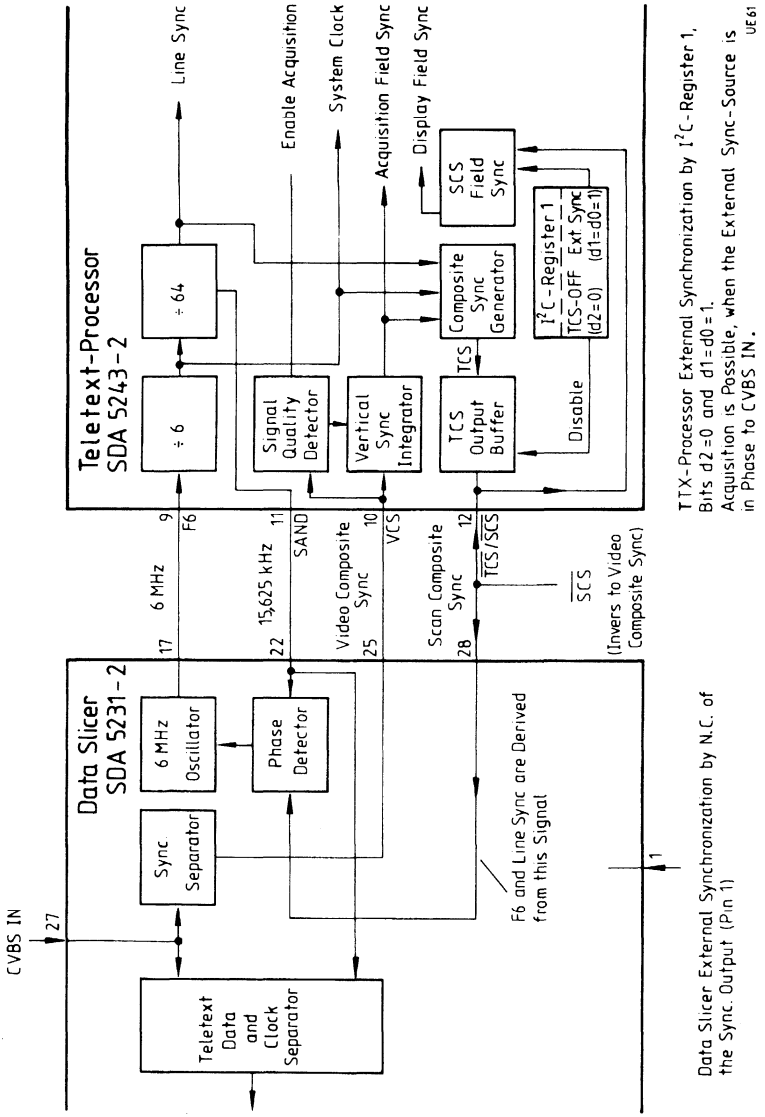
Application Circuit 3a



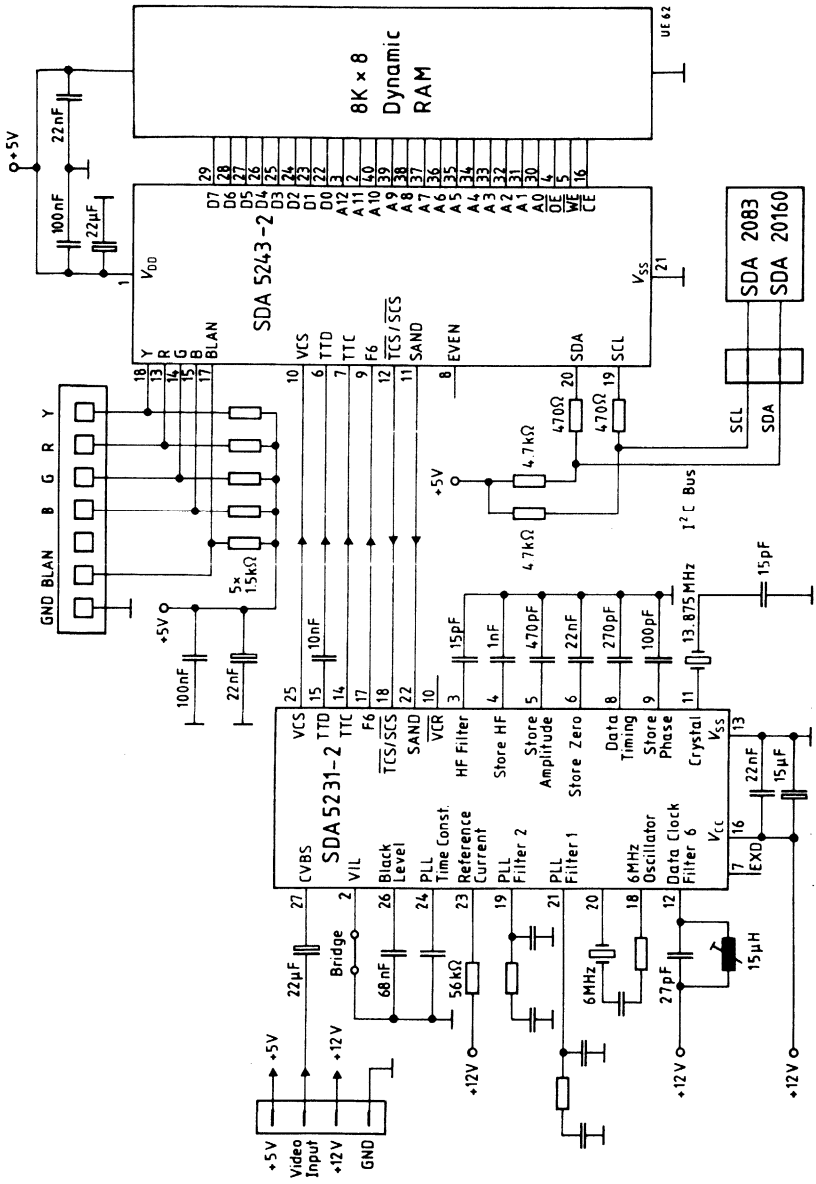
Application Circuit 3b



Application Circuit 3c



Application Circuit 4



Application Circuit 5

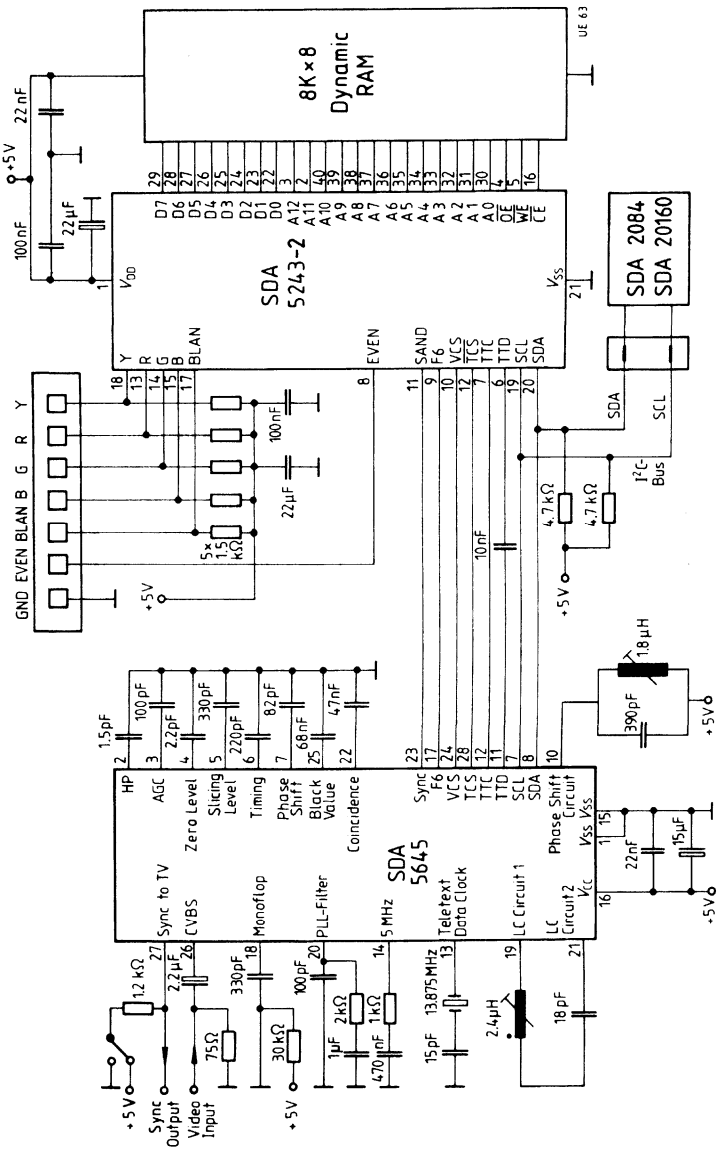


Diagram 1

Teletext Input Signal (Line 2 to 22 and 315 to 335)

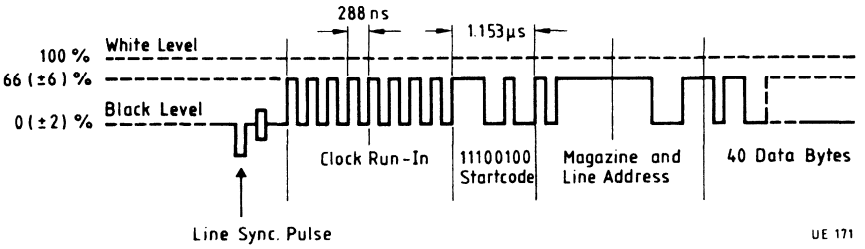


Diagram 2a

Page Memory Organization

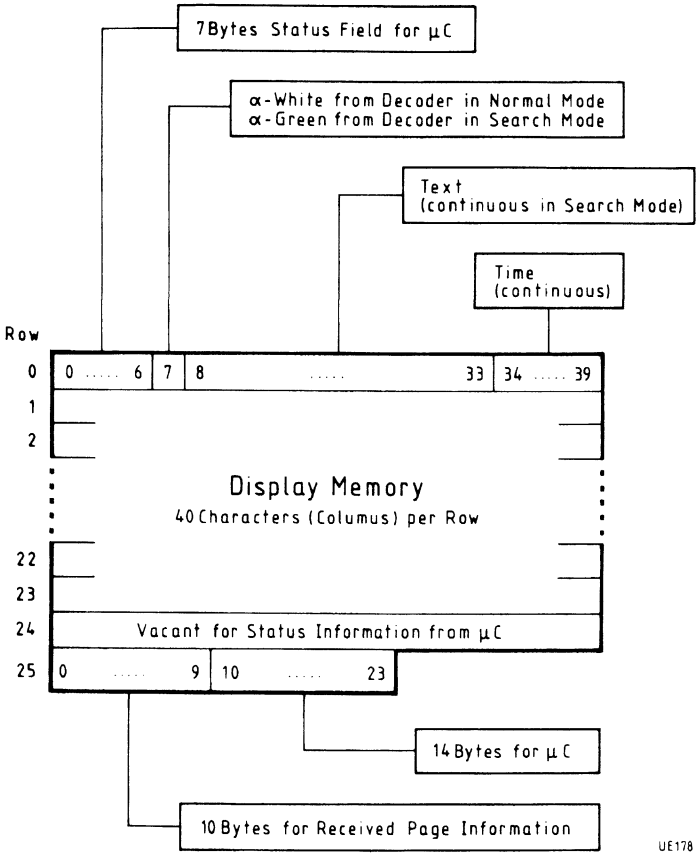
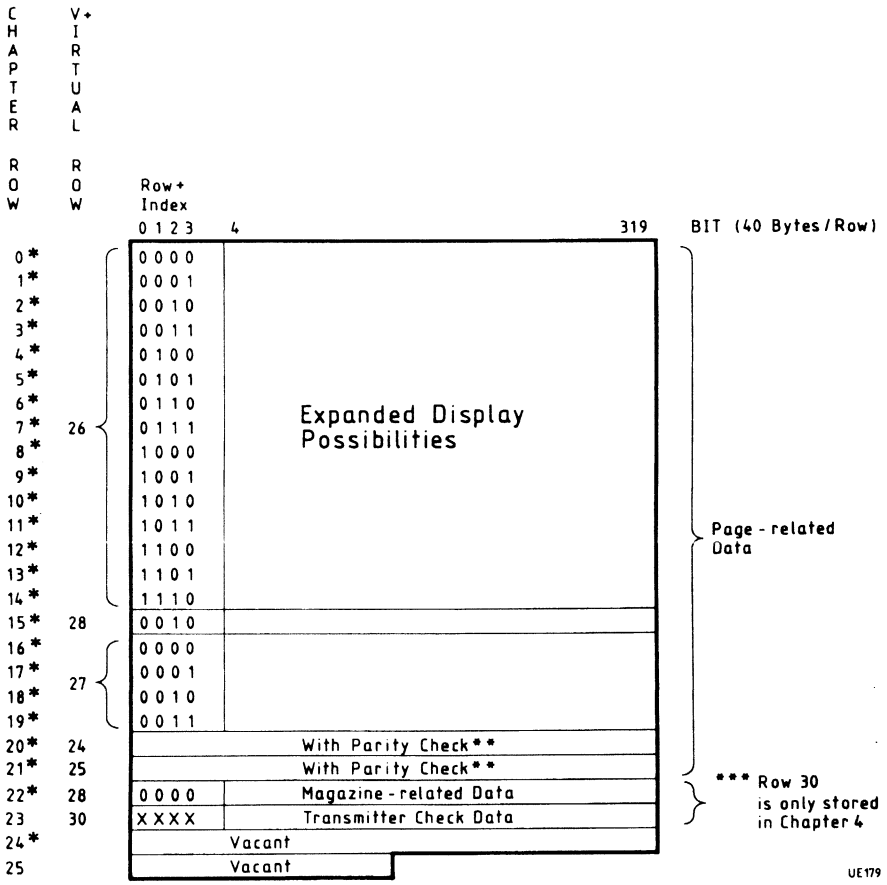


Diagram 2b

Virtual Page (Ghost Rows)**



\+ Packet

* Automatic erasable lines wit RESET, CLEAR MEMORY or control bit 4

*** In 7-bit mode (register 1) the marking bytes are checked ODD-parity and MSB is set to 0. Defective bytes are not taked over in the page memory.

Diagram 3

Page Memory Organization

Line 25, Bytes 0 ... 9

Byte	Data Bits							
	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	HA	PU3	PU2	PU1	PU0
1	0	0	0	HA	PT3	PT2	PT1	PT0
2	0	0	0	HA	MU3	MU2	MU1	MU0
3	0	0	0	HA	C4	MT2	MT1	MT0
4	0	0	0	HA	HU3	HU2	HU1	HU0
5	0	0	0	HA	C6	C5	HT1	HT0
6	0	0	0	HA	C10	C9	C8	C7
7	0	0	0	HA	C14	C13	C12	C11
8	0	0	0	$\overline{\text{FOUND}}$	0	MAG2	MAG1	MAG0
9	0	0	PBLF	0	0	0	0	0

Information Bits

HA = HIGH, Hamming error found in corresponding column
$\overline{\text{FOUND}}$ = LOW, when a page has been found
PBLF = HIGH, page search in progress

Page Number

MAG = Magazine number 0-7 (000 ... 111)
PU = Page number units (0 ... 9)
PT = Page number tens (0 ... 9)
MU = Minute units
MT = Minute tens
HU = Hour units
HT = Hour tens

useable as additional page subcode

Control Bits

C4 = Erase page
C5 = News flash
C6 = Subtitle
C7 = Supress header
C8 = Update indicator
C9 = Interrupted sequence
C10 = Inhibit display
C11 = Serial magazine sequence
C12, C13, C14 = Character set selection

Diagram 4

Register Configuration

RAM Access Registers

	d7	d6	d5	d4	d3	d2	d1	d0	BIT
Register 4	*	*	*	*	*	A2	A1	A0	DISPLAY CHAPTER
Register 5	BACK-GROUND OUT	BACK-GROUND IN	CON-TRAST REDUC-TION OUT	CON-TRAST REDUC-TION IN	TEXT OUT	TEXT IN	PICTURE OUT	PICTURE IN	DISPLAY CONTROL NORMAL INSIDE AND OUTSIDE BOX
Register 6	BACK-GROUND OUT	BACK-GROUND IN	CON-TRAST REDUC-TION OUT	CON-TRAST REDUC-TION IN	TEXT OUT	TEXT IN	PICTURE OUT	PICTURE IN	DISPLAY CONTROL NEWSFLASH OR SUBTITLE
Register 7	STATUS ROW $\overline{\text{BTM}}$ TOP	CURSOR ON	$\overline{\text{CON-}}$ $\overline{\text{CEAL}}$ REVEAL	$\overline{\text{TOP}}$ BOTTOM	$\overline{\text{SINGLE}}$ DOUBLE HEIGHT	BOX ON IN	BOX ON IN	BOX ON IN	DISPLAY MODE

	d7	d6	d5	d4	d3	d2	d1	d0	BIT
Register 8	*	*	*	*	CLEAR MEMORY	A2	A1	A0	ACTIVE CHAPTER
Register 9	*	*	*	R4	R3	R2	R1	R0	ACTIVE ROW
Register 10	*	*	C5	C4	C3	C2	C1	C0	ACTIVE COLUMN
Register 11	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	ACTIVE DATA

*) Undefined register bits (not evaluated), must be set to "0".

Diagram 5

Register Configuration

	d7	d6	d5	d4	d3	d2	d1	d0	Bit
Register 0	*	*	*	*	NO FREE RUN	EVEN OFF	CE ON	SEL 11B	Mode 0
Register 1	VCS TO SCS	$\overline{7+P}$ 8 BITS	ACQ $\overline{ON}$/OFF	GHOST ROW ENABLE	$\overline{DEW}$ FULL FIELD	TCS	Sync-Mode 1	Sync-Mode 0	Mode 1
Register 2	•	BANK SELECT A2	ACQ CCT A1	ACQ CCT A0	TB	START ROW SR2	START ROW SR1	START ROW SR0	Page Request Address

4 X Register 3

d4	d3	d2	d1	d0	Bit	
DO CARE	$\overline{HOLD}$	MAG2	MAG1	MAG0	ROW 0 (MAGAZINE)	Page Request Data
DO CARE	PT3	PT2	PT1	PT0	ROW 1 (PAGE TENS)	
DO CARE	PU3	PU2	PU1	PU0	ROW 2 (PAGE UNITS)	
DO CARE	*	*	HT1	HT0	ROW 3 (HOURS TENS)	
DO CARE	HU3	HU2	HU1	HU0	ROW 4 (HOURS UNITS)	
DO CARE	*	MT2	MT1	MT0	ROW 5 (MINUTES TENS)	
DO CARE	MU3	MU2	MU1	MU0	ROW 6 (MINUTES UNITS)	

ACQ CCT0
ACQ CCT1
ACQ CCT2
ACQ CCT3

*) not defined, must be set to "0".

Diagram 6

Register Configuration

	d7	d6	d5	d4	d3	d2	d1	d0	BIT
Register 4	*	*	*	*	*	A2	A1	A0	DISPLAY CHAPTER
Register 5	BACK-GROUND OUT	BACK-GROUND IN	CON-TRAST REDUC-TION OUT	CON-TRAST REDUC-TION IN	TEXT OUT	TEXT IN	PICTURE OUT	PICTURE IN	DISPLAY CONTROL NORMAL INSIDE AND OUTSIDE BOX
Register 6	BACK-GROUND OUT	BACK-GROUND IN	CON-TRAST REDUC-TION OUT	CON-TRAST REDUC-TION IN	TEXT OUT	TEXT IN	PICTURE OUT	PICTURE IN	DISPLAY CONTROL NEWSFLASH OR SUBTITLE
Register 7	STATUS ROW $\overline{\text{BTM}}$ TOP	CURSOR ON	$\overline{\text{CON-}}$ $\overline{\text{CEAL}}$ REVEAL	$\overline{\text{TOP}}$ BOTTOM	$\overline{\text{SINGLE}}$ DOUBLE HEIGHT	BOX ON 24	BOX ON 1–23	BOX ON 0	DISPLAY MODE

RAM Access Registers

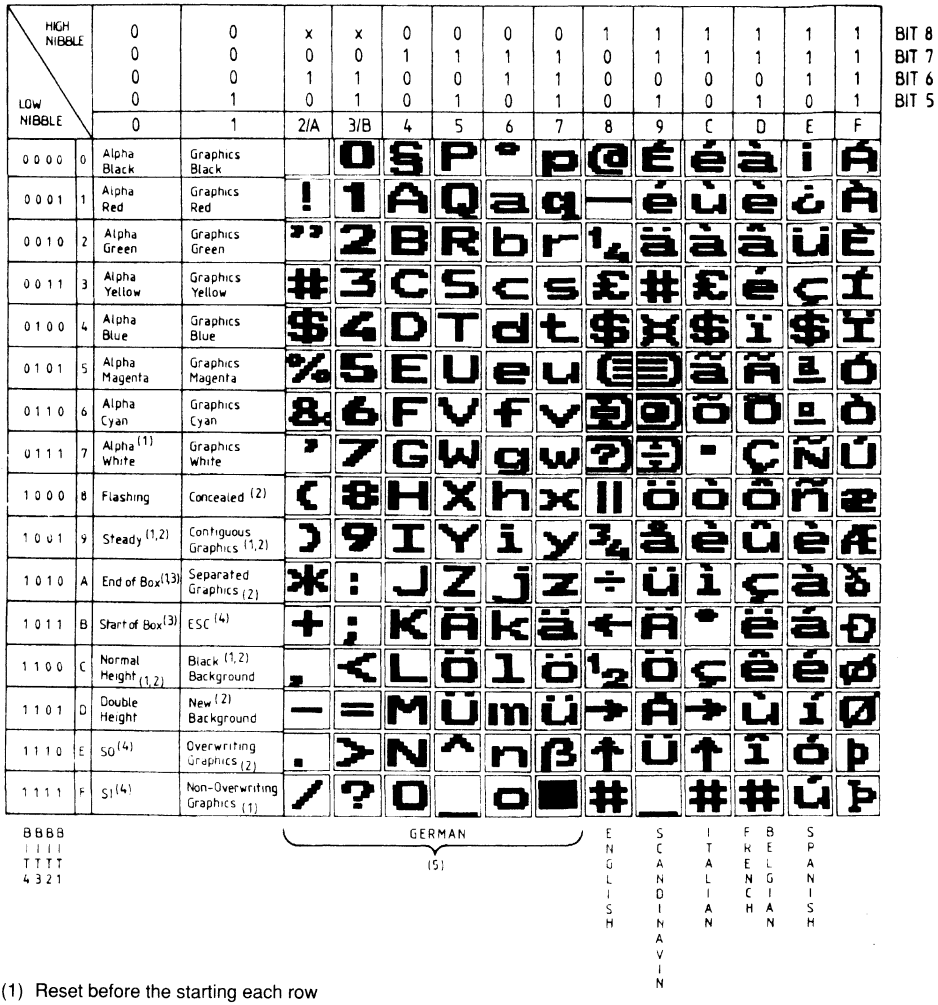
	d7	d6	d5	d4	d3	d2	d1	d0	BIT
Register 8	*	*	*	*	CLEAR MEMORY	A2	A1	A0	ACTIVE CHAPTER
Register 9	*	*	*	R4	R3	R2	R1	R0	ACTIVE ROW
Register 10	*	*	C5	C4	C3	C2	C1	C0	ACTIVE COLUMN
Register 11A	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	ACTIVE DATA
Register 11B	60 Hz	0	0	0	0	0	0	VCS0K	STATUS

*) not defined, must be set to "0"

Diagram 7

Character Set Selection via I²C bus

Display of the Complete Character Set



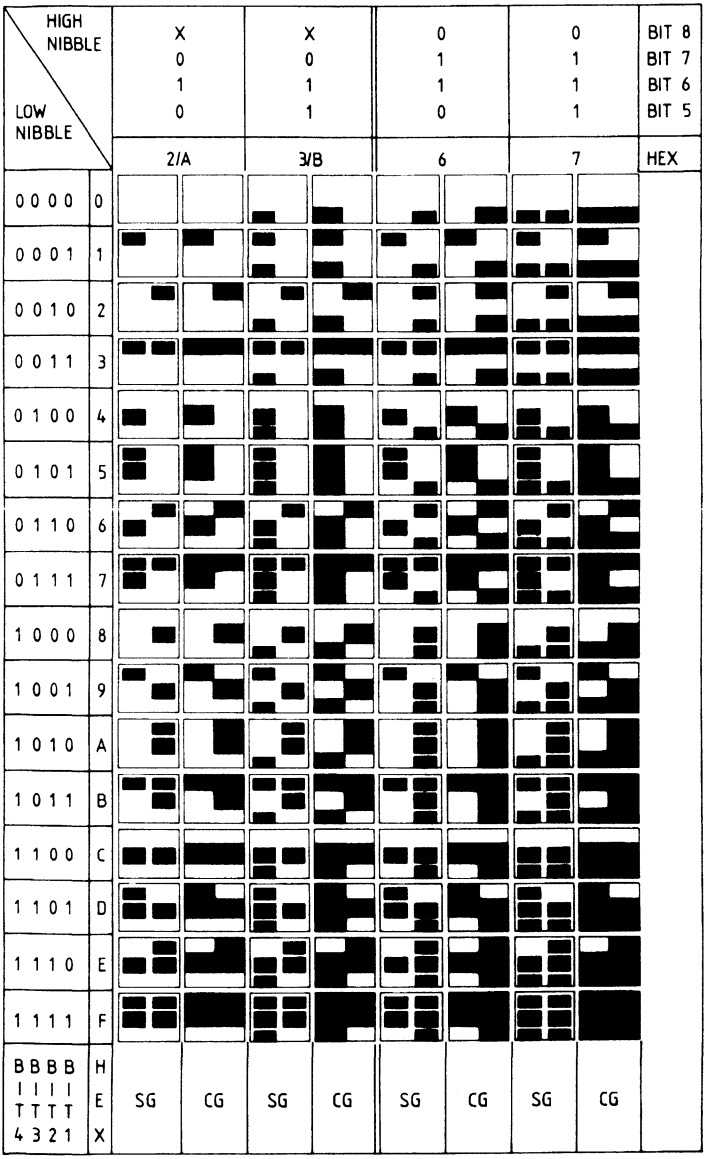
(1) Reset before the starting each row
(2) Is implemented for the control character and not just the following characters
(3) These control characters have to be transmitted twice in succession. Implementation begins between the control characters
(4) Not implemented

Comment: The random access to ^, β and § can be done only when the language selection bits C12, C13, C14 are adjusted to the German language.

Diagram 8

Graphic Characters

Graphics mode is activated by control character (0001 0XXX).



SG: Separated Graphics
CG: Contiguous Graphics

National Character Set Selection using the Transmitted Control Bits

Transmitted parity bit is reset to 0.
The national characters in **diagramm 10** are implemented in the corresponding positions in **diagram 9**.

Transmitter	English	German	Swedish	Italian	French	Spanish	Dynamic character redefinition	reserved
Control bits								
C12	0	0	0	0	1	1	1	1
C13	0	0	1	1	0	0	1	1
C14	0	1	0	1	0	1	0	1
Siemens SDA 5243-2	English	German	Swedish	Italian	French	Spanish	English	English

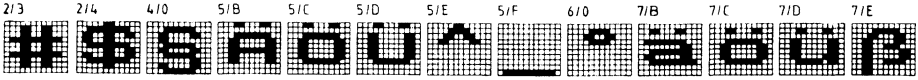
Diagram 9

Basic Character Set

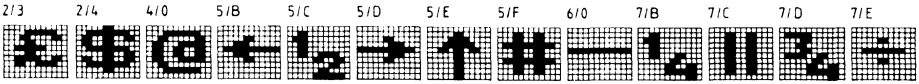
Diagram 10a

National Characters (NC)

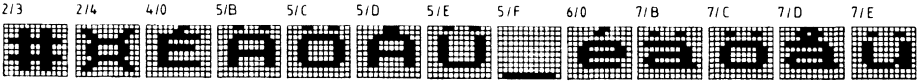
German



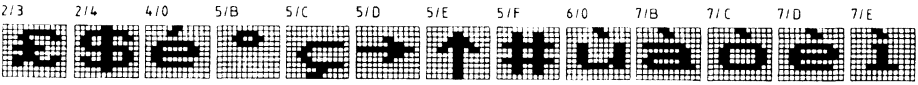
English



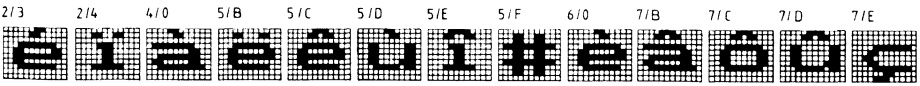
Scandinavian



Italian



French, Belgian



Spanish

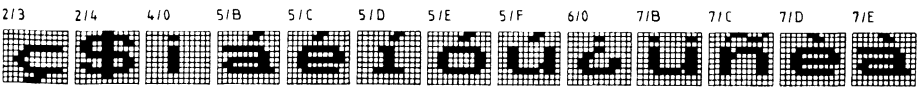
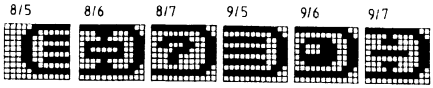
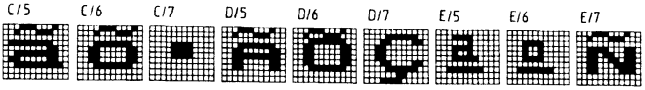


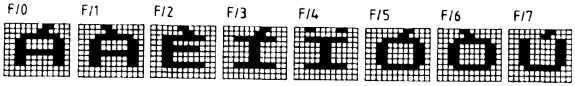
Diagram 10b

National Characters (NC)

Fixed special characters







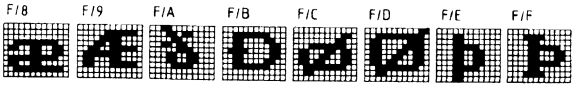
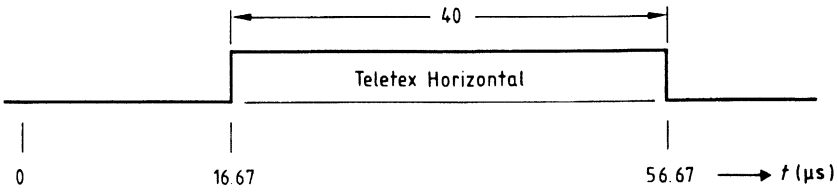


Diagram 11

Display Timing



0 is the reference in measuring circuit 3

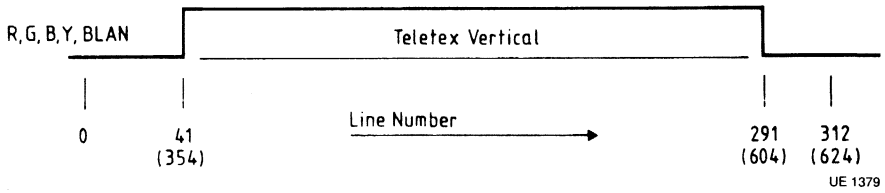
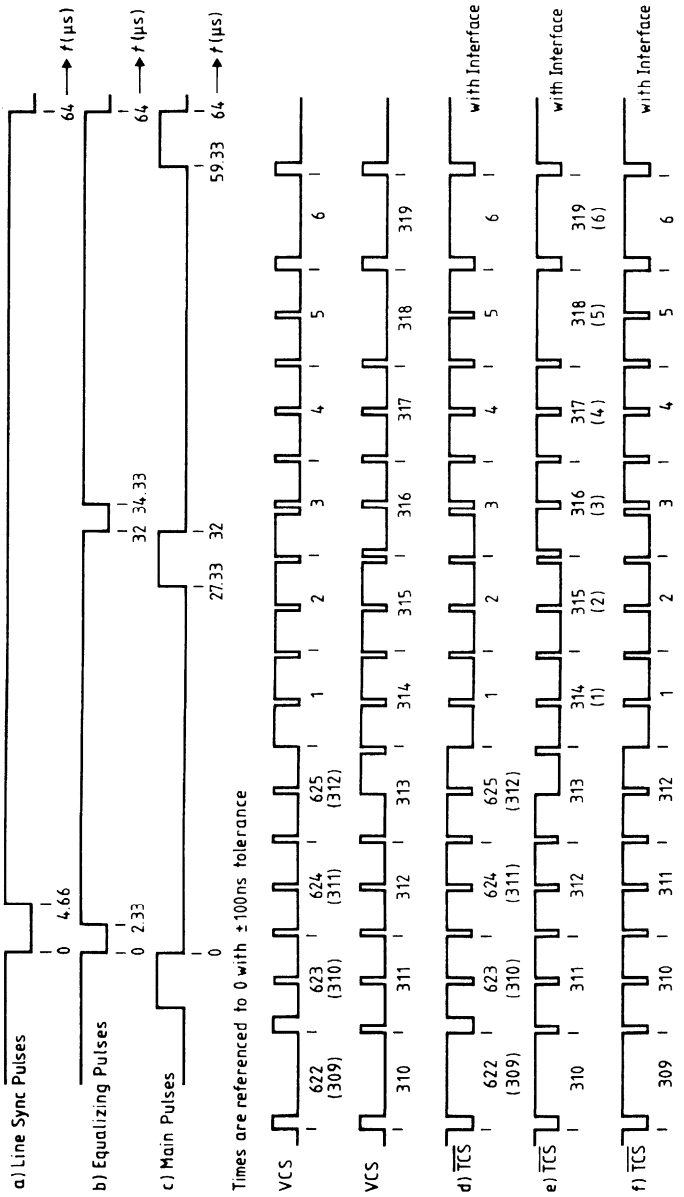


Diagram 12a

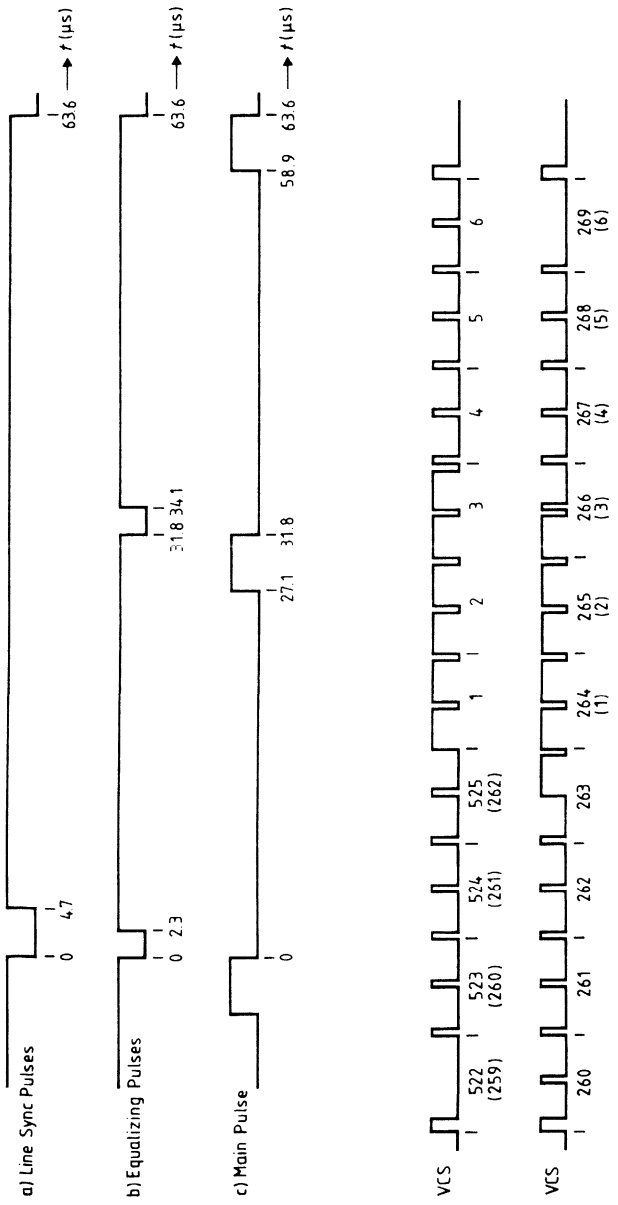
Raster Change Frequency 50 Hz



Composite Sync $\overline{TCS}$, contains line Sync equalizing pulses and main pulses. D,e and f are the vertical Sync signals with line numbers.

Diagram 12b

Raster Change Frequency 60 Hz



1-Chip-VPS-Decoder

SDA 5642

Preliminary Data

MOS IC

Features

- µC suitable VPS data editing direct from CVBS signal
- n-channel MOS
- Generating of the line synchronous 5-MHz clock for the time base and data clock by means of PLL operation
- Very few external components necessary
- Adaptative data separation
- Frame signal recognition
- Decoder for line 16
- Bi-phase and start code checking
- I^2C bus interface
- Operating voltage: 5 V
- Video input signal level. 1 ... 2.0 V_{pp}

Type	Ordering Code	Package
SDA 5642	Q67100-H8547	P-DIP-14
SDA 5642-X	Q67100-H8637	P-DSO-20

Functional Description

The MOS circuit SDA 5642 is used to retrieve the required data for the Video Program System (VPS) service from the data line No. 16 which is included in the CVBS signal. These data are decoded according to the specification given in "Richtlinie ARD/ZDF Nr. 8 R 2".

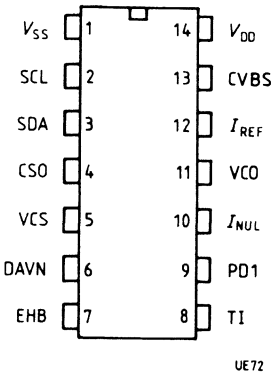
This circuit incorporates the digital functions of the VPS decoder SDA 5640 and the analog functions of the video processor SDA 5232 on one chip. Together with a reduced number of external components this chip is a low cost solution for the VPS detector. The single chip solution can retrieve the data from line 16 of the CVBS signal. These data are decoded, checked for transmission errors and are stored in registers for further processing by a microcontroller. The I^2C bus interface is used for communication of a microcontroller with the VPS-decoder.

The recording of programs by a VTR is controlled by the VPS label, a program related datacode wich accompanies each TV program during its transmission.

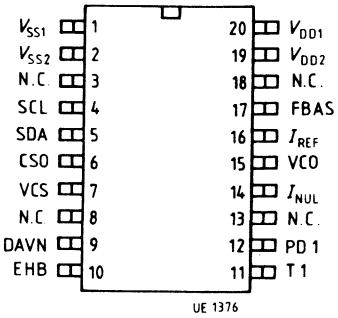
As a result the circuit prevents errors in the recording, as can be seen when using the timer control, when programs are delayed, or are longer than expected.

Pin Configuration
(top view)

P-DIP-14



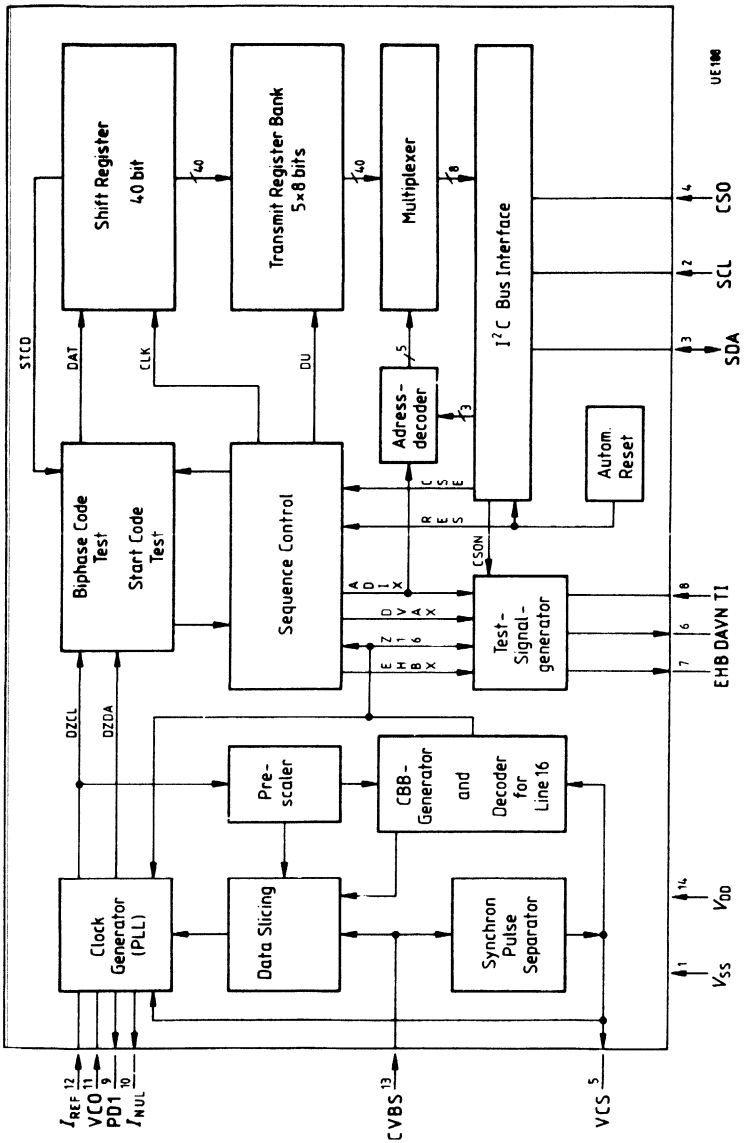
P-DSO-20



Pin Definitions and Functions

Pin No. P-DIP-14	Pin No. P-DSO-20	Symbol	Function
1		V_{SS}	Ground (0 V)
	1	$V_{SS\,1}$	Ground (0 V)
	2	$V_{SS\,2}$	Ground (0 V)
2	4	SCL	Clock line for I^2C bus
3	5	SDA	Data line for I^2C bus
4	6	CSO	To switch the hardware address of the chip from 21 H (CSO = low) to 23 H (CSO = high).
5	7	VCS	Data slicer derives the synchronous signal from the composite video blanking signal.
6	9	DAVN	The form of the output signal provides information whether the set transmitter is transmitting a VPS data line.
7	10	EHB	Output, on "high" level during first half frame.
8	11	TI	By means of the test pins the outputs DAVN and EHB can be switched to test signals outputs; in order to retrieve internal signals for test purposes – depending on the CSO pin.
9	12	PD1	PLL loop filter from system clock phase detector.
10	14	I_{NUL}	Connection for the resistor determining the lower limit of the VCO frequency.
11	15	VCO	Control input for VCO, increase of control voltage raises the VCO frequency.
12	16	I_{REF}	Connection for the resistors determining the upper limit of the VCO frequency.
13	17	CVBS	Video signal input.
14		V_{DD}	Positive voltage supply (+ 5 V).
	20	$V_{DD\,1}$	Positive voltage supply (+ 5 V).
	19	$V_{DD\,2}$	Positive voltage supply (+ 5 V).
	3	NC	Not connected
	8	NC	Not connected
	13	NC	Not connected
	18	NC	Not connected

Block Diagram for 1-Chip-VPS-Decoder



Circuit Description

The function of this integrated circuit is to regenerate the biphase coded VPS data from the CVBS signal. These data are transferred during line 16, which is part of the vertical blanking time. After decoding and a check for transmission errors, these data can be acquired by a microcontroller for further processing. The function of the circuit is explained in more detail by means of the block diagram.

The CVBS signal (pos. video) from the IF-stage is coupled to the device by means of a capacitor. The required level is typically 1 V_{pp}. Then the signal path is split into two parts:

In the synchronous pulse separator stage the CVBS signal is clamped, filtered and the video signal is clipped away from the synchronization pulses. The output signal of this stage is VCS signal. This is used as the control signal for the line 16 decoder and is also used for the blanking of the color burst. This signal is also used in the regeneration of the internal clock (PLL).

The second signal path leads to the data slicer. After amplification of the video signal the level is averaged and the slicing level is derived from this signal. The slicing level is equal to one half of the level difference between the minimum and the maximum value of the data signal. This assures the optimal slicing of the data from the video signal.

The biphase coded data signal sliced from the video signal and the synchronization pulse signal VCS are used in the clock generator circuit. Based upon a PLL, this circuit generates a clock frequency of 5 MHz from the VCS signal. This clock signal is synchronized to the line frequency. During line 16 the clock is synchronized to the data signal.

The synchronization of the data clock is controlled by the signal Z 16, which is the output of the decoder for line 16. This decoder is used to detect line 16 from the VCS signal and to control the data acquisition during this time. An indication signal for the first field of a frame is generated by measuring the duration of the VCS signal pulses and the interval between them.

The regenerated data signal and the recovered data clock are the input signals for a decoding logic which performs the test for the start code and the biphase code. For this purpose the data signal during line 16 is searched for the start bit. This bit, which is used for the synchronization of the decoding logic, is the only bit which does not comply with the biphase format (Manchester code). The detection of the startcode, which is contained in the next six bits following the start bit, is required for the transfer of the correct data into the output register.

Among the 15 bytes (8 bits/byte), which are transferred by the data line 16, only 5 bytes are important for the operation of VPS in the video recorder. These are the 5th and the 11th through the 14th byte. These 40 bits in total are transferred into a serial operating register buffer. The check for the correct transfer of the data according the biphase code is performed during the complete transfer of the data telegram in line 16. After the end of word 14 the relevant bytes are transferred into the transmission register bank. This is done when

1) the start code has been identified
2) the transmission was done correctly according to the biphase code format, and
3) if there is no concurrent access to the device via the I^2C bus.

A microcontroller can read the data from the transmission register bank via the I²C bus interface. The device can operate on the I²C bus as slave-transmitter device. After reading the data, all registers are set to hex "F". Only after the correct reception of data line 16, is the register content updated again.

Because of the fact that data line 16 is transmitted only once during a frame (two fields), the reading of the transfer registers has to be done within a period of greater than 40 msec. between read operations.

The transfer of the data via I²C bus is explained according to the following description and the **figures 5 and 6**. The communication protocol uses the following format:

START	Chip address of Master	AS	Word 11 of Slave	AM	...	Word 14 of Slave	AM	Word 5 of Slave	NAM	STOP

The information content of the bytes 11 through 14 and the byte number 5 are given in **figure 7**.

As a chip address for the I²C bus the following address is selected:

Bit Number:	7	6	5	4	3	2	1	0
	0	0	1	0	0	0	CSO	0

If the device's chip select input is set to a low level or a high level, then bit 1 (CSO) has to be set to "0" or "1"respectively. Bit 0 is the data direction bit and has to be set to "1" because of the fact that only "Read" operations can be performed. (Slave transmitter mode.)

The data transfer between master (microcontroller) and slave (VPS decoder) uses the following procedure **(See figure 5)**:

0. If the bus is not occupied – idle state – then the clock line and the data line are both on logic "high" levels.
1. The master starts the data transmission by generating the start condition. This means that the SDA line is pulled down to a logic "low" level during the time when the SCL line is still on a logic "high" level. The byte address counter in the slave device is reset by this operation and points to byte 11. The following data clock pulses on the SCL line are generated by the master. For the data transfer it has to be observed that changes in the logical level on the SDA line are only possible if the SCL line is kept on a "low" level. The only exceptions are the start and stop conditions on the I²C bus.
2. The master sends the chip address on the SDA line with the first 8 data clock pulses on SCL to the VPS decoder.
3. During the 9th clock pulse the master releases the SDA line. Due to the external pull-up, the SDA line goes to a "high" level and the VPS decoder (slave) generates an acknowledge by pulling the SDA line to a "low" level. At this time the slave switches in the transmission mode.
4. During the next 8 clock pulses the slave outputs the data of the addressed data byte to the SDA line.

5. The reception of the byte will be acknowledged by the master during the following clock pulse. This means the master pulls the SDA line to a "low" level. This action increases the byte counter in the slave increments and prepares the output of the next data byte.
6. The slave outputs the next data byte to the SDA line.
7. and 8.

. For every data byte to be transferred, steps 5 and 6 have to be repeated. To conclude the read operation, the master does not acknowledge the last byte – as described in step no. 9.

9. During the acknowledge interval the master lets the SDA line remain in the "high" status (so called Non Acknowledge by Master, NAM). The slave understands this NAM as the end of the communication process and switches from transmit mode to receiver mode.
10. The master now has the full control over the SDA line and finishes the communication process by issuing the stop-condition. This means that during the time when the SCL is on "high" level, the microcomputer generates a "low" to "high" transmission on the SDA line. This brings the I^2C bus into the idle state.

Description of Added Functions

1. The pin Data-Valid (DAVN) allows very easy control of the availability of the VPS signal by the selected TV transmitter. If the VPS data line is available, this pin will show pulses with the frequency of the frame repetition rate. This output is set "high" at the beginning of line 16 and is reset by the data transfer pulse, an internal signal at the end of byte 14 in the data line 16. If, due to a missing VPS information in the CVBS signal, this data transfer pulse is not generated, the DAVN pin remains on a "high" level.

   This output is also set "high", when the circuit is accessed via the I^2C bus. This may be useful in some cases when the output is low without the presence of a CVBS signal – thus pretending a TV transmitter carrying VPS information.
2. By means of the "Test" pin (TI = "high") it is possible to use the DAVN pin to output internal test signals. Depending on the status of the input CSO, the internal signal Z16N (CSO = "low") or the ADIX signal (CSO = "high") is switched to the DAVN output.
3. The data transfer from the VPS decoder to the microcomputer starts after the master controller has transmitted the chip address of SDA 5642. This chip address has to be identical with the hardware address of the VPS decoder. By means of the CSO input it is possible to switch this hardware address from 21 H (CSO = "low") to 23 H (CSO = "high").
4. The output EHB generates an indication for both of the fields in a frame. During the first field this pin shows the "high" level. The correct timing of this pulse is given in **figure 4**. For test purpose this pin can be switched to the test signal output mode. This is done by setting the TI pin to high. The output signal in this mode depends on the logical level on the CSO pin. If CSO is "low", the internal signal LL64ON is generated, if the CSO pin is "H" the output signal is DZDAX, which is also an internal test signal, is generated.

Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Ambient temperature	T_A	0		70	°C	in operation
Storage temperature	T_{stg}	– 40		125	°C	by storage
Total power dissipation	P_{tot}			300	mW	
Power dissipation per output	P_{DQ}			10	mW	
Input voltage	V_{IM}	– 0.3		6	V	
Supply voltage	V_{DD}	– 0.3		6	V	
Thermal resistance	$R_{th\ SU}$			80	K/W	

Operating Range

Supply voltage	V_{DD}	4.5	5	5.5	V	
Supply current	I_{DD}			50	mA	
Ambient temperature range	T_A	0		70	°C	

Characteristics
T_A = 25 °C

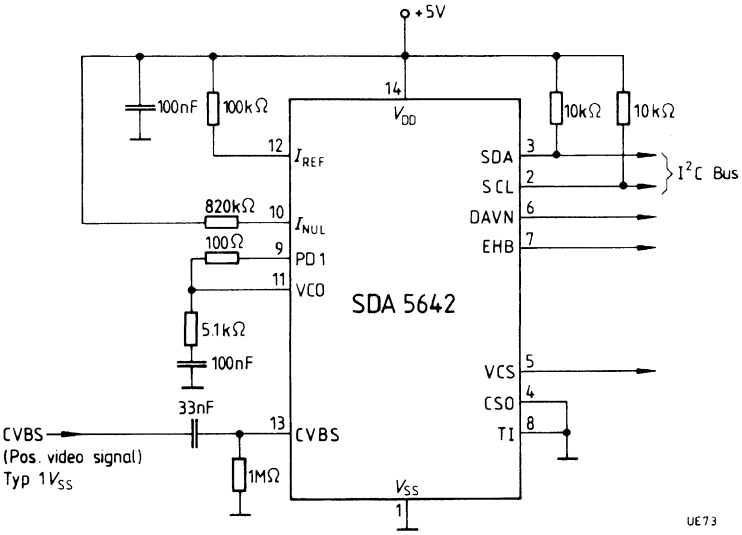
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Signals SDA, SCL						
H - input voltage	V_{IH}	3.0		V_{DD}	V	
L - input voltage	V_{IL}	0		0.8	V	
Input capacitance	C_I			10	pF	
Input voltage	I_{IM}			10	µA	
Input Signals CSO, TI						
H - input voltage	V_{IH}	2.0		V_{DD}	V	
L - input voltage	V_{IL}	0		0.8	V	
Input capacitance	C_I			10	pF	
Input current	I_{IM}			10	µA	
Input Signals CVBS (pos. Video, neg. Sync)						
Video input signal level	V_{CVBS}	0.7	1.0	2.0	V	
Synchron signal amplitude	V_{SYNC}	0.15	0.3	1.0	V	
Data amplitude	V_{DAT}	0.25	0.5	1.0	V	
Coupling capacitor	C_C		33		nF	
H - input current	I_{IH}			10	µA	V_I = 5 V
L - input current	I_{IL}	– 1000	– 400	– 100	µA	V_I = 0 V
Source impedance	R_S			250	Ω	
Leakage resistance at coupling capacitor	R_C	0.91	1	1.2	MΩ	

Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ..	max.		
Output Signals DAVN, EHB, VCS						
H - output voltage	V_{QH}	$V_{DD}-0.5$			V	$I_Q = -100\ \mu A$
L - output voltage	V_{QL}			0.4	V	$I_Q = 1.6$ mA
Output Signals SDA (Open-Drain-Stage)						
L - output voltage	V_{QL}			0.4	V	$I_Q = 3.0$ mA
Permissible output voltage				5.5	V	
PLL – Loop Filter Components						
Resistance at PD1	R_1	0	100	150	Ω	
Resistance at VCO	R_2		820		kΩ	
Attenuation resistance	R_3		5.6		kΩ	
Integration capacitor	C		100		nF	
VCO – Frequence Range Adjustment						
Resistance at IREF (for bias current adjustment)	R_4		100		kΩ	
Resistance at INUL (for quiescent current adjustment)	R_5		820		kΩ	

Test Circuit

Data Line Receiver



Application Circuit

Data Line Receiver

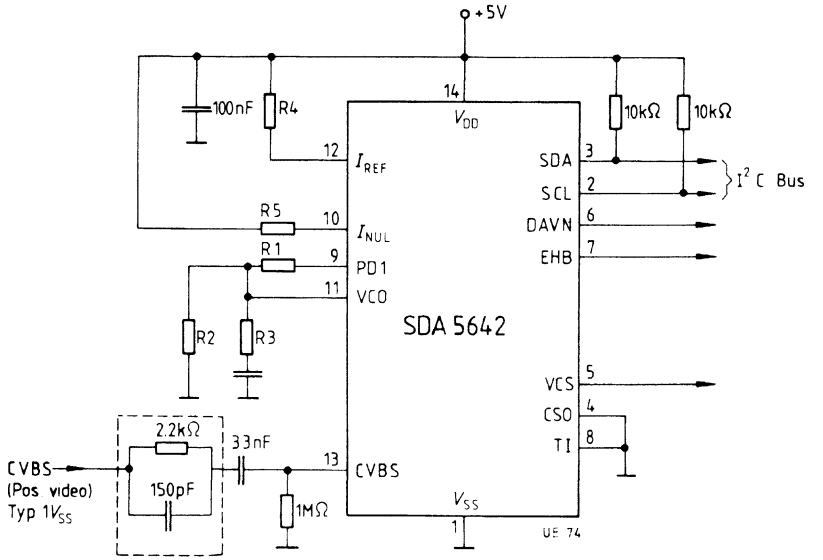


Figure 1

CVBS Signal with Position of VPS Data Line

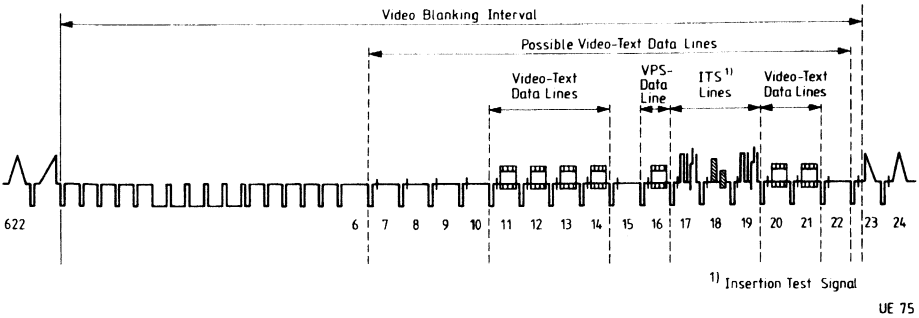


Figure 2

Insertion of Data Line into CVBS Signal

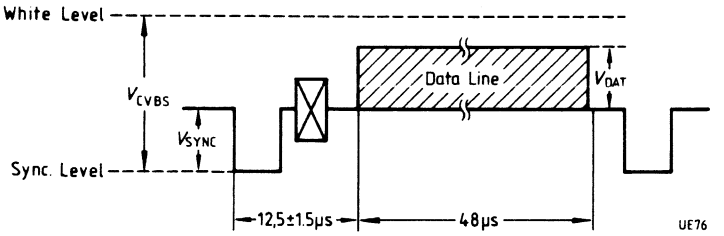


Figure 3

Video Signal

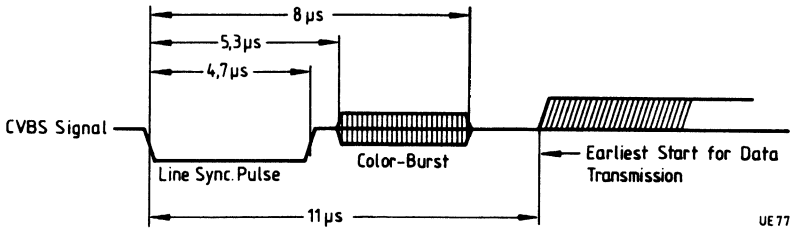


Figure 4
VCS-DAVN-EHB Signal

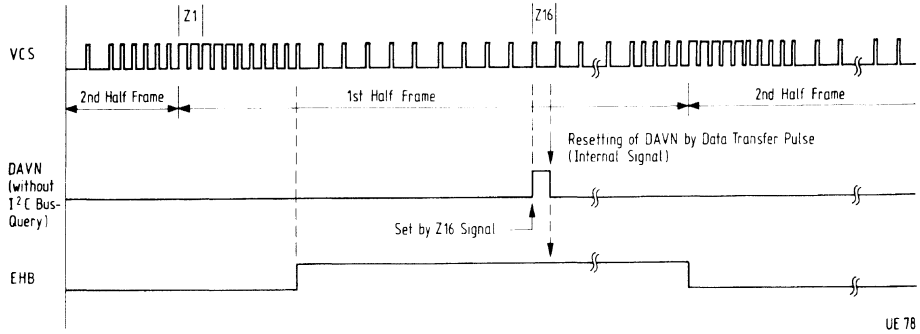
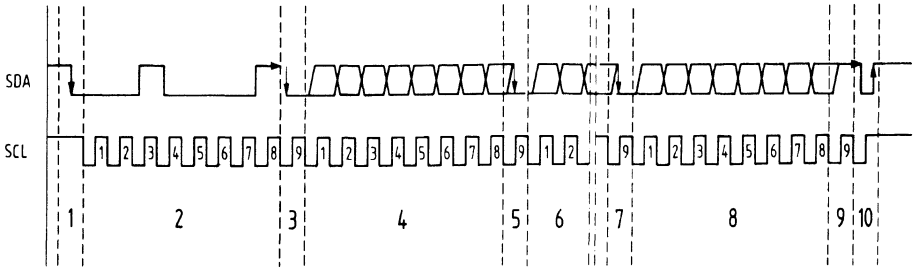


Figure 5
Transfer Protocol for I²C Bus



1 START CONDITION
SDA ↓ when SCL = High

2 Chip Address Input

3 Acknowledge from Slave

4 Output of 1st Data Word
from Slave → Master

5 Acknowledge from Master
(Prompt for Additional Output=
Word Address is Simultaneously
Incremented by 1)

6 Output of next Data Word

7 Acknowledge Master

8 Output of 5th Data Word

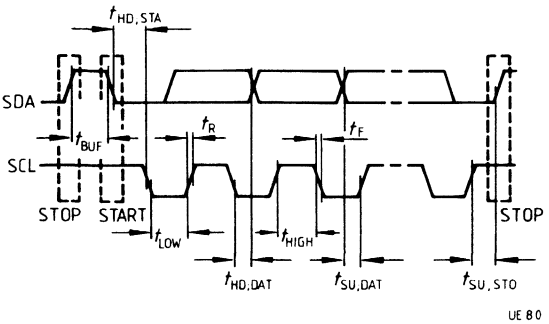
9 No-Acknowledge Master

10 STOP CONDITION
SDA ↑ by SCL = High

UE 79

Figure 6

I²C Bus Timing

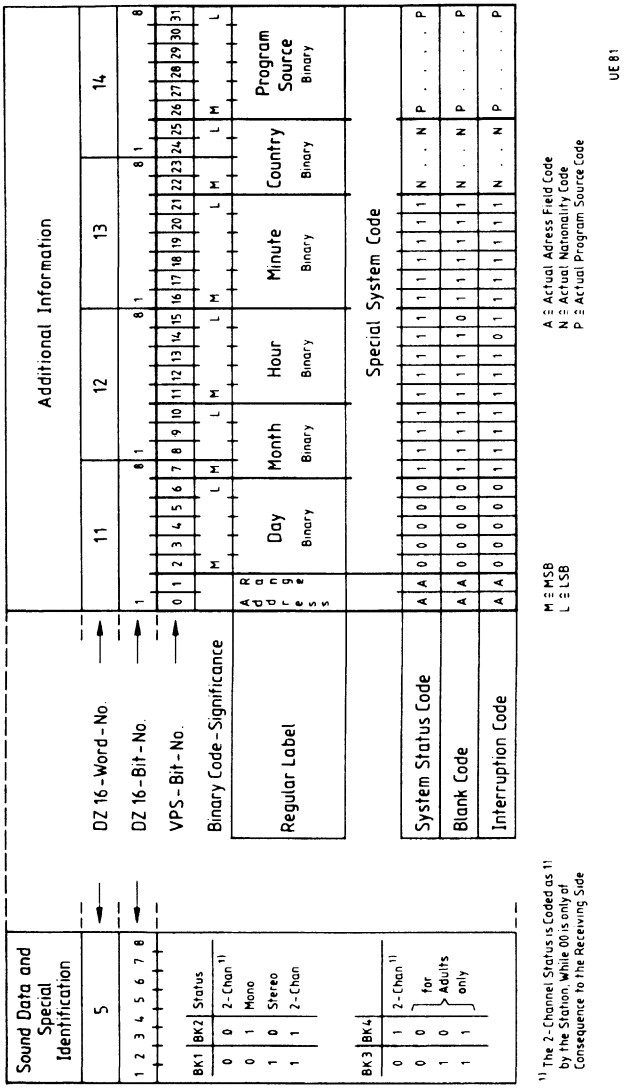


Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	f_{SCL}	0	100	kHz
Inactive time period prior to new transmission start-up	t_{BUF}	4.7		µs
Hold time during start condition (subsequent to this time period the first CLOCK pulse will be generated)	$t_{HD;STA}$	4.0		µs
LOW-period of lock	t_{LOW}	4.7		µs
HIGH-period of clock	t_{HIGH}	4.0		µs
Set-up time for Data	$t_{SU;DAT}$	250		ns
Rise time for SDA and SCL signal	t_R		1	µs
Fall time for SDA and SCL signal	t_F		300	ns
Set-up time for SCL clock during STOP conditions	$t_{SU;STO}$	4.7		µs

All values referred to V_{IH} and V_{IL} levels.

Figure 7

Data Format of Additional Information in Data Line 16



SIEMENS

Analog-Digital-Interface for Inserted Picture — SDA 9087

Preliminary Data — **MOS IC**

Features

- 3 separate A/D converters
- Resolution: 5 bit
- Sampling rate: 13.5 MHz, 3.375 MHz
- Clamping crcuit for the inut sgnals
- Adjustable delay for the luminance signal (9 steps)
- Color difference signals Y and V can be inverted
- Multiplexed output interface (DMSD compatible)
- Internal clock synchronization by sandcastle signal
- System clock generation for picture insertion processor
- BLN synch signal

Type	Ordering Code	Package
SDA 9087	Q67100-H8707	P-DIP-28

Description

Together with an analog color decoder and a sync separator for the H, V sync signals, the SDA 9087 forms an analog picture channel on whose input the analog CVBS signal is applied. This output produces the digital components Y, U, V plus the sync signals of this CVBS signal. The resolution of the digital output signals is 5 bit.

Furthermore, with the aid of PLL, the SDA 9087 generates the line locked clock LL3 (nom. 13.5 MHz) and the blanking signal BLN.

The picture channel described can replace a high-grade and costly digital picture channel consisting of the devices 7-bit ADC, digital multi-standard decoder (DMSD) and central clock generator (CCG).However, the quality of the picture is reduced , and for this reason the more obvious application is as a picture channel for the inset picture that is inserted in a picture-in-picture (PIP) system.

Y, U and V are digitized by 5-bit flash converters and output in a format that matches the interface of the PIP processor. The PLL synchronizes to an external, horizontal sync signal that is derived from the CCV signal of the inset picture.

Circuit Description

The luminance signal Y and the chrominance signals U, V are fed to the SDA 9087 by means of coupling capacitors. The black level of Y is clamped to V_{REFL}; the color subcarrier must be filtered out of Y.

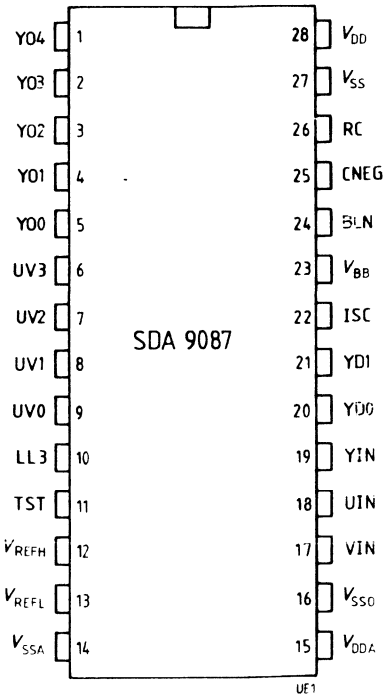
The three signals components are digitized by 5-bit A/D flash converters; the sampling rate is determined by LL3. Y is output as binary offset code. The digitized Y signal is delayed in a delay block. This delay can be varied in increments of two LL3 cycles in a range of 0 through 16 LL3 cycles on pins YD0,1 to compensate for different delays in the preceding luminance and chrominance decoders.

The white level of U and V is clamped to 0.5 x (V_{REFH} + V_{REFL}). U, V are then converted into a 5-bit two's complement code. The digitized U, V signals can be inverted via CNEG control input. A multiplexer selects every fourth U, V sample and applies this 10-bit information in four clock cycles in a nibble format to pins UV (0:3).

The horizontal PLL, consisting of a horizontal timer, phase comparator and VCO, generates the line-locked picture-in-picture system clock LL3 and the internal chip timing.

The horizontal timer divides the LL3 clock by 864 (the same for PAL and NTSC) and applies this signal as a horizontal reference signal to the phase comparator (PC). The external horizontal signal is decoded from the sandcastle signal and matched in its pulse width (= 345 LL3 cycles) to the reference signal. The digital phase comparator is frequency- and phase-sensitivite (type 4) and produces current pulses at its output. The up/down pulses of the phase comparator are filtered on pin RC. The filtered signal is the control voltage of the VCO. The horizontal timer also determines the start time and the width of the clamping pulse as well as the location of the blanking signal BLN, which in turn defines the horizontal duration of the picture information on the Y output and should be synchronous with it. BLN is consequently delayed to the same degree as Y.

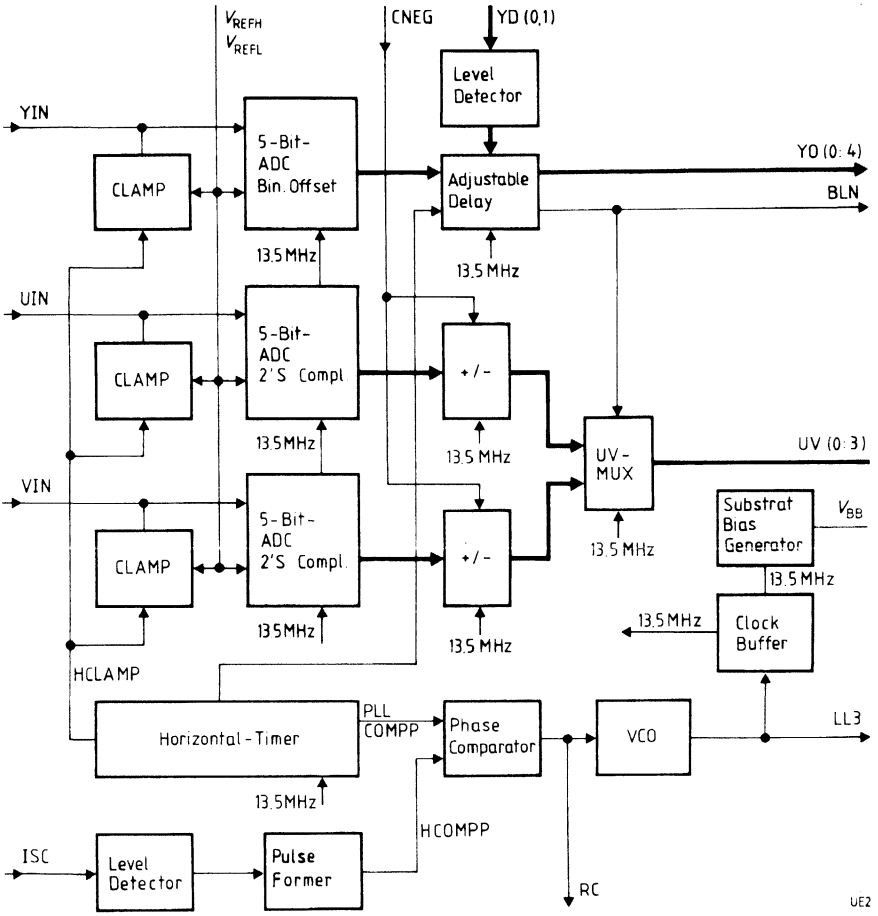
Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
1-5	YO (4:0)	O	Digital Y output signal (Index 0 = LBS)
6-9	UV (3:0)	O	Digital Chrominance signal (nibble format)
10	LL3	O	Output of the line locked system clock (nom. 13.5 MHz)
11	TST	I	Test pin, to be switched at V_{SS} or open no wiring = L level
12	V_{REFH}		High reference voltage for the A/D converter
13	V_{REFL}		Low reference voltage for the A/D converter
14	V_{SSA}		Analog ground
15	V_{DDA}		Analog 5 V supply voltage
16	V_{SSO}		V_{SS} connection for the oscillator
17	VIN	I	Analog input for the V signal
18	UIN	I	Analog input for the U signal
19	YIN	I	Analog input for the Y signal
20, 21	YD0, YD1	I	To adjust the Y delay No wiring = L level
22	ISC	I	Input for the sandcastle-synchronous signal of the gate signal
23	V_{BB}		Substrate bias (internally produced)
24	BLN	O	Blanking signal output
25	CNEG	I	Color negated. By H level the crominance signals are multiplied by 1 and are output. No wiring = L level
26	RC	O	Pin to the analog loop filter connection of the PLL
27	V_{SS}		Digital ground
28	V_{DD}		Digital 5 V supply voltage

Block Diagram



Absolute Maximum Ratings
T_A = 0 to 70 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{DD} V_{DDA}	– 0.3 – 0.3	6 6	V V
Voltages at I/O pins	V_{IN}	– 0.3	7	V
Voltages differences between $V_{REF\,H}$ and $V_{REF\,L}$	ΔV_{REF}	– 4	4	V
Ambient temperature	T_A	– 20	70	C
Storage temperature	T_{stg}	– 20	125	C
Power dissipation	P_{tot}		0.8	W

Operating Range

Supply voltages	V_{DD} V_{DDA}	4.5 4.5	5.5 5.5	V V
Ambient temperature	T_A	0	70	°C
Reference voltage	$V_{REF\,H}$ $V_{REF\,L}$	2.5 1.5	3.5 2.5	V V

Characteristics

T_A = 25 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply Voltages	V_{DD}	4.5	5	5.5	V	
	V_{DDA}	4.5	5	5.5	V	
Current consumption	I_{DD} total		100	120	mA	

Digital Output Y0 (0:4), UV (0:3), BLN, LL3

Load capacitance	C_L	0		20	pF	
Low level	V_{QL}	0		0.4	V	I_{QL} = 1.6 mA
High level	V_{QH}	2.4			V	I_{QH} = – 0.2 mA
Delay to the negative transition of LL3	t_d			14	ns	LL3 = V_{QL}

LL3 Pulse Form

Rise time	t_{LL3R}	0		7	ns	
Fall time	t_{LL3F}	0		5	ns	
H-pulse widh	t_{LL3H}	28			ns	T_{LL3} = 68 ns
L-pulse widh	t_{LL3L}	28			ns	T_{LL3} = 68 ns
LL3 period duration	T_{LL3}	< 68	74	< 80.6	ns	

Digital Input

CNEG						
Low level	V_{CNL}			0.8	V	
High level	V_{CNH}	2.0			V	
Input current	I_{CN}			30	µA	V_{CNH} = 5 V
YD (0,1)						
Low level	V_{YDL}			0.8	V	
Mid level	V_{YDM}	2.0		0.55 V_{DD}	V	
High level	V_{YDH}	4.0			V	
Input current	I_{CN}			30	µA	V_{CNH} = 5 V

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Sandcastle Input ISC						
High level	V_{HSC}	3.5		V_{DD}	V	
Mid level	V_{ASC}			2.5	V	
Low level	V_{VSC}	0		V_{ASC}	V	
Switching threshold for High level			0.6 V_{DD}			
VCO **Sandcastle input ISC**						
Frequency range		< 12.4	13.5	> 14.7	MHz	
		< 12.4			MHz	V_{RC} = 1.0 V V_{DD} = 4.5 V T_A = 0 °C
				> 14.7	MHz	V_{RC} = 3.8 V V_{DD} = 5.5 V T_A = 70 °C
Phase Detector						
Pulse current	I_{PD}		160		µA	V_{DD} = 5 V
PLL Loop Filter (recommended value)						
R_1			3.8		kΩ	see application circuit
C_1			2.2		µF	
C_2			0.1		µF	
Analog Input YIN, UIN, VIN						
The dynamic range of the converter goes from $V_{REFL\text{-}intern}$ to $V_{REFH\text{-}intern}$ with:						
$V_{REFH\text{-}intern}$	= V_{REFH} – 30 mV typ.					
$V_{REFL\text{-}intern}$	= V_{REFL} + 30 mV typ.					
Clamping level YIN	= $V_{REFL\text{-}intern}$ +/–10 mV					
Clamping levels UIN, VIN	= 0.5 × ($V_{REFH\text{-}intern}$ + $V_{REFL\text{-}intern}$) +/–10 mV					

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input capacitance	C_{IN}		35		pF	
Leakage current at YIN, UIN, VIN	I_L		1.0		µA	$V_{YIN} = V_{UIN} =$ $V_{VIN} = 3.0$ V $V_{REFH} = 3.0$ V $V_{REFL} = 2.0$ V
Internal resistance in clamping time for R_I of V_{REFH} and $V_{REFL} = 0\ \Omega$	R_{CU} = R_{CV} R_{CY}		2.4 0.5	3.0 1.0	kΩ kΩ	$V_{REFH} = 3.0$ V $V_{REFL} = 2.0$ V
Start of the clamping pulse refer to the transmission of the horizontal ISC burst pulse	t_C		1.4*		µs	
Clamping pulse duration	t_{CPD}		0.666**		µs	
Coupling capacitor for YIN, UIN, VIN	C_U, C_V, C_Y		10		nF	

* (= 19 LL3 period)
** (= 9 LL3 period)

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Dynamic range of the converter ($V_{REF\,L}$ intern to $V_{REF\,H}$ intern)			0.95 × (V_{REFH} – V_{REFL})			

DC-Transfer-F Function of the A/D Converter

Integral non-linearity*				+/- 1	LSB	$V_{REF\,H}$ = 3.0 V $V_{REF\,L}$ = 2.0 V
Differential non-linearity*				+/- 0.5	LSB	

Reference Voltage
V_{REFH}, V_{REFL}

Current consumption	$I_{REF\,H}$ $I_{REF\,L}$			2.5 – 2.5	mA mA	$V_{REF\,H}$ – $V_{REF\,L}$ = 1 V
$V_{REF\,H}$ $V_{REF\,L}$		2.5 1.5	3.0 2.0	3.5 2.5	V V	

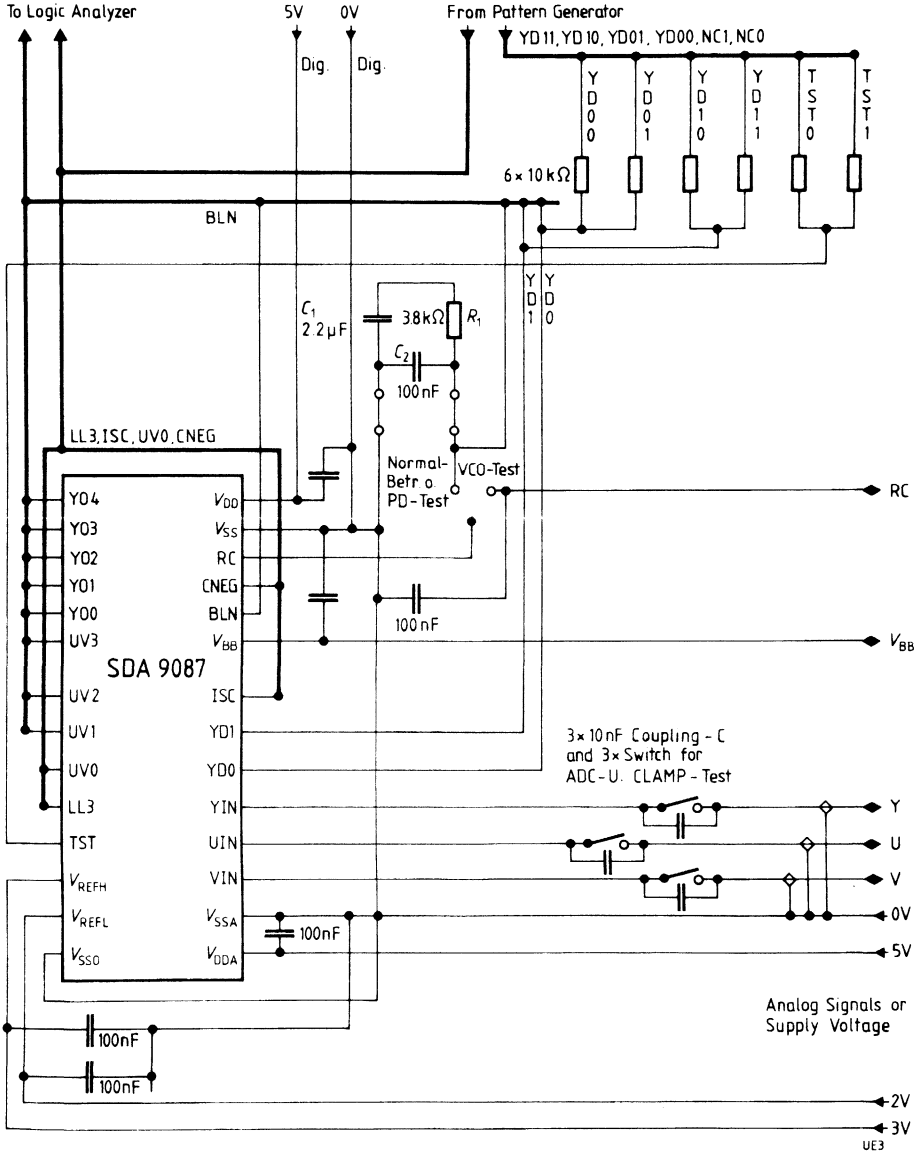
Substrate Bias
V_{BB}

V_{BB}		– 2.6		– 1.6	V	V_{DD} = 5.0 V R_L between V_{BB} and V_{SS}> 100 kΩ

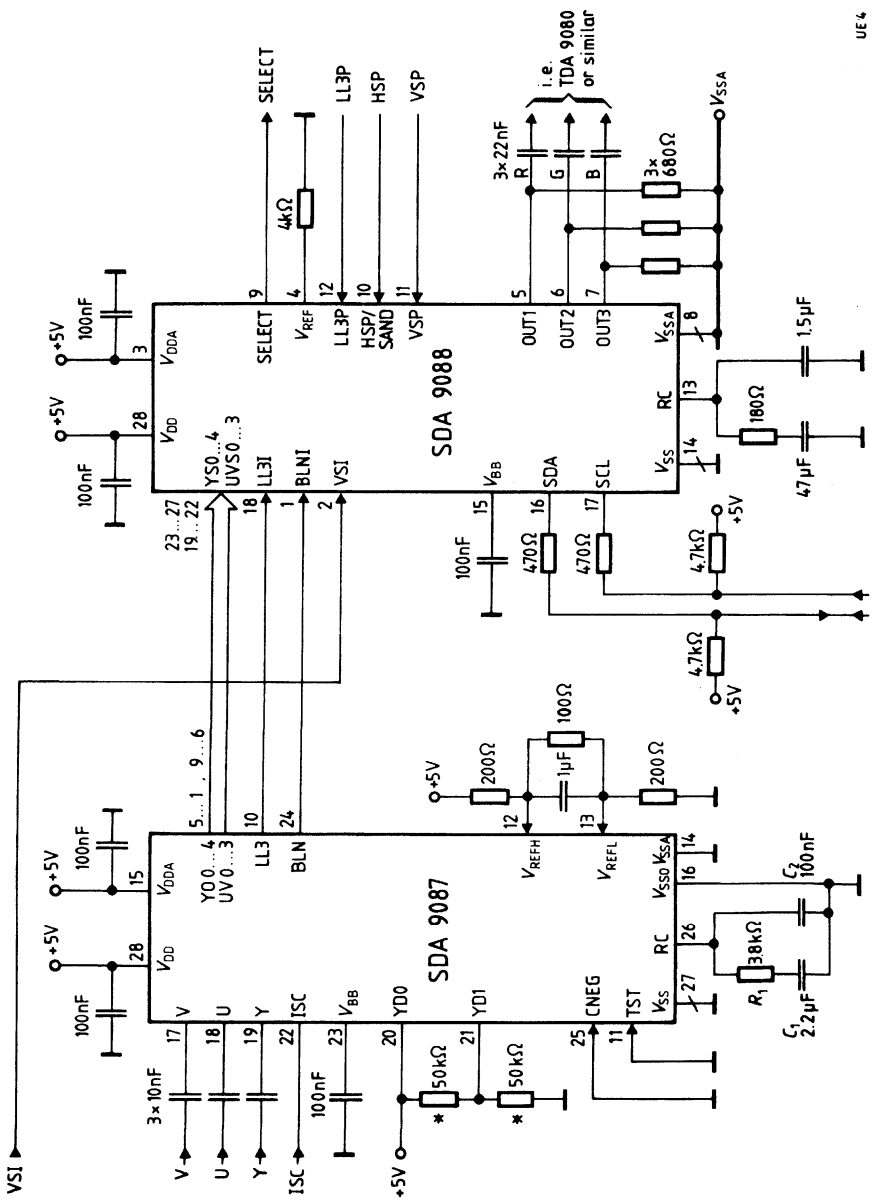
* The absolute tolerance of the coupling level and the converter characteristic line are not influenced by the difference V_{REFH} – V_{REFL} (dynamic range of the converter) which lead to big errors by $V_{REF\,H}$ – $V_{REF\,L}$ < 1 V

Measuring Circuit

Digital Signal or Supply Voltages

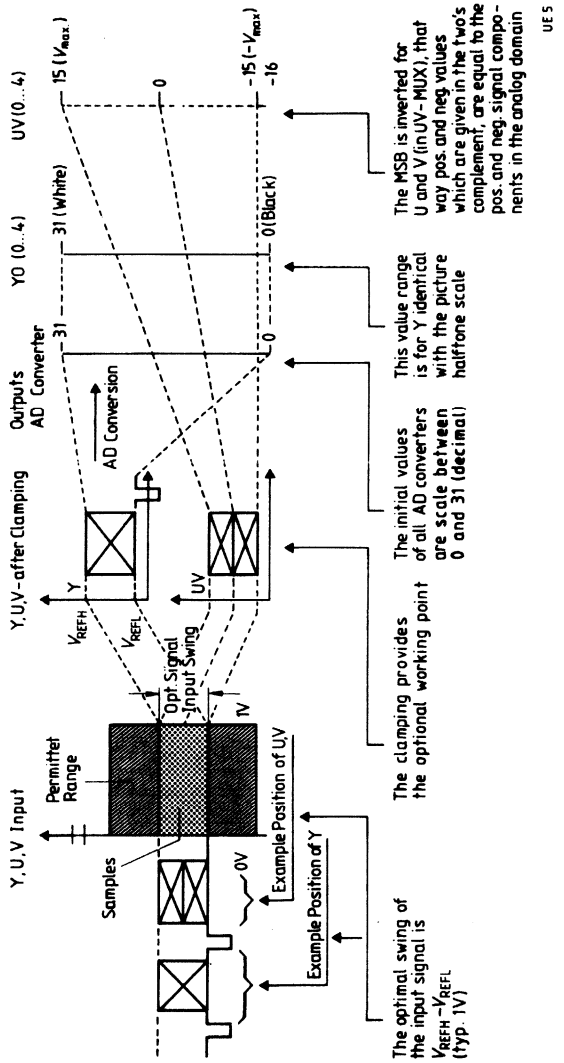


Application Circuit

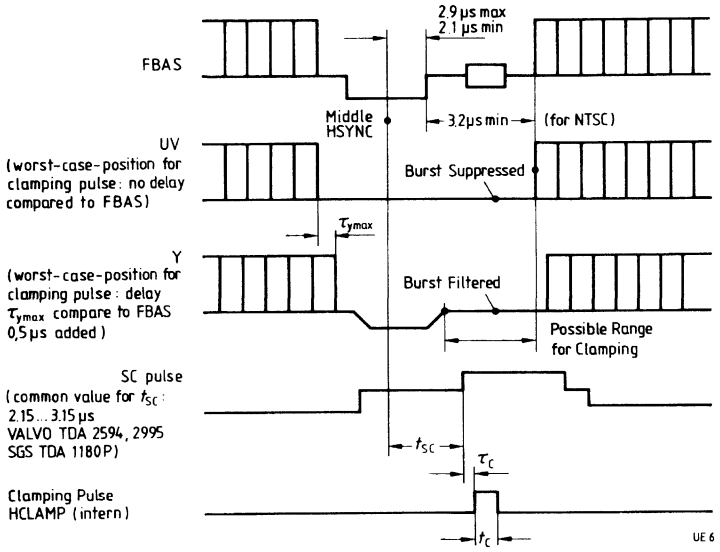


Pulse Diagram

Input Voltage Range of Y, U and V and them Translation in Initial Values ("Digital Values")



Clamping Pulse Timing



Leading edge at clamping pulse

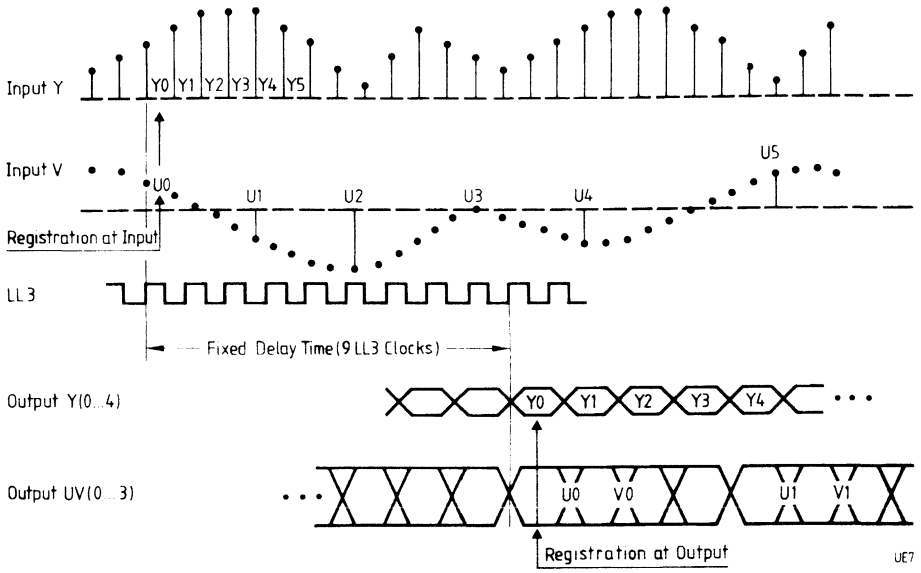
$t_{SC\,min} + \tau_C > 2.9\ \mu s + \tau_{ymax} \approx 3.4\ \mu s$
chosen: $\tau_C = 1.4\ \mu s$ (19 LL3 clocks)

Tailing edge at clamping pulse

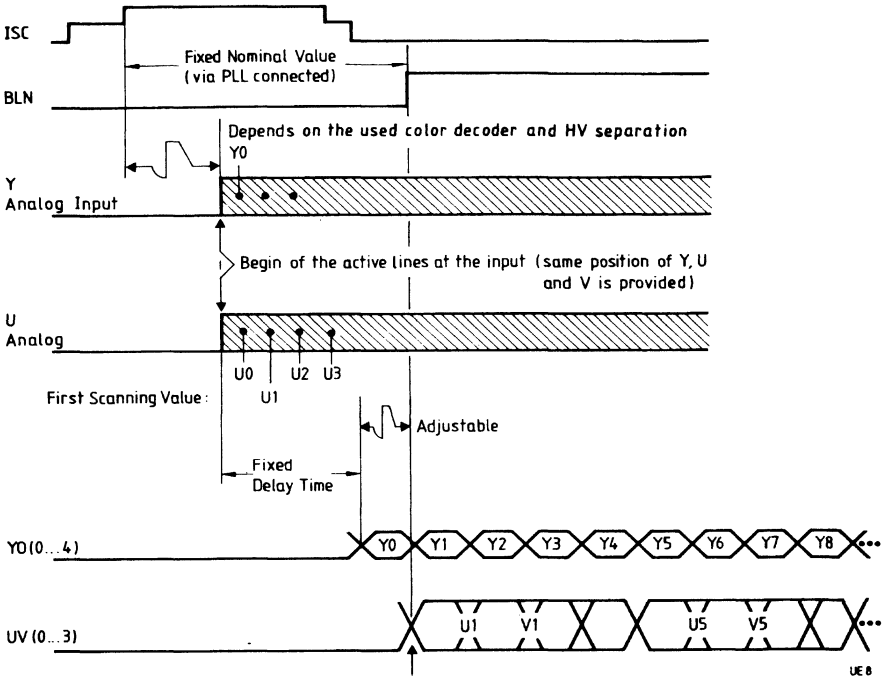
$t_{SC\,max} + \tau_C + t_C < 5.3\ \mu s = 3.2\ \mu s + 2.1\ \mu s$
chosen: $t_C = 0.7\ \mu s$ (9.5 LL3 clocks)

Signal Delay Time for U, V and Y
(used indication: number of scanning values).

Additionally programmable delay time in DELAY-Block-0.

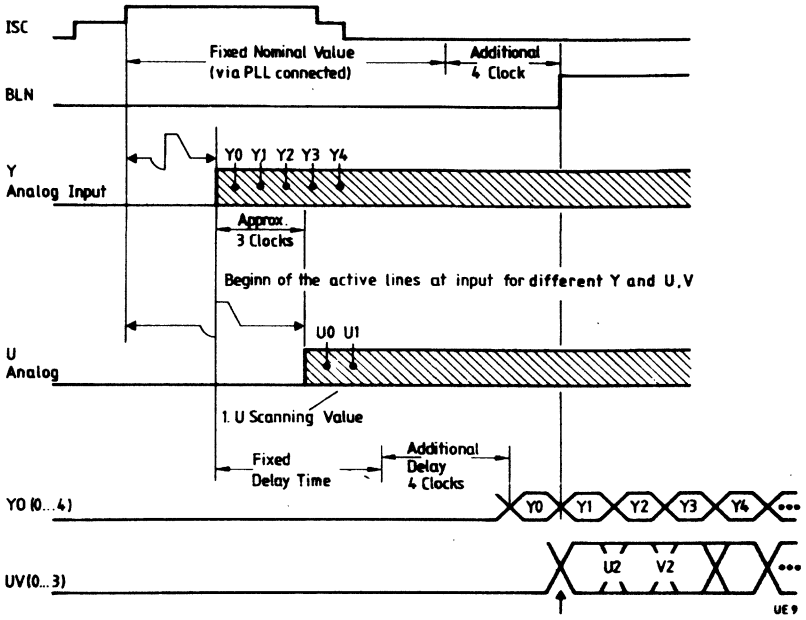


Relation between SC, BLN and Y and UV
(used indication: number of pixels)



- Y, U, V have no delay time differences.
- Delay between SC and Y, U, V is smaller than provided for the optimal case.

Relation between SC, BLN and Y and UV
(used indication: number of pixels)



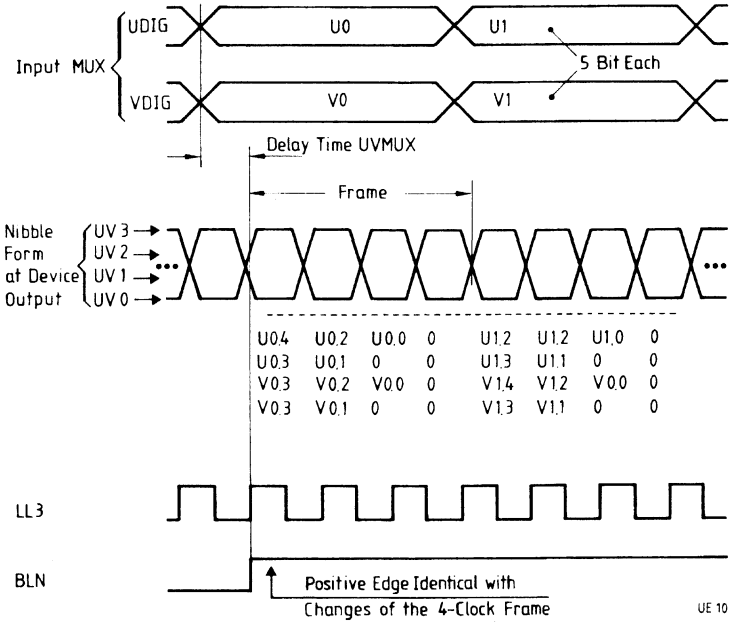
U, V are delayed approx. 3 LL3 clocks compare to Y;

Compensation through an additional Y-delay of 4 clocks.

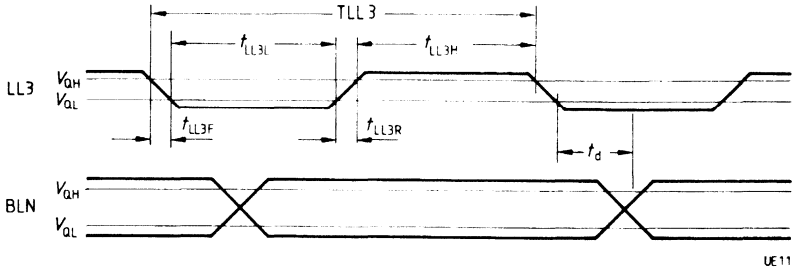
- BLN edge and raster correspond to each other;
- Begin of the active lines of Y0 (0 ... 4) and UV (0 ... 3) is moved.
- Registration errors still 1 clock (Y value 1 clock to late, because of 4 clocks delay, U-delay but only 3 clocks).

Conversion of U and V in a Nibble Form with 13.5 MHz, 4 Bit

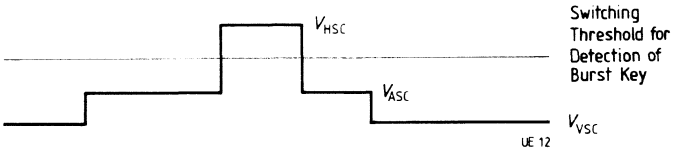
It means: 1. index: number of scanning value (pixels)
2. index: number of bits; 4 = MSB



Specification of Edges



Sandcastle Pulse

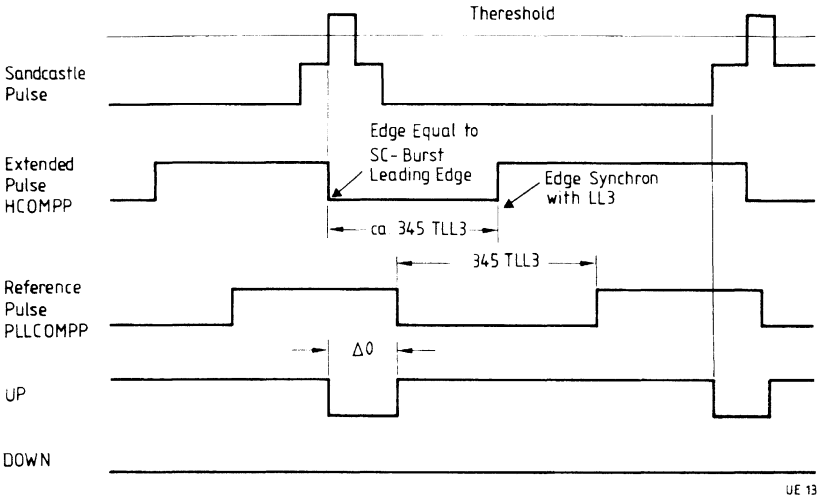


Adjusting of Y-Delay via YD0, YD1

Level Range		Additional Delay for Y and BLN	
PIN YD1	Pin YD0		
		LL3 clocks	typ. value
1	1	0	0
1	2	2	148 ns
1	3	4	296 ns
2	1	6	444 ns
2	2	8	592 ns
2	3	10	740 ns
3	1	12	888 ns
3	2	14	1.04 µs
3	3	16	1.18 µs

Level range:
1 = V_{YDL}
2 = V_{YDM}
3 = V_{YDH}

Function of SC Pulse Extention and Phase Comparison
(PLL is unlocked, behind the external H phase)



SIEMENS

Picture-in-Picture Processor — SDA 9088

Preliminary Data — **MOS IC**

Features

- Input interface compatible to the data format of the Digital Multistandard Decoder (DMSD)SDA 9050/51 if Y, U, V output is used
- Decimation of the Y, U, V data for pictures sizes 1/9 and 1/16
- Intermediate storage of the inset picture (on-chip-memory)
- Readout of the data in the parent window, framing, generation of a SELECT signal
- Interpolation of the chrominance data rate to the luminance data rate
- RGB- or Y-, U-, V-signal generation
- D/A conversion
- Generation of an internal parent clock for an analog system environment from the sandcastle pulse by means of PLL

Type	Ordering Code	Package
SDA 9088	Q67100-H8630	P-DIP-28
SDA 9088-2	Q67100-H5043	P-DIP-28

Functional Description

The SDA 9088 Picture in Picture (PIP) processor combines two asynchronous picture sources so that a small moving picture (the inset picture) can be superimposed in a moving picture of normal size (the parent picture). The functions of the PIP are as follows **(see block diagram).**

The components of the video signal of the inset source must reach the SDA 9088 in digitized form **(figure 1)**. Amplitude resolution of the signal components is 5 bit at a sampling rate of 13.5 MHz for the luminance signal and 3.375 MHz for the chrominance signals.

The PIP handles picture reduction (decimation with horizontally and vertically acting filters), intermediate data storage in an integrated image memory (167.904 bits) as well as the output of the decimated picture.

The picture can be set 1/9 or 1/16 of its original size. In order to indicate the border between parent picture and inset picture the inset picture can be surrounded with a frame. Different signal sources can be identified by using different framing colors. The four corners of the parent picture are possible positions for the inset picture. The inset picture can also be inserted as a still picture, independently of the parent picture.

The output signals of the PIP are analog. Either RGB or Y, U, V signals can be output, whereby a 6-bit, broadband conversion is obtained in all components. If Y, U, V are selected, the inset picture signals must be clamped externally before switching between inset and parent channels. The sandcastle pulse of the parent channel can be used to control the clamping circuit. Clamping for RGB output signal is performed in an RGB processor (e.g. TDA 4580).

Only a few additional devices are required for a complete picture-in-picture system. **Application circuits 1 and 2** illustrate two possibilities for use of the PIP device. It can be operated both in systems with analog or digital signal processing or in any combinatioof the two.

If the CVBS input signal is to be decoded using an analog color decoder for the PIP, the analog/digital interface for the inset picture (ADIIP, SDA 9087) performs the conversion of the Y, U, V components into digital signals as well as the generation of the inset clocks BLNI and LL3I.

The PIP processes both 50 Hz/625 and 60 Hz/525 line signals. The field frequency can be 50 Hz or 60 Hz. For systems with Siemens TV feature box a field frequency of 100 Hz or 120 Hz is also possible by doubling the clock frequency LL3P (LL1.5P). Frame reproduction with 50 Hz or 60 Hz can also be set via the I^2C bus. Adaptation to the number of lines occurs automatically. If the field frequencies in the parent and inset channels are different, artifacts may result in the picture.

An unfavourable phase, varying with time, of the sync signals and clock of the parent channel may produce jumps in the position of the inset picture on the TV screen by a line or a pixel (ragged vertical borders). Similar condition for the sync signals of the inset channel may lead to slight instability within the inset picture.

Synchronization with the parent channel is performed via the horizontal and vertical sync signals HPS/SAND and VSP plus the LL3P clock (13.5 MHz) or in the case of standard conversion via the LL1.5P clock (27 MHz).

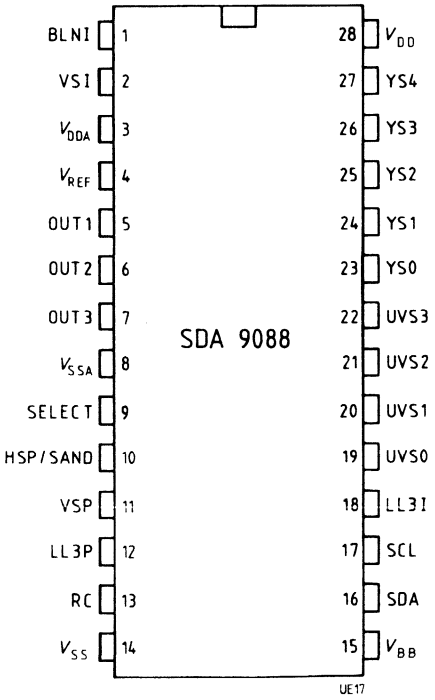
For an analog parent channel the LL3P clock can be generated from the sandcastle pulse (SAND) by an internal PLL.

The horizontal and vertical sync signals BLNI and VSI plus the LL3I clock (13.5 MHz) are used for synchronization with the inset source.

The interface between inset and parent channel is done by the on-chip memory. The memory write access is controlled by the inset clock and the read access controlled by the parent clock.

The SELECT output signal inserts the inset picture into the parent picture driving an external analog switch, e.g. the TDA 4580. All operation modes of the PIP can be controlled via the I^2C bus. Five registers can be used.

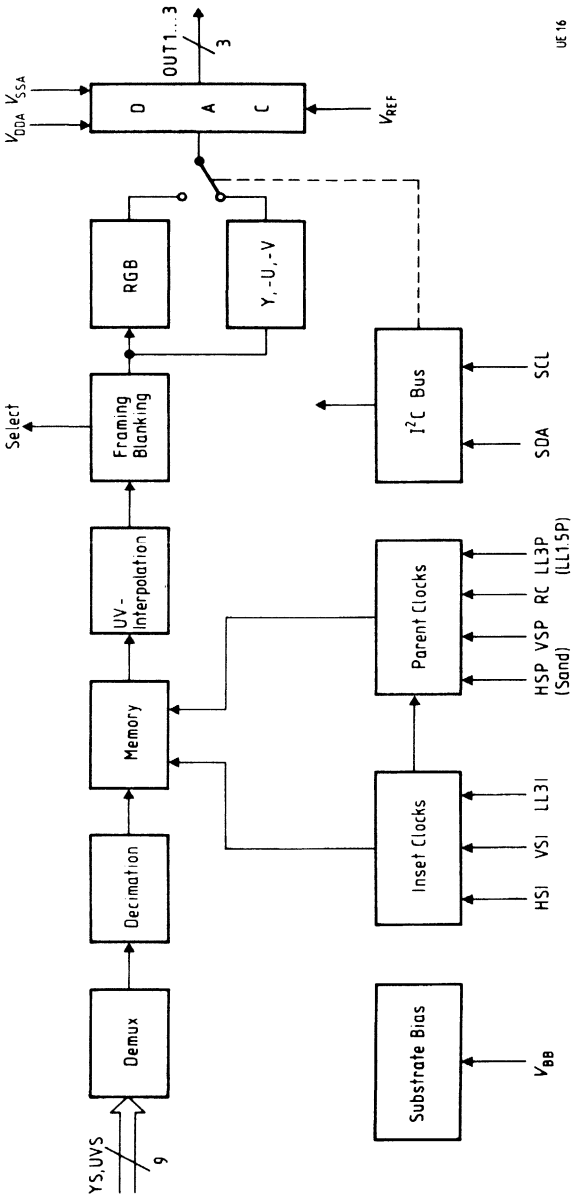
Pin Configuration
(top view)



Pin Definitions and Functions

Pin No	Symbol	Function	Definition
1	BLNI	Blanking inset	Inset lines synchronization
2	VSI	Vertical synchron inset	Inset field synchronization
3	V_{DDA}	Analog supply	V_{DD} power supply for D/A converter and PLL
4	V_{REF}	Reference voltage generation	Current mirror for OUT1-OUT3
5-7	OUT1-OUT3	Analog R, G, B, Y, UV-outputs	Analog RGB-, YUV outputs
8	V_{SSA}	Analog ground	Ground for D/A converter and PLL
9	SELECT	SELECT	Valid signals at OUT1-OUT3
10	HSP/SAND	Horizontal synchron/ Sandcastle parent	Parent line synchronization
11	VSP	Vertical synchron parent	Parent field synchronization
12	LL3P	Line locked clock parent	Parent system clock
13	RC	RC	RC network for PLL loop to V_{SSA}
14	V_{SS}	Digital ground	Ground
15	V_{BB}	Substrate bias	V_{BB} smoothing
16	SDA	Serial data	I^2C data
17	SCL	Serial clock	I^2C clock
18	LL3I	Line locked clock inset	Inset system clock
19-27	UV0-UV3, Y0-Y4	UV, Y data	Digital YUV input data
28	V_{DD}	Digital supply	V_{DD} delay

Block Diagram



Circuit Description

The DMSD compatible data are transferred under the control of LL3I, BLNI and VSI on pins YS0-YS4 and UVS0-UVS3. The decimated data are stored automatically. Either R, G, B or Y, U, V analog signals are available at the outputs OUT1-OUT3. The validity of the signals is identified by SELECT = 1. In a digital system environment the input is controlled by LL3P, HSP and VSP. In an analog system environment a line frequency signal has to be applied to the pin called SAND. An internal PLL can then generate the internal output clock pulses. In this case an RC network must be connected to pin RC to act as part of a low-pass filter.

Inset Data Reduction

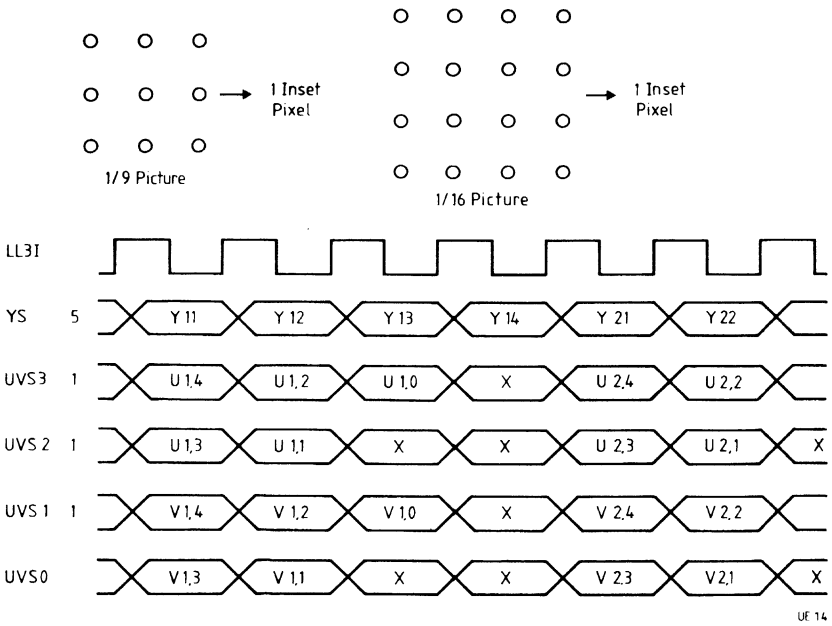
The data rate at the inputs YS0-YS4, UVS0-UVS3 is 13.5 MHz in multiplexed format (DMSD compatible), **see figure 1.**

In order to reduce the quantity of data which have to be stored and to prevent artifacts in the inset picture, nine pixels are processed into an inset pixel for a 1/9 picture and 16 pixels for 1/16 picture.

This is done by horizontal and vertical averaging of pixels:

Figure 1

Input Data Format



The pixel and line number of the inset picture depend on the standard of the inset channel and on the selected picture size:

Table 1

Inset Picture Size

Picture Size	TV Standard (Inset) (Frame Line Number)	Pixel Number P			Line Number L
		Y	U	V	
1/9	625	212	53	53	88
1/9	525	212	53	53	76
1/16	625	160	40	40	66
1/16	525	160	40	40	57

Intermediate Storage of Inset Picture

The PIP memory has a capacity of 167.904 bits large enough to store the data of the inset picture and to output data, which are synchronized with the parent channel. The memory organisation is 88 × 212 × 9 bits. Its size is oriented on the maximum pixel and line number required (1/9 picture, 625 lines).

Data are written in with the inset and read out with the parent clock frequency.

Table 2 shows the processed sections of the original picture stored in the memory.

To avoid strong 25-Hz flicker, only every second field of the inset source is processed.

Table 2

Processed Sections of Original Picture (BWL, BWP = Starting Point)

Picture Size	TV Standard (Inset) (Frame Line Number)	Pixel Number P		Section	
		TV Line (BWL)	Pixel (BWP)	Line Number	Pixel Number
1/9	625	36	13	264	636
1/9	525	26	13	228	636
1/16	625	36	17	264	640
1/16	525	26	17	228	640

Output of Data in Parent Window

The four corners of the parent picture are foreseen as positions for inserting the inset picture. To enable compatibility to different system configurations, readout from memory can be shifted horizontally in 63 steps by max. 252 LL3P cycles and vertically in 15 steps by max. 30 lines in the parent field setting the control bits RDH and RDV in control register 2 and 3.

The coordinates BRP, BRL of the normal location of all four insertion positions are given in **table 4** for RDH = RDV = 8.

The SELECT signal goes high during the display of the inset picture. Outside of the inset picture SELECT signal is low and the analog outputs OUT1-OUT3 provide the black level. The external wiring can produce a delay between the SELECT signal and the analog outputs. This delay can be compensated for by bits SD0-SD2 in register 2 via the I^2C bus.

A frame with one of eight colors can be inserted using control bits FRON, COL0-2. The width of the frame is fixed at three lines and six pixels. The size is shown in **table 3.**

Figure 2

Insertion Positions of Inset Picture

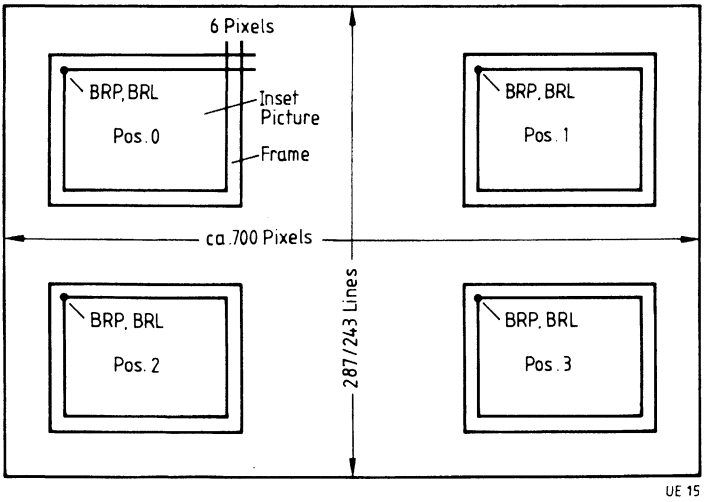


Table 3

Frame Size

Picture Size (with Frame)	TV Standard (Inset)	TV Standard (Parent)	POS	Horiz. Bar		Vert. Bar	
				Pixel Number	Line Number	Pixel Number	Line Number
1/9	625	X	0	224	3	6	94
1/9	625	X	1	224	3	6	94
1/9	525	X	0	224	3	6	82
1/9	525	X	1	224	3	6	82
1/16	625	X	0	172	3	6	72
1/16	625	X	1	172	3	6	72
1/16	525	X	0	172	3	6	63
1/16	525	X	1	172	3	6	63
1/9	X	625	2	224	3	6	94
1/9	X	625	3	224	3	6	94
1/9	X	525	2	224	3	6	94[1)]
1/9	X	525	3	224	3	6	94[1)]
1/16	X	625	2	172	3	6	72
1/16	X	625	3	172	3	6	72
1/16	X	525	2	172	3	6	63
	X	525	3	172	3	6	63

X = don't care

1) Clamping to minimal RDV if a 625-standard picture has to be inserted; the vertical position cannot be changed by software.

Table 4

Display of Inset Picture

Position	TV Standard (Parent) (Frame Line Number)	Picture Size	Location of Top Left Corner Point		
			TV Line (FL)		Pixel (FP)
			NINT	INT	
0	625	X	59	30	54
0	525	X	43	22	54
1	625	1/9	59	30	448
1	525	1/9	43	22	448
1	625	1/16	59	30	502
1	525	1/16	43	22	502
2	625	1/9	367	184	54
2	525	1/9	295	148	54
2	625	1/16	411	206	54
2	525	1/16	335	168	54
3	625	1/9	367	184	448
3	525	1/9	295	148	448
3	625	1/16	411	206	502
3	525	1/16	335	168	502

Pixel data related to positive HSP edge
Line data related to positive VSP edge

Interpolation of Chrominance Data Rate to Luminance Data Rate

To avoid chrominance artifacts after D/A conversion and for digital RGB conversion, the data rate of the chrominance signals is quadrupled in order to match the luminance data rate. This is done by repeating the chrominance data twice followed by low-pass filtering.

RGB, Y, U, V Outputs

A digital RGB matrix converts the Y, U, V data in R, G, B data. The outputs of the matrix are:

$$R = Y + 0.75\ V$$
$$G = Y - 0.375\ V - 0.1875\ U$$
$$B = Y + U$$

If not required a by-pass can be switched allowing the Y, U, V data to reach the D/A converters at the output of the RGB matrix, the chrominance signals U and V being inverted at the same time.

D/A Conversion

SDA 9088 includes three 6-bits D/A converters. Each D/A converter delivers a current through an external resistor that is to be connected between OUT1-OUT3 and V_{SS}. The resistor value determines the output voltages **(see application circuit).** The assignment of outputs OUT1-OUT3 to R, G, B and Y, U, V is shown in **table 5.**

Table 5

Assignment of Output Signals to OUT1-OUT3

Output	RGB	YUV
OUT1	R	– V
OUT2	G	Y
OUT3	B	– U

PLL

In an analog system environment (PLLL = 1) the internal PLL can be activated. Input LL3P is switched off in VCO mode. The internally generated output clock rate is:

$f_T = 864 \cdot f$ (SAND)

I²C BUS

Organization of I²C Bus Registers

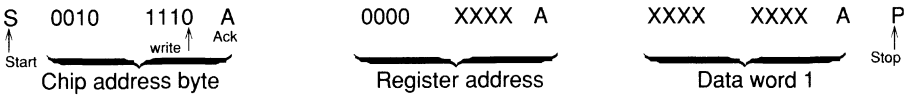
SDA 9088 has the device address

$$00101110 = 2E_H$$

Applying the supply voltage V_{DD} produces a power-up reset. The bus lines SDA and SCL are enabled. All bits in the registers except bit PLL (D3 in Register 0) are set to 0. Bit PLL is set to 1.

The I²C bus interface works as a slave receiver and only functions if the inset clock LL3I is available.

Write Operation



After writing a byte into any register, the register address is automatically incremented for the write access to the next register.

The following table shows the functions that can be set on the I²C bus and define the data bytes.

Table 6

I²C Bus Register

Function	SUB-Address	Data Byte							
		D7	D6	D5	D4	D3	D2	D1	D0
CONTROL 0	00	0	0	STILL	SIZE	PPLL	NINT	OUT	PON
CONTROL 1	01	0	0	0	0	COL2	COL1	COL0	FRON
CONTROL 2	02	0	SD2	SD1	SD0	RDV3	RDV2	RDV1	RDV0
CONTROL 3	03	POS1	POS0	RDH5	RDH4	RDH3	RDH2	RDH1	RDH0
CONTROL 4	04	CON0	CON1	CON2	CON3	HSPINT	SOP	PL27	HSP5

All bits which are not used have to be set to "0".

The bits are numbered in the reverse order to the data stream of the I²C bus.

Register 0 (Address 00_H)

Bit	Function	Name	Remarks
d0	0 = PIP OFF 1 = PIP ON	PON	If d0 = 0, no SELECT generated
d1	0 = Y, -U, -V 1 = RG	OUT	Output format
d2	0 = Field mode 1 = Frame mode	NINT	Reproduction mode
d3	0 = PLL inactive 1 = PLL active	PPLL	Parent clock generation. External clock has to be connected to LL3P is PPLL = 0.
d4	0 = 1/9 1 = 1/16	SIZE	Picture size
d5	0 = normal picture 1 = still picture	STILL	Still/moving picture
d6, d7	not assigned		

Register 1 (Address 01_H)

Bit	Function	Name	Remarks
d0	0 = without frame 1 = with frame	FRON	
d1-d3	frame colour d3 d2 d1 0 0 0 = blue 0 0 1 = violet 0 1 0 = green 0 1 1 = white 1 0 0 = red 1 0 1 = yellow 1 1 0 = orange 1 1 1 = cyan	COL0- COL2	
d4-d7	without function		

Register 2 (Address 02_H)

Bit	Function	Name	Remarks
d0-d3	Read delay vertical in BLNP period d3 d2 d1 d0 0 0 0 0 = 0 0 0 0 1 = 2 0 0 1 0 = 4 : 1 1 0 1 = 26 1 1 1 0 = 28 1 1 1 1 = 30	RDV0– RDV3	Increment in 2 BLNP period
d4-d6	SELECT delay in LL3P period d6 d5 d4 0 0 0 = 0 0 0 1 = 1 0 1 0 = 2 0 1 1 = 3 1 0 0 = 4 1 0 1 = 5 1 1 0 = 6 1 1 1 = 7	SD0- SD2	
d7	without function		

Register 3 (Address 03H)

Bit	Function	Name	Remarks
d0-d5	Read delay horizontal d5 d4 d3 d2 d1 d0 0 0 0 0 0 0 = 0 0 0 0 0 0 1 = 4 0 0 0 0 1 0 = 2 ⋮ 1 1 1 1 0 1 = 244 1 1 1 1 1 0 = 248 1 1 1 1 1 1 = 252	RDH0–RDH5	Increment in 4 LL3P period
d6, d7	Insert picture location d7 d6 0 0 top left 0 1 top right 1 0 down left 1 1 down right	POS0-POS1	

Register 4 (Address 04H)

Bit	Function	Name	Remarks
d0	0 = SANDCASTLE at HSP 1 = TTL level at HSP	HSP5	Level switch
d1	0 = 13.5 MHz PLL 1 = 27 MHz PLL	PL27	Switch off the VCO clock prescaler
d2	0 = SELECT PULLUP INTERN 1 = SELECT PULLUP EXTERN	SOP	Open drain for SELECT output
d2	0=HSP EXTERN 1=HSP INTERN	HSPINT	HSP from the PLL divider For PLL d3 =1 has to be set
d4-d7	Contrast DA converter	CON 0-3	Applying an external resistor between V_{REF} and V_{SS} the same output voltage is reached if R = 6.8kΩ and d7 ...d4 = 0000 are selected. d4 = LSB d7 = MSB

Absolute Maximum Ratings
T_A = 0 to 70 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{DD}	– 1	6	V
Voltages at V_{BB}*	V_{BB}			V
HSP/SAND	V_{IN}	– 1	10.5	V
All the rest	V_{IN}	– 1	6	V
Ambient temperature	T_A	– 20	70	°C
Storage temperature	T_{stg}	– 20	125	°C
Power dissipation	P_{tot}		1	W

*Note: the voltage V_{BB} is internally generated.

Operating Range
T_A = 25 °C

Supply voltage	V_{DD}	4.5	5.5	V
Ambient temperature	T_A	0	70	°C

Characteristics
T_A = 25 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply voltage	V_{DD}/V_{DDA}	4.5	5	5.5	V	
Current consumption dig. analog	I_{DD}	13 5	40 10	70 20	mA mA	without load LL3I = 13.5 MHz LL3P = 27 MHz

Inputs
YS0-YS4, UVS0-UVS3,
LL3I, BLNI, VSI, LL3P, VSP

H-input voltage L-input voltage	V_{IH} V_{IL}	2.3 – 1.0		V_{DD} 0.8	V V	
Input capacitance	C_I			7	pH	
Input leakage current	I_L			10	µA	V_{IH} = 5.5 V

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Select						
H-output voltage	V_{QH}	2.4		V_{DD}	V	$-I_{QH}$ = 0.2 mA SOP = 0
L-output voltage	V_{QL}	0		0.4	V	I_{QH} = 1.6 mA SOP = 0
H-output voltage	V_{QH}			V_{DD}	V	SOP = 1
L-output voltage	V_{QL}	0		0.1	V	I_{QL} = 1.6 mA SOP = 1
Load capacitance	C_L			50	pF	
Transition period	t_r, t_f			15	ns	
Input HSP / SAND						
H-input voltage	V_{IH}	2.3		V_{DD}	V	PPLL = 0 or HSP5 = 1
L-input voltage	V_{IL}	− 1.0		0.8	V	PPLL = 0 or HSP5 = 1
H-input voltage	V_{IH}	V_{DD}+2.5 5		10	V	PPLL = 1 and HSP5 = 0
L-input voltage	V_{IL}	0		V_{DD}+0.5 5	V	PPLL = 1 and HSP5 = 0
Input capacitance	C_I			7	pF	
Input leakage current	I_L	− 10		10	µA	$0 \le V \le V_{DD} + 0.5$ V
Input current	I_{IH}			1	mA	$V_{DD} + 2.5 \le V_I \le 11$

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Input SCL, In/Output SDA							
L-input voltage	V_{IL}	– 1		1.5	V		
H-input voltage	V_{IH}	3		V_{DD}	V		
Input leakage current	I_L			10	µA		
Input capacitance	C_I			7	pF		
Input frequency	f_{SCL}			100	kHz		
Transition period	t_r, t_f			2	µs		
Max. capacitance at bus	C_{max}			400	pF		
Fall time	t_f			0.2	µs	from 3 V to 1 V	
SDA by replay message	V_{AL}	0		0.4	V	I_{AL}= 3 mA	
Output OUT1...3, RGB Mode*							
Output current	I_Q	0	– 1.57		mA	V_{DDA} = 5 V	
Output voltage H	V_{QH}		1.07		Vpp	RGB-Mode	6
Output voltage L	V_{QL}	0			mV	RGB-Mode	6
Numerical range		0		63			
Resolution	$I_{Q\,quant}$		25		µA		
Load resistance	R_L		680		Ω		7
Output capacitance	C_Q			7	pF		7
Coupling capacitance	C_C		47		nF		7
Time constant	t_{const}			35	ns	BW = 4.5 MHz	7
Output voltage range	$V_{Q\,max}$	V_{SSA}		2	V		
Differential non-linearity		– 0.5		0.5	LSB		
Maximum difference between the voltage levels of the RGB outputs at the same full modulation		– 3		3	%		

*The nominal color saturation is achieved in RGB mode by an amplitude ratio of 0.72/0.93/1for Y/U/V at the inputs.

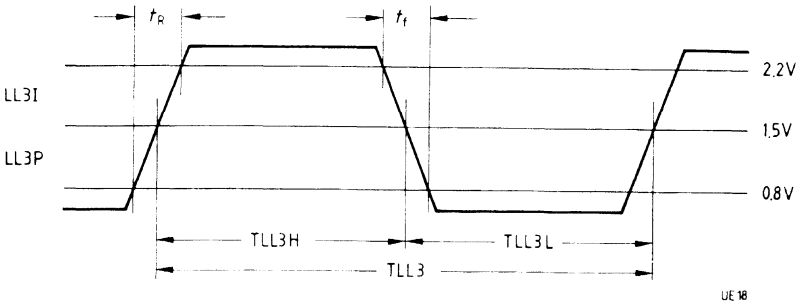
Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Output OUT1 (V) **YUV Mode**							
Output current	I_Q	0	– 1.57		mA	V_{DDA} = 5 V	
Output voltage H Output voltage L	V_{QH} V_{QL}		1.070		Vpp mV	YUV-Mode YUV-Mode	6 6
Numerical range		0		63			
Resolution	$I_{Q\,quant}$		25		µA		
Load capacitance	R_L		680		Ω		7
Output capacitance Coupling capacitance	C_Q C_C		 47	7	pF nF		7 7
Time constant	t_{const}			35	ns	BW = 4.5 MHz	7
Output voltage range		V_{SSA}		2	V		
Differential non-linearity Maximum difference between the voltage levels of the YUV outputs at the same full modulation.		– 0.5 – 3		0.5 3	LSB %		
Output OUT2 (V) **YUV Mode**							
Output current	I_Q	0	– 1.57		mA		
Output voltage H Output voltage L	V_{QH} V_{QL}		0.43 0		Vpp mV	YUV-Mode YUV-Mode	6 6
Numerical range		0		63			
Resolution	I_{Qquant}		25		µA		
Load capacitance	R_L		270		Ω		7
Output capacitance Coupling capacitance	C_Q C_C		 47	7	pF pF		7 7
Time constant	t_{const}			35	ns	BW = 4.5 MHz	7
Output voltage range		V_{SSA}		2	V		
Differential non-linearity Maximum difference between the voltage levels of the YUV outputs at the same full modulation.		– 0.5 – 3		0.5 3	LSB %		

Characteristics (cont'd)

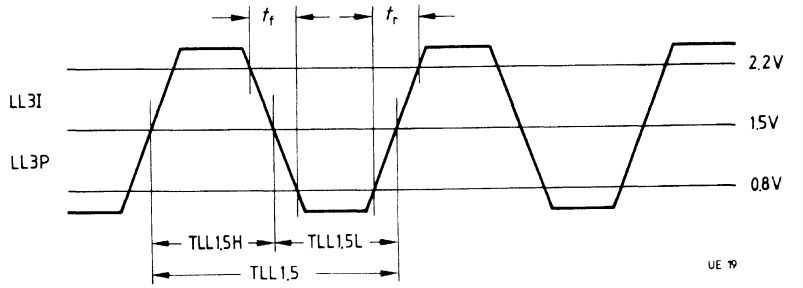
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Output OUT3 (U) **YUV Mode**							
Output current	I_Q	0	– 1.57		mA	V_{DDA} = 5 V	
Output voltage H Output voltage L	V_{QH} V_{QL}		1.42 0		Vpp mV	YUV-Mode YUV-Mode	6 6
Numerical range		0		63			
Resolution	I_{Qquant}		25		µA		
Load capacitance	R_L		900		Ω		7
Output capacitance Coupling capacitance	C_Q C_C			7	pF nF		7 7
Time constant	t_{const}			35	ns	BW = 4.5 MHz	7
Output voltage range		V_{SSA}		2	V		
Differential non-linearity Maximum difference between the voltage levels of the YUV outputs at the same full modulation.		– 0.5 – 3		0.5 3	LSB %		
Output RC							
Pulse current	I_P		0.8		mA		8
First external capacitance Second external capacitance	C_1 C_2		22 470		µF µF		
Resistance	R		4.7		kΩ		
Output capacitance	C_Q			7	pF		

Measuring Circuit 1



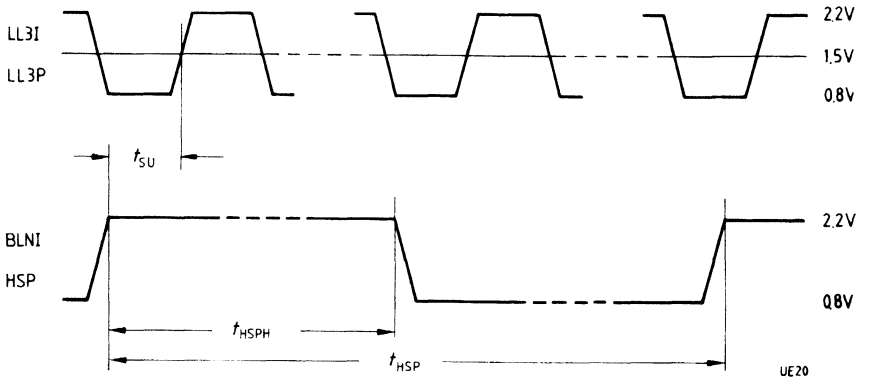
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
LL3I, LL3P					
Period time	T_{LL3}	68	74	80	ns
Rise time	t_r			3	ns
Fall time	t_f			3	ns
Sampling ratio	T_{LL3H}/T_{LL3}	0.43		0.57	

Measuring Circuit 2



Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
LL1.5P					
Period time	$T_{LL1.5}$	34	37	40	ns
Rise time	t_r			3	ns
Fall time	t_f			3	ns
Sampling ratio	$T_{LL1.5H}/T_{LL1.5}$	0.43		0.57	

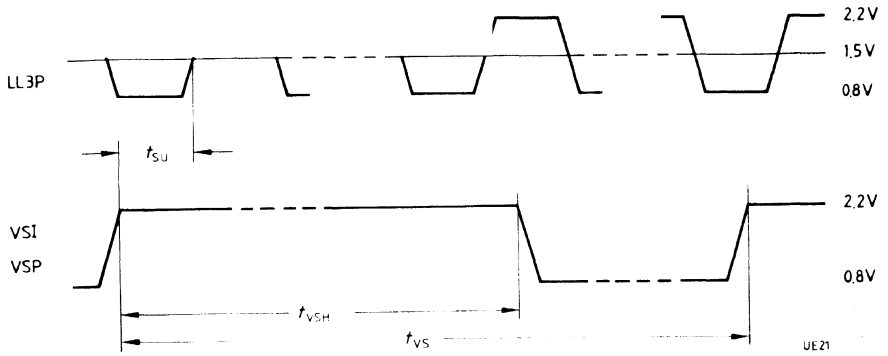
Measuring Circuit 3



Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
BLNI					
Period time 625 lines	t_{BLN}	864	864	864	T_{LL3I}
Period time 525 lines	t_{BLN}	858	858	864	T_{LL3I}
High time	t_{BLNH}	1		857	T_{LL3I}
Set-up time	t_{SU}	12			ns
HSP					
Period time 625 lines	t_{HSP}	864	864	864	$T_{LL3P}/T_{LL1.5P*}$
Period time 525 lines	t_{HSP}	858	858	864	$T_{LL3P}/T_{LL1.5P*}$
High time	t_{HSP}	1		857	$T_{LL3P}/T_{LL1.5P*}$
Set-up time	t_{SU}	12			ns

*by standard conversion

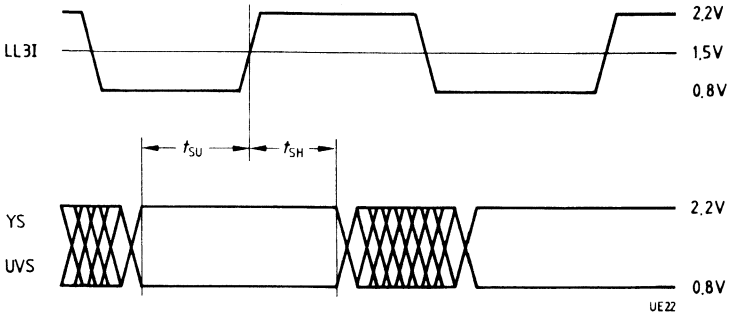
Measuring Circuit4



Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
VSI					
Period time 625 lines	t_{VS}		312.5		T_{BLNI}
Period time 525 lines	t_{VS}		262.5		T_{BLNI}
High time	t_{VSH}	1			T_{LL3I}
Set-up time	t_{SU}	12			ns
VSP					
Period time 625 lines	t_{VS}		312.5/625*		T_{HSP}
Period time 525 lines	t_{VS}		262.5/525*		T_{HSP}
High time	t_{VSH}	1			T_{LL3P}
Set-up time	t_{SH}	12			ns

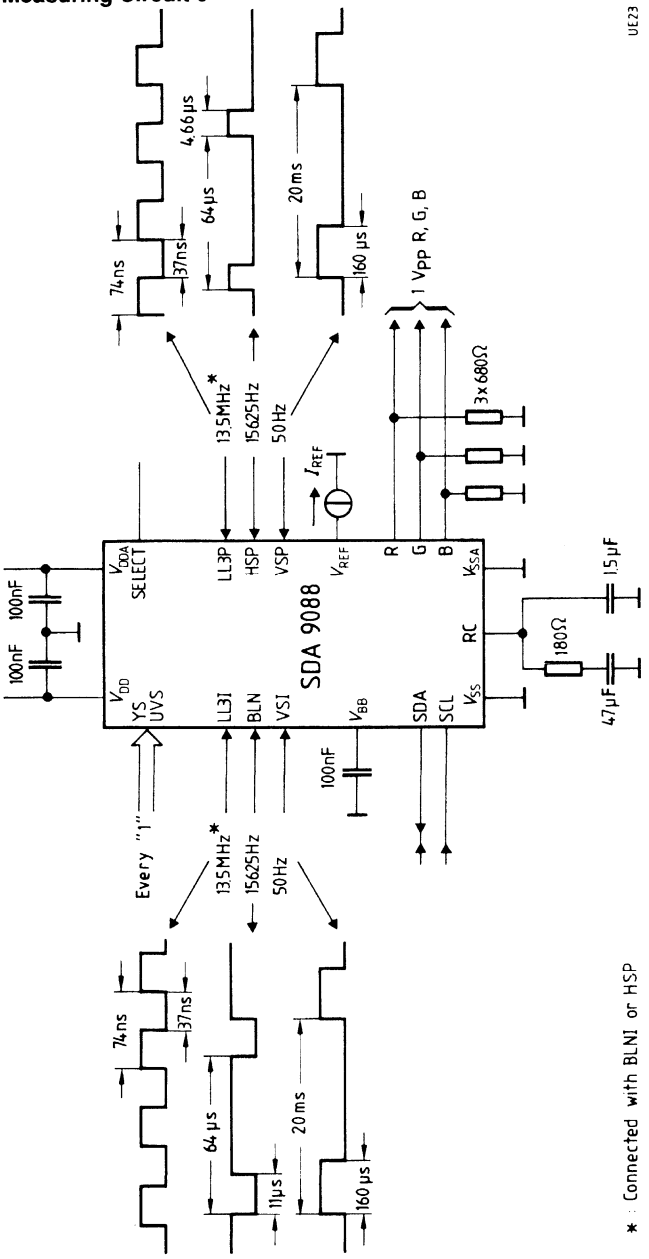
*by progressive scanning

Measuring Circuit 5

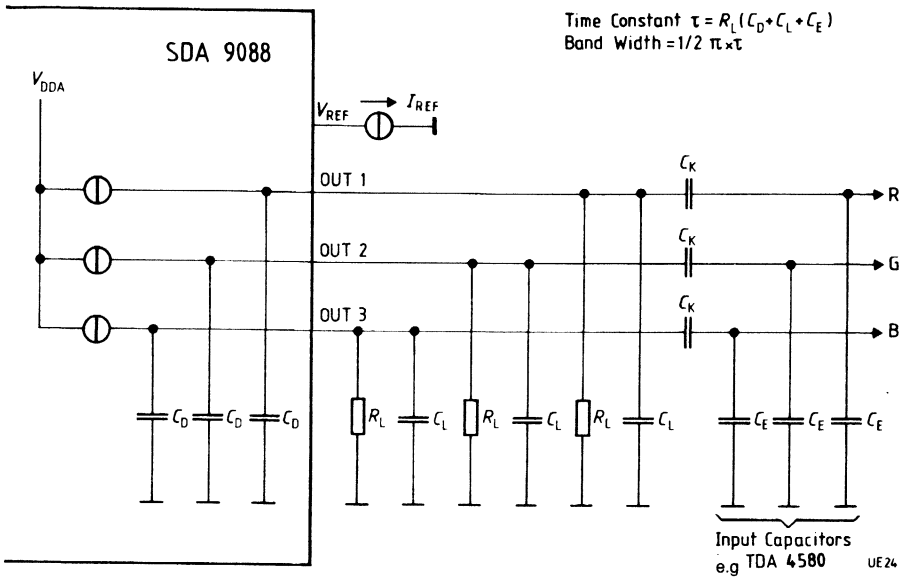


Parameter	Symbol	Limit Values		Unit
		min.	max.	
YS, UVS				
Set-up time	t_{SU}	12		ns
Hold time	t_{SH}	3		ns

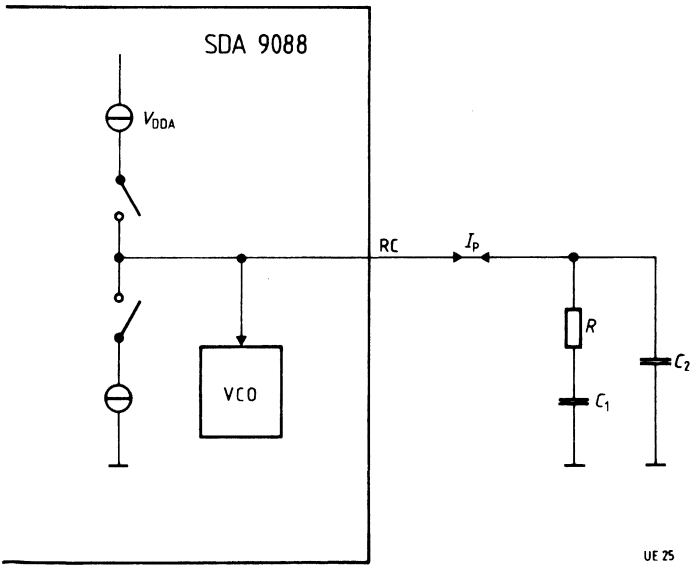
Measuring Circuit 6



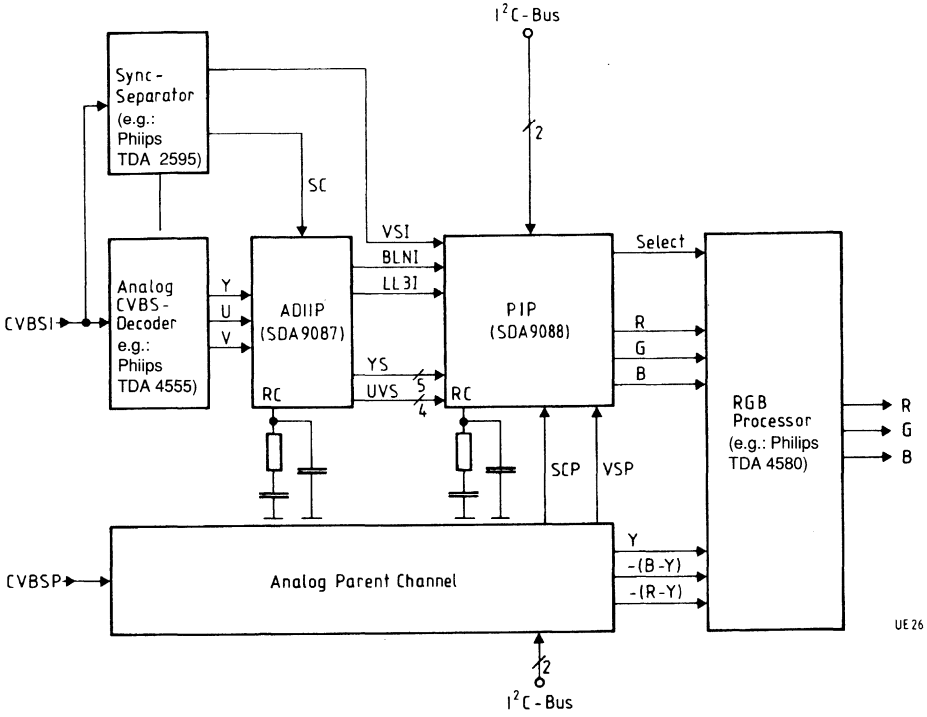
Measuring Circuit 7



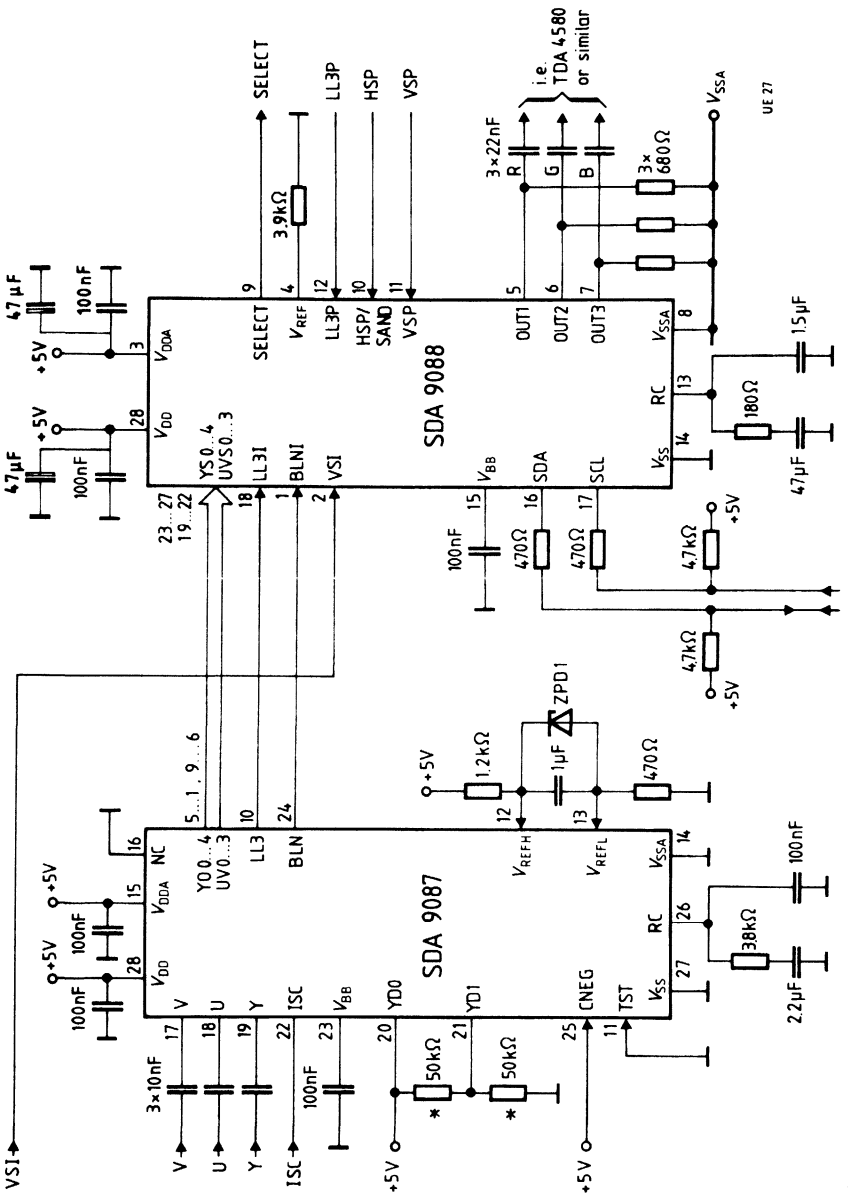
Measuring Circuit 8



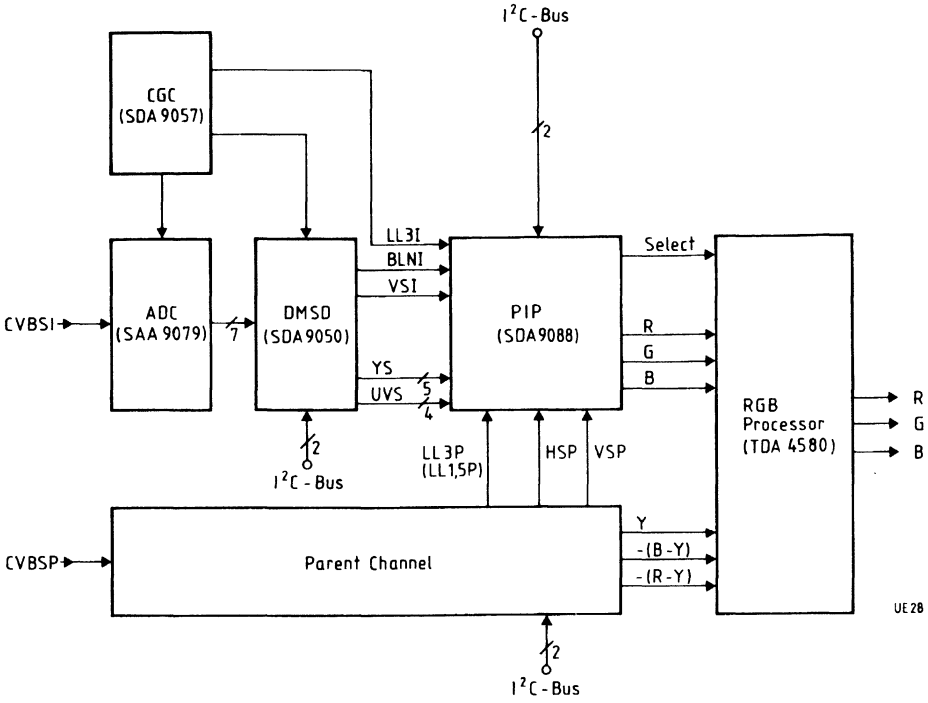
Application Circuit 1a



Application Circuit 1b



Application Circuit 2



SIEMENS

FM IF Amplifier with Demodulator

TBA 120

Bipolar IC

Features

- Outstanding limiting qualities
- Few external components
- Terminal for video recorder
- AF output voltage independent of supply voltage
- Insensitive to hum
- Very little residual IF

Type	Ordering Code	Package
TBA 120 T	Q67000-A919	P-DIP-14
TBA 120 UB	Q67000-A920	P-DIP-14

The symmetrical 8-stage amplifier with symmetrical coincidence demodulator for amplifying, limiting, and demodulating frequency-modulated signals, is especially suited for the sound IF units in TV sets. In addition to the controlled AF output, an uncontrolled AF output and an AF input for the connection of video recorders is available.

TBA 120 T: Input and demodulator matched to ceramic resonators
TBA 120 UB: Input and demodulator matched to *LC* networks.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	18	V
Voltage	V_5	6	V
Current	I_4	5	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating Range

Supply voltage	V_S	10 to 18	V
Ambient temperature	T_A	– 15 to 70	°C
Frequency	f	0 to 12	MHz

Characteristics
V_S = 12 V; T_A = 25 °C, Q_B approx. 45, f_{IF} = 5.5 MHz

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption	I_S	9.5	13.5	17.5	mA
IF voltage gain V_6 / V_{14}	G_v		68		dB
IF output voltage with limiting at each output	$V_{Q\,pp\,6\text{-}10}$	175	250	325	mV
Output resistance	$R_{Q\,8}$,$R_{Q\,12}$	0.8	1.1	1.4	kΩ
Input resistance	$R_{I\,3}$	1.4	2.0	2.6	kΩ
Internal resistance	$R_{I\,4}$		12	16	Ω
DC level of output signal	V_8	3.4	4.0	4.7	V
V_I = 0	V_{12}	4.4	4.9	6.3	V
Stabilized voltage	V_4	4.2	4.8	5.3	V
Residual IF voltage without deemphasis	V_8 V_{12}		20 30		mV mV
AF gain (AF not attenuated)	V_8 / V_3	6	7.5	8.5	
Attenuation $R_{4\text{-}5}$ = 5 kΩ; $R_{5\text{-}1}$ = 13 kΩ	V_{AF8}	20	30	40	dB
Range of volume control	$\frac{V_{AF8\,max}}{V_{AF8\,min}}$	70	85		dB
Resistance	$R_{4\text{-}5}$ [1])	1		10	kΩ
Input voltage for limiting Δf = ± 50 kHz; f_{mod} = 1 kHz	$V_{I\,lim}$		30	60	µV
Hum suppression	V_S / V_{11} V_{12} / V_{11}		35 30		dB dB
Signal-to-noise ratio (V_I = 10 mV)	$a_{S/N}$	80	85		dB
Noise voltage (in acc. with DIN 45405)	V_n			70	µV
Input impedance	$R_{Q\,7\text{-}9}$		5.4		kΩ

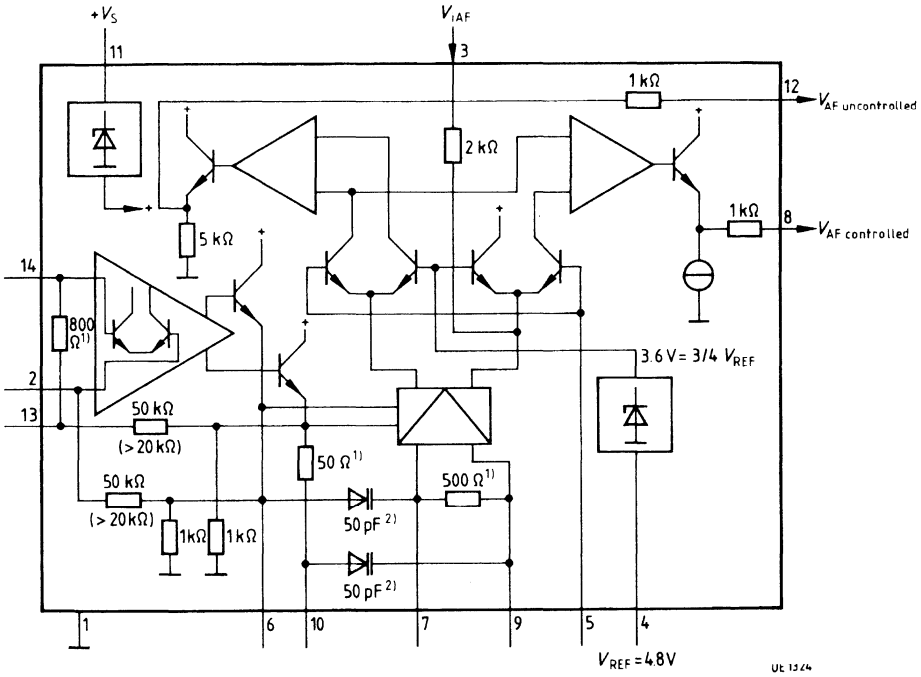
1) If DC volume control is not used, pin 4 has to be connected directly to pin 5.

Characteristics

V_S = 12 V; T_A = 25 °C, Q_B approx. 45, f_{IF} = 5.5 MHz

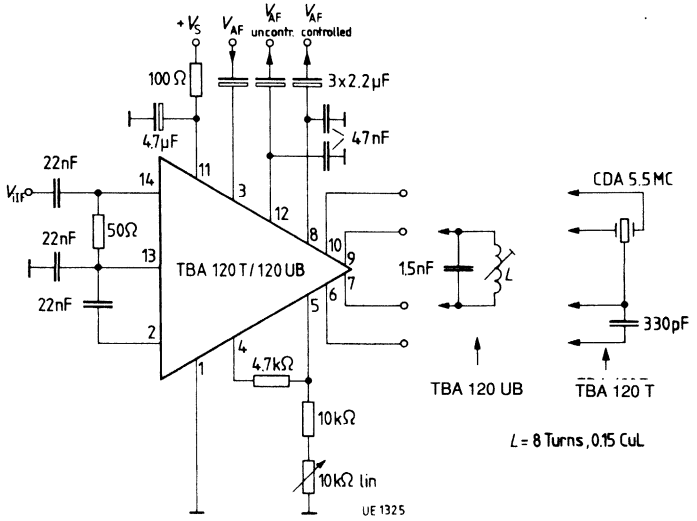
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
TBA 120 T only:					
AF output voltage	$V_{8\,rms}$	650	900	1100	mV
Δf = ± 50 kHz; f_{mod} = 1 kHz	$V_{12\,rms}$	400	650	1000	mV
Input impedance	Z_I		800/5		Ω/pF
AM suppression V_I = 500 µV; Δf = ± 50 kHz; m = 30%; f_{mod} = 1 kHz	a_{AM}	50	60		dB
Bridging resistance	$R_{13\text{-}14}$			1	kΩ
TBA 120 UB only:					
AF output voltage	$V_{8\,rms}$	850	1200	1700	mV
Δf = ± 50 kHz; V_I = 10 mV; f_{mod} = 1 kHz; THD = 4%	$V_{12\,rms}$	600	1000	1600	mV
Input impedance (f_I = 5.5 MHz)	Z_I	15/6	40/4.5		kΩ/pF
AM suppression Δf = ± 50 kHz; V_I = 500 µV; f_{mod} = 1 kHz; m = 30%	a_{AM}	50	60		dB
Total harmonic distortion Δf = ± 25 kHz; V_I = 10 mV; f_{mod} = 1 kHz	THD		1.3	2.5	%
Noise Voltage (in acc. with DIN 45405)	V_n			50	µV

Block Diagram

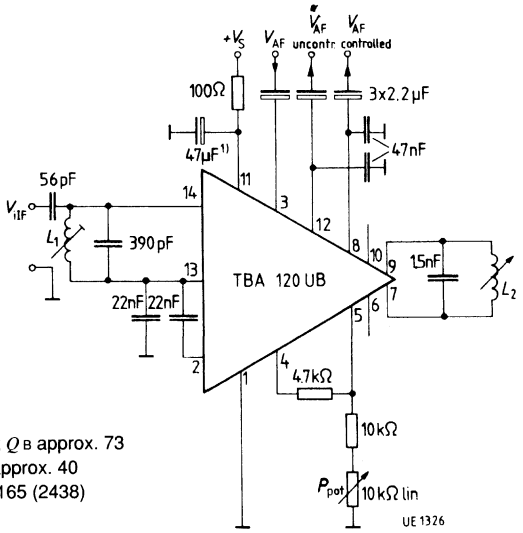


1) only TBA 120 T
2) only TBA 120 UB

Test Circuit (5.5 MHz)

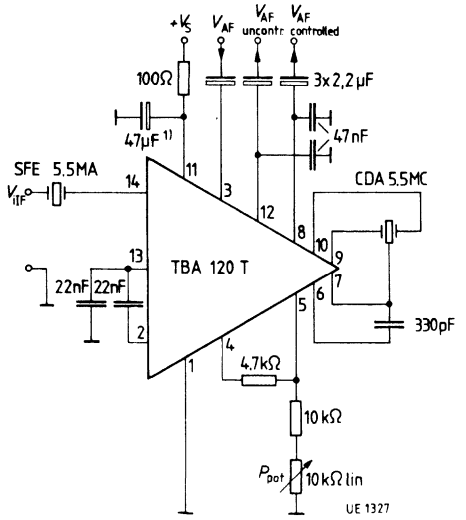


Application Circuit TBA 120 UB for 5.5 MHz



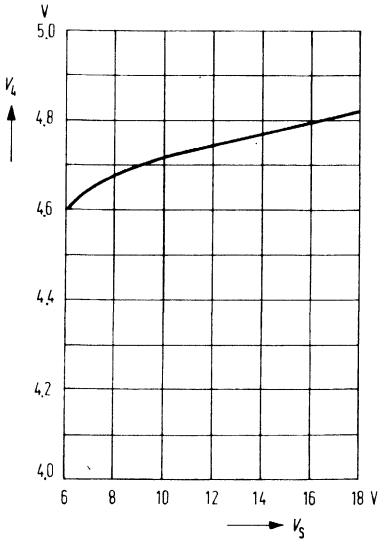
L_1: 20 turns 15 × 0.05 CuLs; Q_B approx. 73
L_2: 9 turns 0.25 CuLs; Q_B approx. 40
Coil assembly Vogt D41 – 2165 (2438)
without cup core

Application Circuit TBA 120 T for 5.5 MHz

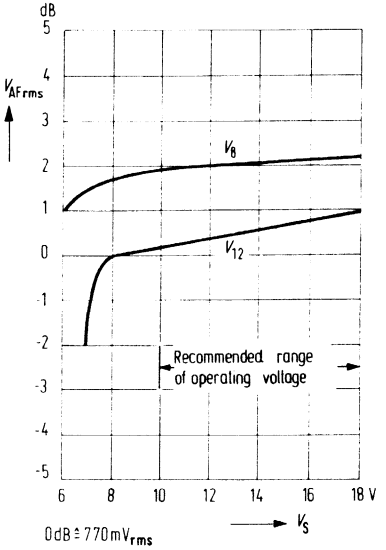


1) Omitting the electrolytic capacitor 47 µF at pin 11 changes the volume-control range.

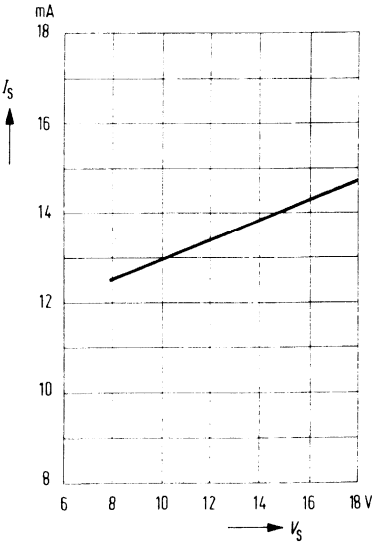
Z voltage versus supply voltage



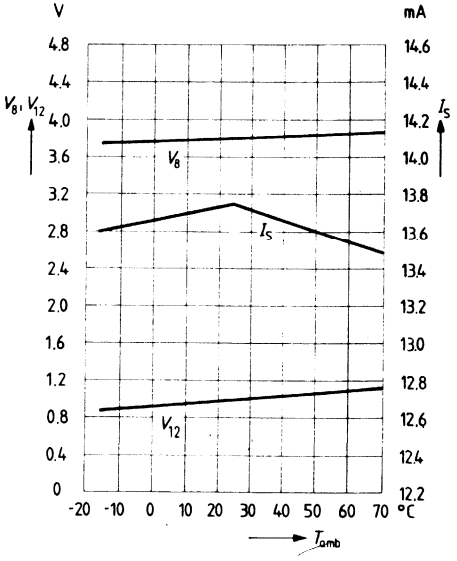
AF output voltage versus supply voltage



Current consumption versus supply voltage

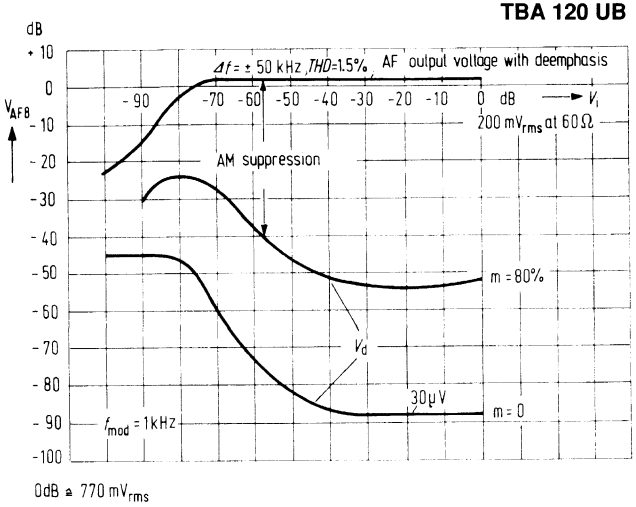


AF output voltage and current consumption versus ambient temperature



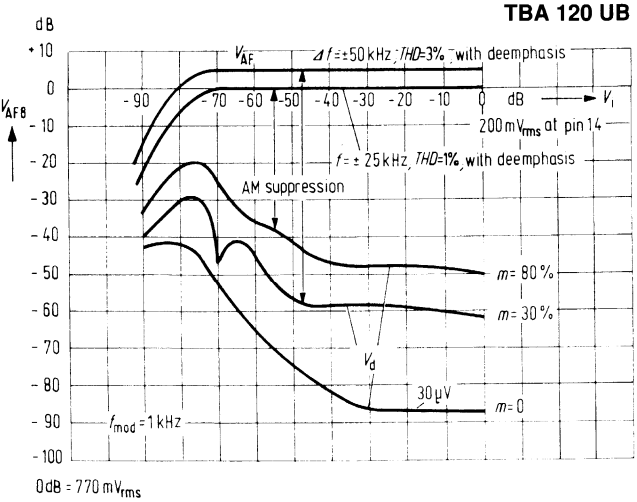
AF output voltage and disturbance voltage versus input voltage
(Input wired with SFE 5.5 MA/Murata)

TBA 120 UB

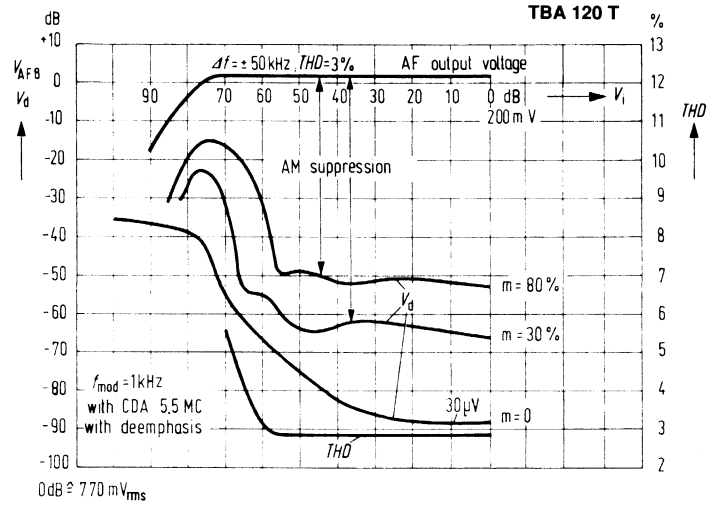


AF output voltage and disturbance voltage versus input voltage
(Input 60 Ω impedance broadband)

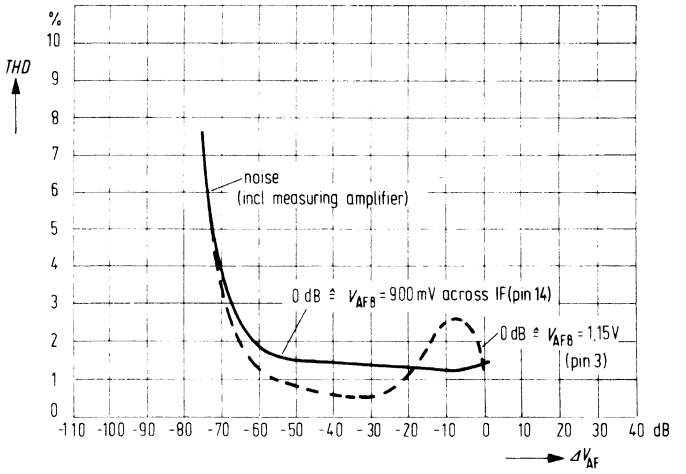
TBA 120 UB



AF output voltage (pin 8) disturbance voltage, and total harmonic distortion versus input voltage

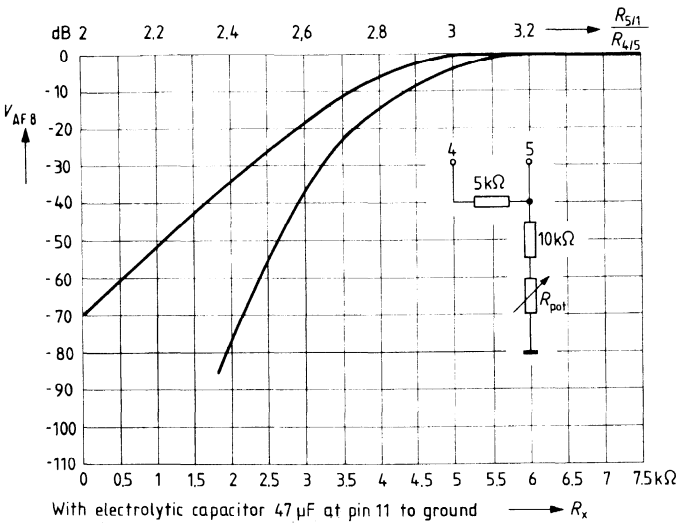


Total harmonic distortion versus volume control

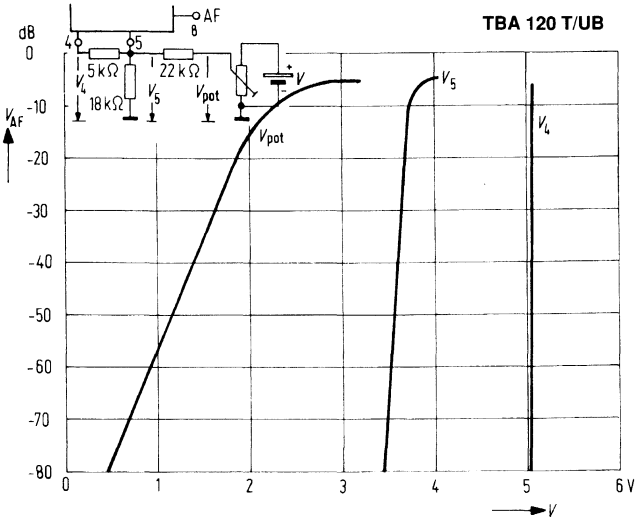


Spread

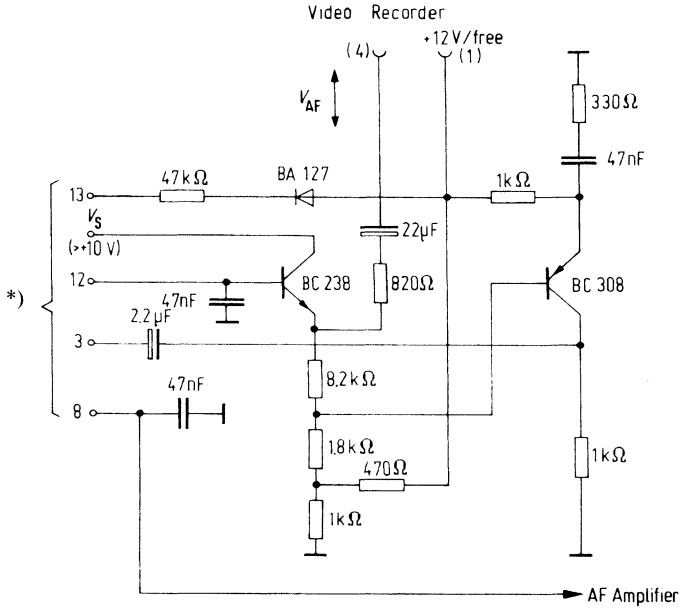
AF output voltage (pin 8) versus potentiometer resistance and versus ratio of resistance



AF output voltage (pin 8) versus voltage fed into pin 5



Circuit for Direct Connection to Video Recorders



*) to TBA 120 T/UB

Socket (1): Switching voltage: at playback +12 V
at recording: free

Socket (4): Simultaneous input and output for AF

Function

When the switching voltage is applied, the emitter follower BC 238 is blocked at the output, and the buffer stage BC 308 is switched on. A preemphasis is included to balance the deemphasis at the AF output. The IF amplifier becomes inoperable by means of the diode BA 127 and the 47 kΩ resistor. The remote-controlled volume regulator in the TBA 120 is used for recording and playback.

SIEMENS

FM Sound IF with SCART Switch and Volume Control

TBA 121

Bipolar IC

Features

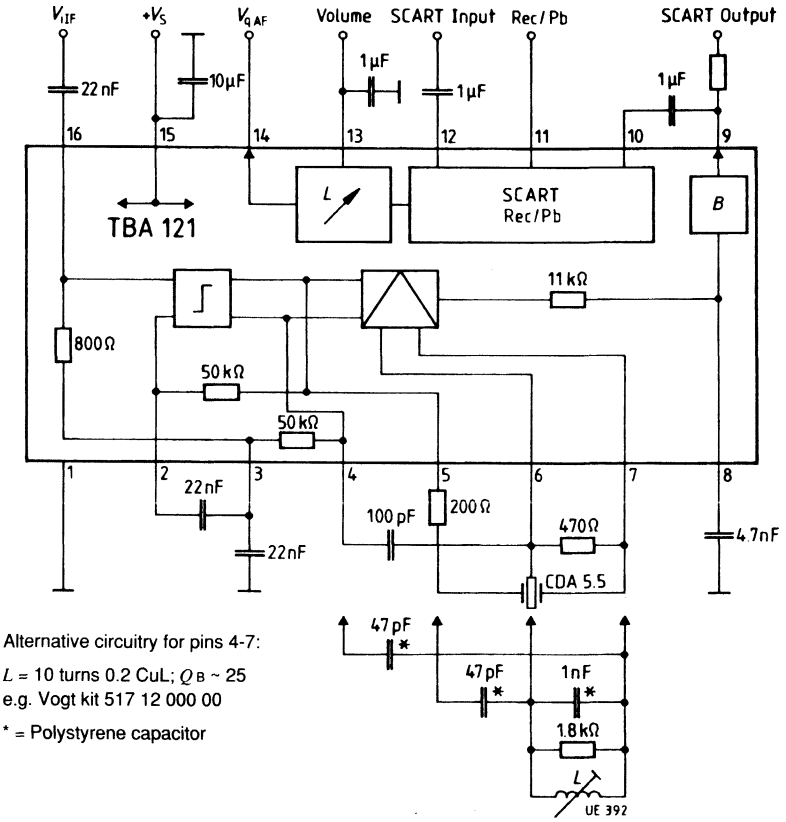
- Outstanding limiting qualities
- Few external components
- Integrated deemphasis resistor
- Low harmonic distorsion factor

Type	Ordering Code	Package
TBA 121	Q67000-A8252	P-DIP-16

In its FM section the device incorporates an eight-stage, balanced limiter amplifier followed by a coincidence demodulator. The AF section includes an analog switch for the SCART record/playback function and an analog volume control with AF output.

Application of the IC is intended in mono TV sets.

Block Diagram

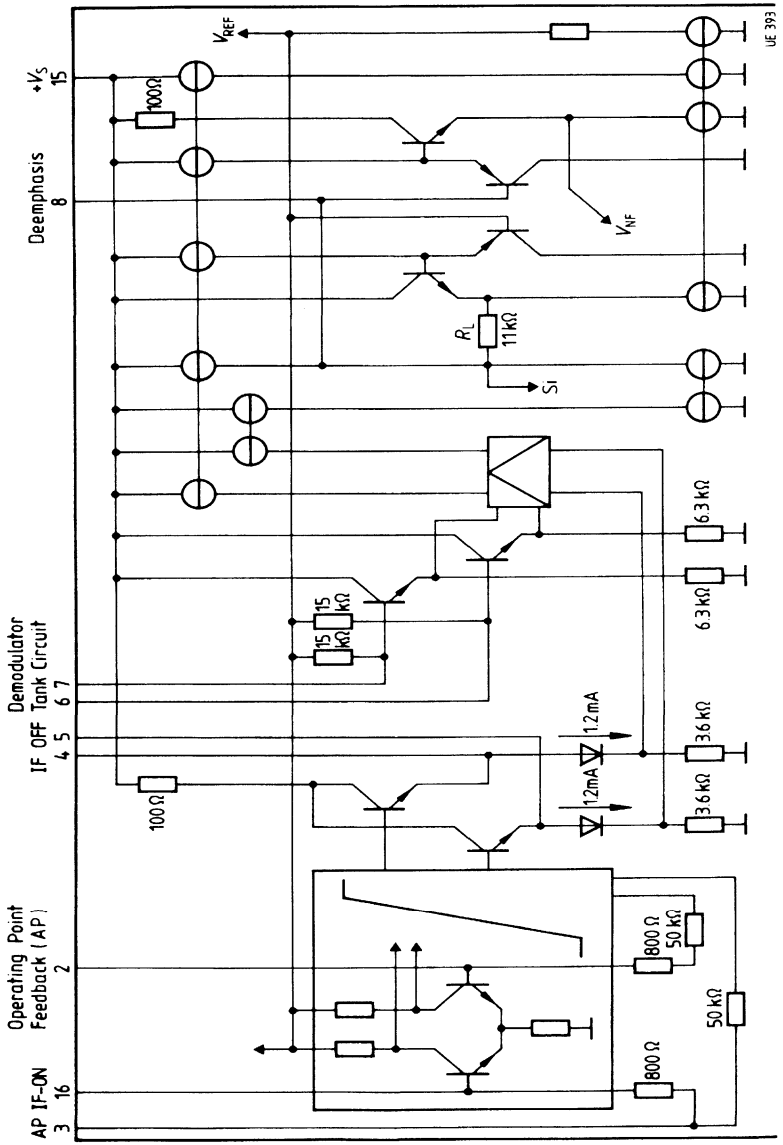


Alternative circuitry for pins 4-7:

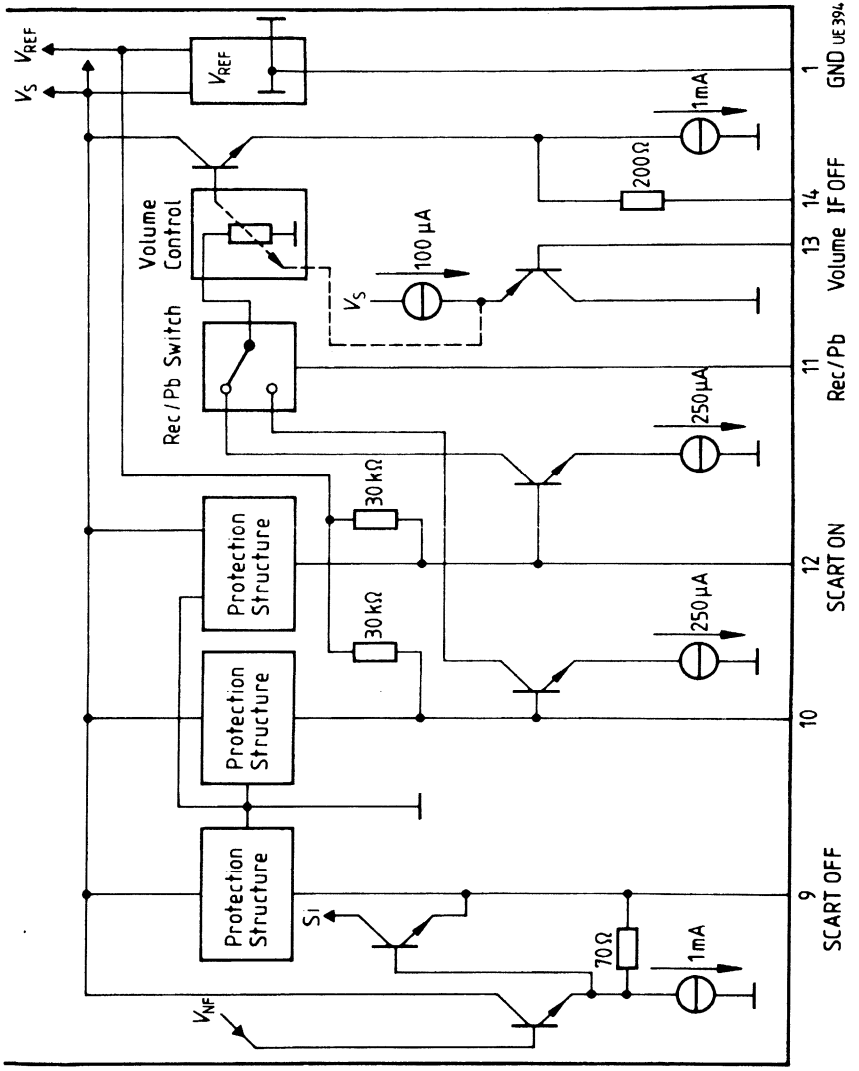
L = 10 turns 0.2 CuL; Q_B ~ 25
e.g. Vogt kit 517 12 000 00

* = Polystyrene capacitor

Expanded Block Diagram, Part 1



Expanded Block Diagram, Part 2



Pin Functions

Pin No.	Function
1	Ground
2	Limiter amplifier operating point feedback (RF decoupling of IF amplifier with appropriate capacitors is required!)
3	Limiter amplifier operating point feedback and low end (RF decoupling of IF amplifier with appropriate capacitors is required!)
4	IF amplifier output (emitter follower)
5	IF amplifier output (emitter follower)
6	Demodulator input with high impedance input and internal 15 kΩ supply resistor (if an LC circuit is used, the Q is determined by the damping resistance across pins 6 and 7)
7	Demodulator input with high impedance input and internal 15 kΩ supply resistor (if an LC circuit is used, the Q is determined by the damping resistance across pins 6 and 7)
8	Connection for deemphasis capacitor (a series resistor of 11 kΩ is integrated)
9	AF output of the SCART interface (emitter follower with short circuit limiter)
10	AF input 1 of the SCART interface (IF branch)
11	Rec/Pb switch input
12	AF input 2 of the SCART interface (SCART input)
13	Volume control
14	IF output (emitter follower)
15	Supply voltage
16	IF input (limiter amplifier input; internal resistor between pin 16 and 3 typ. 800 Ω)

Absolute Maximum Ratings

T_A = 0 to 70 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	0	16	V
IF input voltage	$V_{I\,16\,rms}$	0	600	mV rms
DC voltage	V_2	0	V_{REF}	V
DC voltage	V_3	0	V_{REF}	V
DC voltage	V_6	0	V_S	V
DC voltage	V_7	0	V_S	V
DC voltage	V_8	0	V_S-2	V
DC voltage	V_9	0	V_{REF}	V
DC voltage	V_{11}	0	V_S	V
DC voltage	V_{12}	0	V_S	V
DC voltage	V_{13}	0	V_S	V
DC voltage	V_{16}	0	V_{REF}	V
DC current	I_4	0	2	mA
DC current	I_5	0	2	mA
DC current	I_9	− 1	2	mA
DC current	I_{14}	− 1	2	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	− 55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		80	K/W

Operating Range

Supply voltage	V_S	10.5	15.75	V
Frequency range	f	0.1	12	MHz
Ambient temperature in operation	T_A	0	70	°C

Characteristics
V_S = 10.5 to 15.5 V; T_A = 0 to 70 °C, refer to test circuit

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_S	21	29	37	mA	
Input voltage for limiting response ($V_{Q9,14}$ = -3 dB)	$V_{I16\,rms}$		60	100	µV	f_{I16} = 5.5 MHz; Δf = 30 kHz; f_{mod} = 1 kHz
SCART output voltage	V_{Q9}	500	720		mV	V_{I16} = 10 mV; Δf = 30 kHz; f_{mod} = 1 kHz; f_{I16} = 5.5 MHz
AF output voltage	V_{Q14}	450	650		mV	V_{13} = 4.8 V; Δf = 30 kHz; f_{mod} = 1 kHz; f_{I16} = 5.5 MHz
DC component	V_{Q9} V_{Q14}		5.2 6		V V	V_{I16} = 10 mV; Δf = 0; $THD = THD_{min}$
Total distortion factor	THD_9 THD_{14}			1 1.1	% %	Δf = 30 kHz; V_{I16} = 10 mV; f_{mod} = 1 kHz; f_{I16} = 5.5 MHz; V_{13} = 4.8 V
AM suppression (test conditions for reference point)	$a_{AM9,14}$	50	60		dB	V_{I16} = 500 µV; m = 30%; f_{mod} = 1 kHz; f_{I16} = 5.5 MHz; Δf = 30 kHz; V_{I16} = 10 mV
Volume control range	V_{14}	80			dB	V_{13}=5-0V
Maximum SCART input voltage	V_{I12}	2			Vrms	
Gain between SCART input (pin 10) and AF output (pin 14)	G_{SC}		– 1		dB	V_{11}≥8V≤12V V_{13}=4.8V

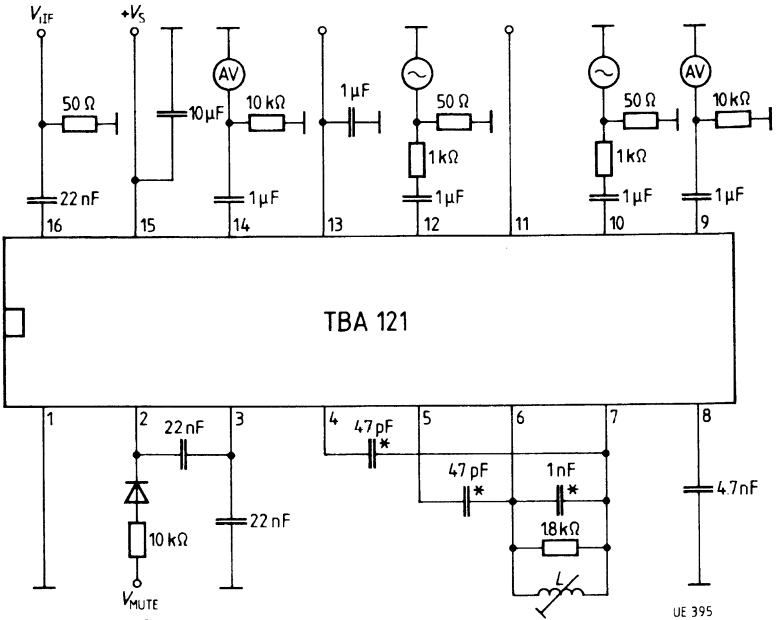
Switching Voltage, Muting

ON (AF OFF) OFF	V_3 V_3	8 0		V_S 3	V V	

Characteristics (cont'd)
V_S = 10.5 to 15.5 V; T_A = 0 to 70 °C, refer to test circuit

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Design Notes:						
Input resistance	$R_{I\,6,7}$	10			kΩ	
Output resistance	$R_{Q\,9}$			100	Ω	
Output resistance	$R_{Q\,14}$			200	Ω	
Input resistance	$R_{I\,10,12}$	20			kΩ	
Input impedance	$Z_{I\,16}$		800		Ω	
Residual IF voltage	$V_{Q\,9,14\,(IF)}$			10	mV	
Hum suppression $V_S/V_{Q\,9,14}$ (without deemphasis *C*)	a_{qh}		30		dB	ΔV_S = 500 m V_{rms} f_S=100Hz
Crosstalk attenuation (test conditions for reference point)	$a_{12\text{-}14}$	60			dB	V_{12} = 2V rms; RF mode; Δf = 30 kHz; f_{mod} = 1 kHz; $f_{I\,16}$ = 5.5 MHz $V_{I\,16}$ = 10 mV
Attenuation IF MUTE	a_{14}	80			dB	$f_{I\,16}$ = 5.5 MHz; V_{13} = 4.8 V; $V_{I\,16}$ = 300 mV; f_{mod} = 1 kHz ; Δf = 30 kHz; IF MUTE on; measured selectively at 1 kHz

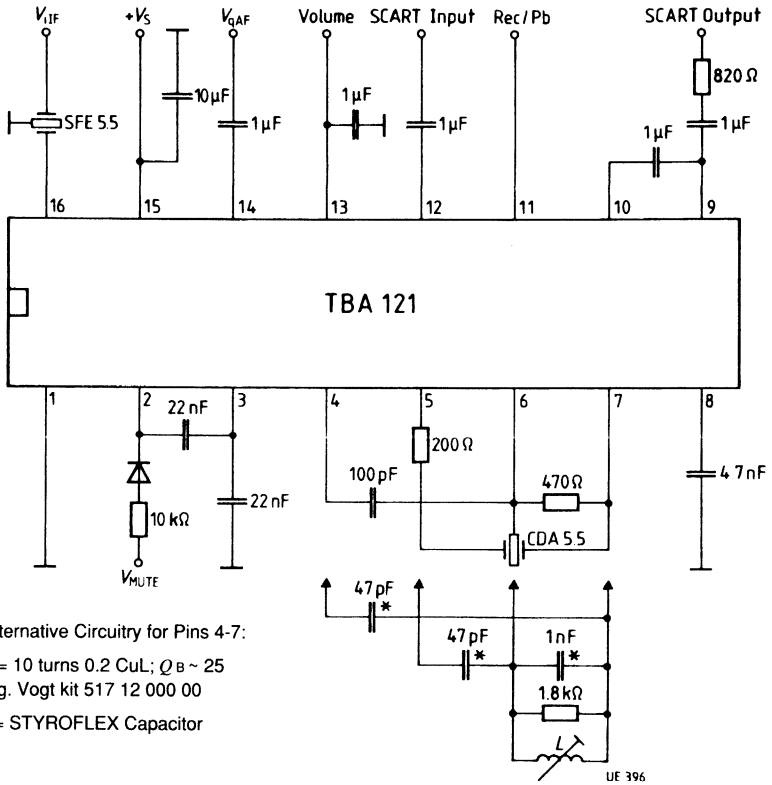
Test Circuit



L = 10 turns 0.2 CuL; Q_B ~ 25
e.g. Vogt kit 517 12 000 00

* = STYROFLEX capacitor

Application Circuit



Alternative Circuitry for Pins 4-7:

L = 10 turns 0.2 CuL; Q_B ~ 25
e.g. Vogt kit 517 12 000 00

* = STYROFLEX Capacitor

SIEMENS

FM Sound IF for Television Applications with I²C Bus and SCART

TBA 130-2

Preliminary Data

Bipolar IC

Features

- I²C bus control for the functions volume, muting, voice/music switching, as well as SCART recording/playback switching
- Integrated deemphasis resistor
- Low harmonic distortion factor

FM IF amplifier, comprising a limiter amplifier with an FM demodulator.

The AF section includes an SCART recording/playback switch, a voice/music switch, as well as a digital/analog converter to set the volume for the AF output. Control of volume, SCART recording/playback switch, and voice/music switch is achieved via an I²C bus serial interface.

The component is used in mono television sets with internal I²C bus control.

Type	Ordering Code	Package
TBA 130-2	Q67000-A8054	P-DIP-18

Circuit Description

In its FM section, the component contains an eight-stage, symmetrical limiter amplifier with subsequent coincidence demodulator. The AF section contains a mute circuit, an analog switch for the SCART recording/playback function, as well as a 6-bit D/A converter to set the volume for the AF output, and a voice/music switch. Control of the D/A converter, the switch function for record/playback and voice/music is achieved via an I²C bus serial interface (ref. diagrams).

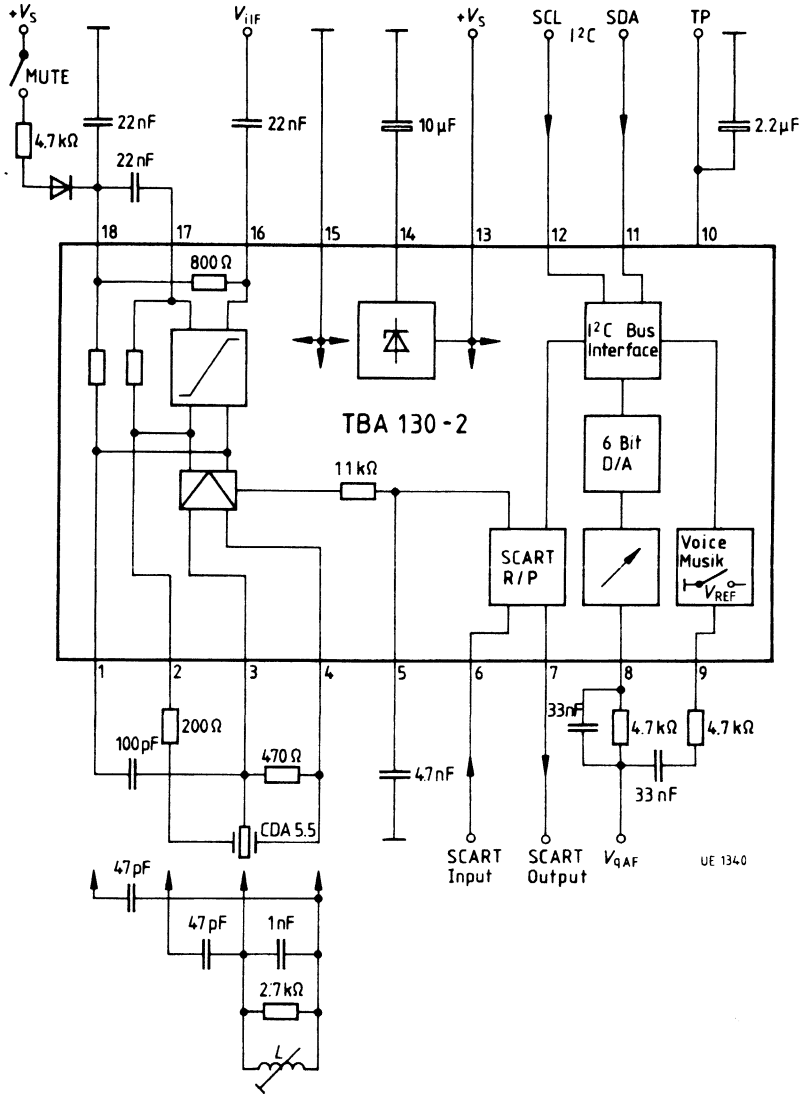
Data from the processor passes through an I²C bus control and is stored in registers according to its function (latch 1-3). If the bus is free, both lines will be in the mark state (SDA, SCL high). Each message begins with the start conditions: SDA goes L, while SCL remains H.

Any additional information transfer takes place while SCL = L, data is accepted by the control with the positive clock edge. If SDA goes H while the clock is H, the circuit recognizes a stop condition and thus, an end of the message.

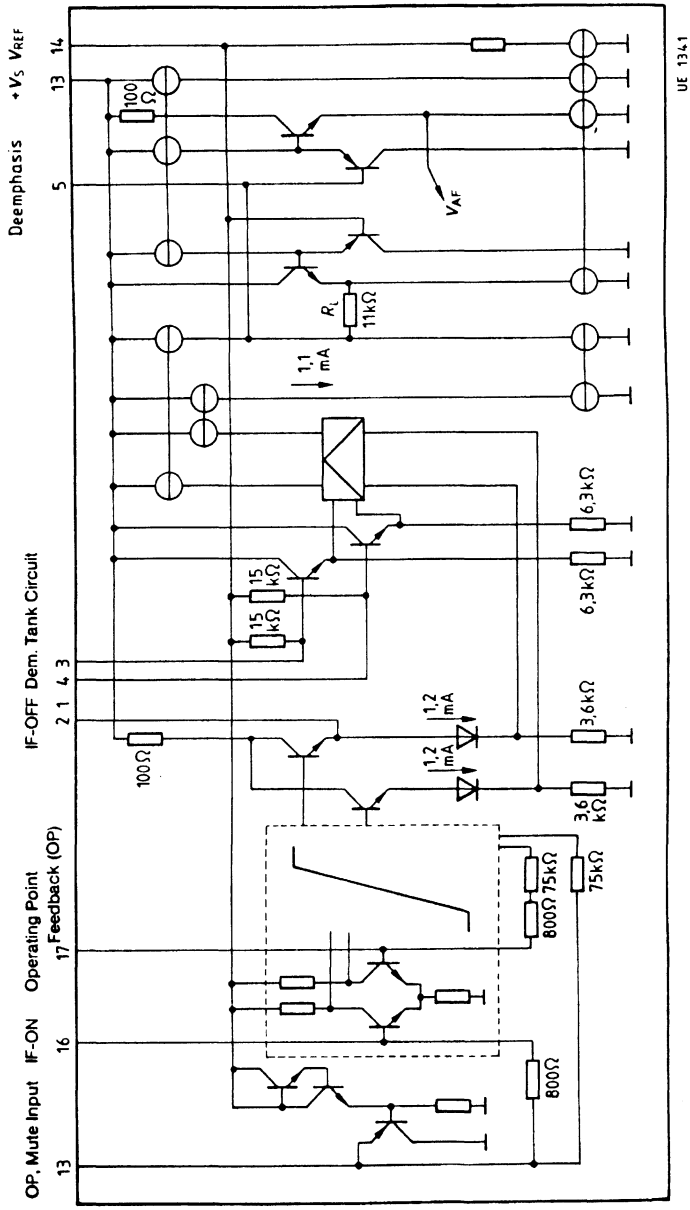
The logic operates according to the table shown on page 375. All messages are transmitted byte-by-byte, followed by a ninth clock pulse, while the control returns the SDA line to L (acknowledge condition). The first byte consists of 7 address bits, with which the processor selects the TBA 130-2 from among several peripheral components (chip select). The eighth bit determines the direction of the subsequent data traffic (in this case read mode only).

The first and the second bit of the data bytes determine which latch will be called (sub-address). The volume information is contained in 6 bits (64 steps). For reasons of compatibility with the TDA 6200, a second bit with the same sub-address but with random contents must be transmitted for setting the volume.

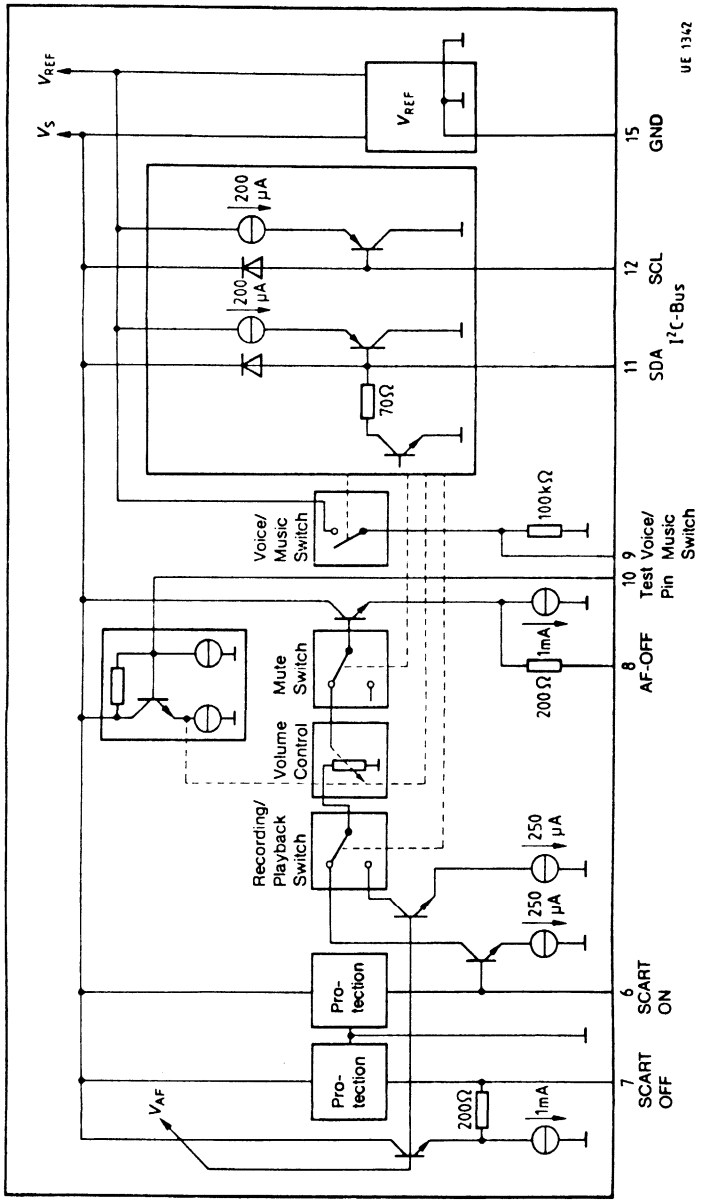
Block Diagram



Expanded Block Diagram Part 1



Expanded Block Diagram Part 2



Pin Functions

Pin No.	Function
1, 2	IF amplifier output (emitter follower)
3, 4	Demodulator tank circuit connection (high impedance input – slope of S curve determined by external resistor between pins 3 and 4)
5	Connection for deemphasis capacitor (a series resistor of 11 kΩ is integrated)
6	AF input of SCART interface
7	AF output of SCART interface (emitter follower)
8	AF output (emitter follower)
9	Voice/music switch (open collector; max. 1 mA!)
10	Test pin (access to volume control)
11	Data input/output of the I^2C bus control
12	Clock frequency input of the I^2C (inter IC) bus control
13	Supply voltage
14	Internal reference voltage (6 V typ.)
15	GND
16	IF input (limiter amplifier input; internal resistor between pins 16 and 18 is 800 Ω typ.)
17	Limiter amplifier operating point feedback (RF decoupling of IF amplifier with appropriate capacitors if required)
18	Limiter amplifier operating point and low end; MUTE input (RF decoupling of IF amplifier with appropriate capacitors if required)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	0	16	V
Reference current	I_{REF}	0	2	mA
IF input voltage	$V_{I\,16\,rms}$	0	600	mV
DC voltage	$V_{3,4,6}$	0	V_S	V
DC voltage	$V_{11,12}$	0	V_S	V
DC voltage	$V_{16,17,18}$	0	V_{REF}	V
DC current	$I_{1,2}$	0	2	mA
DC current	$I_{5,7,8}$	– 1	2	mA
DC current	I_9	0	2	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		80	K/W

Operating Range

Supply voltage	V_S	10.5	15.75	V
Frequency	f	0.1	12	MHz
Ambient temperature	T_A	0	70	°C

Characteristics

V_S = 12 V; T_A = 25 °C; $f_{I\,14}$ = 5.5 MHz; Δf = ± 30 kHz; f_{mod} = 1 kHz

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption	I_S	24	36	48	mA
Reference voltage	V_{REF}	5.4	6	6.6	V
Input voltage for limiter threshold $V_{Q\,7,8}$ = − 3 dB	$V_{I\,16\,rms}$		50	100	µV
SCART output voltage $V_{I\,16\,rms}$ = 10 mV	$V_{Q\,7}$	450	650	850	mV
AF output voltage L byte = BF	$V_{Q\,8}$	450	650	850	mV
DC voltage portion $V_{I\,16\,rms}$ = 10 mV; Δf = 0; $THD = THD_{min}$	$V_{Q\,7}$; $V_{Q\,8}$		6		V
Total harmonic distortion $V_{I\,16\,rms}$ = 10 mV L byte = BF	THD_7; THD_8			1	%
AM suppression[1] $V_{I\,16\,rms}$ = 500 µV; m = 30%	$\alpha_{AM\,7,8}$	50	60		dB
Volume control L byte = 80-BF	ΔV_8	80			dB
Max. input voltage SCART $THD_8 \leq 1\%$	$V_{I\,6\,rms}$	2			V
Gain between SCART input (pin 6) and AF output (pin 8) L byte = BF	G_{SC}		0		dB

Switching Voltage Muting

ON (AF OFF)	V_{18} =	8		V_S	V
OFF	V_{18} =	0		3	V

Voice / Music Switch ($I_{Q\,9}$ = 1 mA)

V/M = 0 = high-ohmic R_{OFF} Pin 14 V_{REF}		75	100		kΩ
V/M = 1 = low-ohmic R_{ON} DC voltage at pin 9 ($I_{Q\,9}$ = 0)	V_9 =	5.4	6	800 6.6	Ω V

[1] Test conditions for the reference point
$f_{I\,14}$ = 5.5 MHz; $V_{I\,14\,rms}$ = 10 mV; Δf = ± 30 kHz; f_{mod} = 1 kHz

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C; f_{i14} = 5.5 MHz

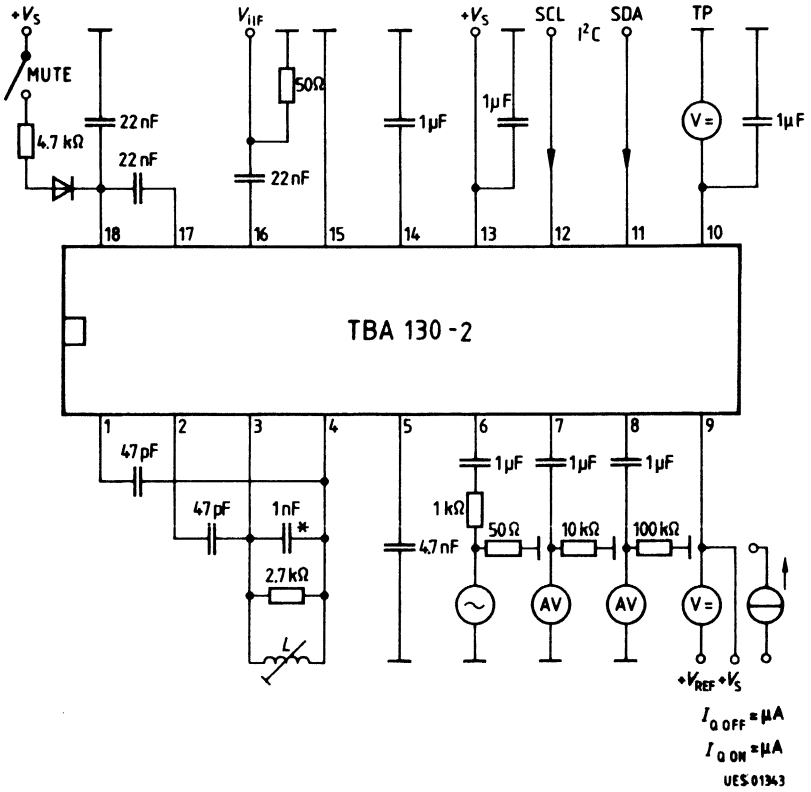
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
I²C Bus (SCL, SDA)					
Edges SCL, SDA					
Rise time	t_r			1	µs
Fall time	t_f			0.3	µs
Shift Clock SCL					
Frequency	f_{SCL}	0		100	kHz
H-pulse width	t_{HIGH}	4			µs
L- pulse width	t_{LOW}	4			µs
Start					
Set-up time	t_{SUSTA}	4			µs
Hold time	t_{HDSTA}	4			µs
Stop					
Set-up time	t_{SUSTO}	4			µs
Bus free	t_{BUF}	4			µs
Data Change					
Set-up time	t_{SUDAT}	1			µs
Hold time	t_{HDDAT}	1			µs
Input SCL, SDA					
Input voltage	V_{IH} V_{IH}	2.4 0.3		5.5 1	V V
Input current	I_{IH} I_{IH}			50 100	µA µA

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C; $f_{I\,14}$ = 5.5 MHz

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Output SDA (open collector)					
Output voltage R_L = 2.5 kΩ I_{QL} = 2 mA	V_{QH} V_{QL}			5.5 0.4	V V
Design-Related Characteristics					
Input resistance	$R_{I\,3,4}$	20			kΩ
Output resistance	$R_{Q\,7,8}$			200	Ω
Input resistance	$R_{I\,6}$	20			kΩ
Input impedance	$Z_{I\,16}$		800		Ω
IF residual voltage ΔV_S rms = 500 mV; f_S = 100 Hz	$V_{Q\,7,8}$		10		mV
Hum suppression $V_S/V_{Q\,7,8}$ (without deemphasis C) ΔV_S rms = 500 mV; f_S = 100 Hz	α_{hum}		30		dB
Crosstalk rejection[1] V_6 rms = 2 V; SC = 0	$\alpha_{6\text{-}8}$	60			dB

[1] Test conditions for the reference point
$f_{I\,14}$ = 5.5 MHz; $V_{I\,14\,rms}$ = 10 mV; Δf = ± 30 kHz; f_{mod} = 1 kHz

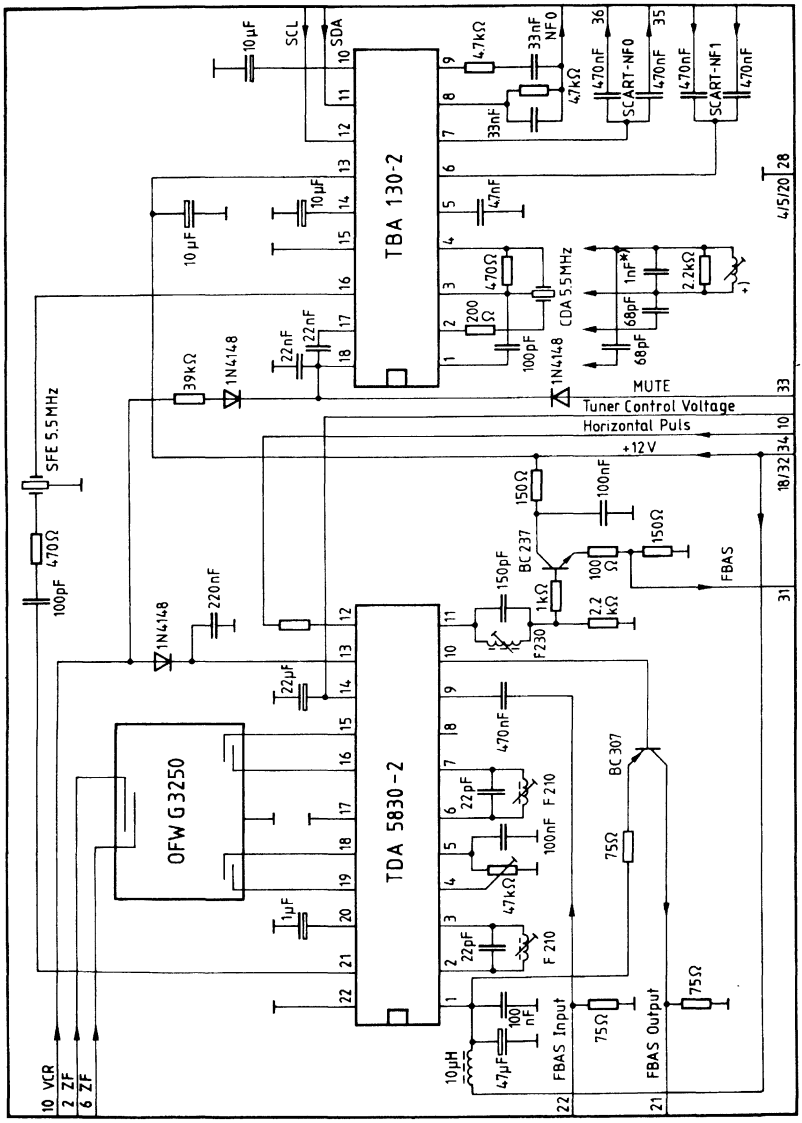
Test Circuit



L: 10 turns, 0.2 CuL; Q_B approx. 25
e.g. Vogt Coil Assembly 517 12 000 00

* STYROFLEX Capacitor

Application Circuit



L: 10 turns, 0.2 CuL; Q_B approx. 25
e.g. Vogt Coil Assembly 517 12 000 00

* STYROFLEX Capacitor

Software Definition

The following data format is used:

1) **Chip Address**

MSB							LSB	
1	0	0	0	0	0	0	0	acknowledge

MSB is transmitted first

2) **Data Bytes with Sub-Addresses**

a) volume

MSB							LSB
1	0	V_{05}	V_{04}	V_{03}	V_{02}	V_{01}	V_{00}
1	0	X	X	X	X	X	X

The second byte has to be included in the transfer

V_{X5} = MSB
V_{X0} = LSB

1	0	0	0	0	0	0	0	min. volume
1	0	1	1	1	1	1	1	max. volume

b) SCART control byte

MSB							LSB
1	SC	X	X	X	X	X	0

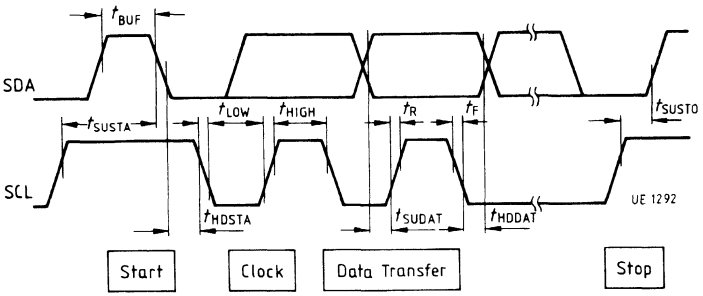
SC = 1 SCART playback; SCART input is connected with AF output
SC = 0 standard operating mode

c) AF control byte

MSB							LSB
0	0	M	X	V/M	X	X	X

V/M = 0 pin 9 high-impedance
V/M = 1 pin 9 low-impedance
M = 1 muting for AF output
M = 0 AF ON

I²C Bus Timing Diagram



t_{SUSTA}	Set-up time (start)
t_{HDSTA}	Hold time (start)
t_{HIGH}	H- pulse width (clock)
t_{LOW}	L- pulse width (clock)
t_{SUDAT}	Set-up time (data transfer)
t_{HDDAT}	Hold time (data transfer)
t_{SUSTO}	Set-up time (stop)
t_{BUF}	Bus free
t_F	Fall time
t_R	Rise time

Above times are referenced to V_{IH} and V_{IL} values.

SIEMENS

Dual Sound FM IF Amplifier

TBA 229-2

Bipolar IC

The component contains two separate limiter amplifiers with FM demodulators and separate AF outputs.

Features

- High AM suppression over a very wide input voltage range
- High sensitivity
- Very high symmetry

Type	Ordering Code	Package
TBA 229-2	Q67000-A8037	P-DIP-16

Circuit Description

The component contains two separate FM sound IF sections for television stereo applications or for multistandard receivers. Each FM section consists of an eight-stage symmetrical limiter amplifier followed by a coincidence demodulator and an AF pre-amplifier with a low-ohmic output. The component features considerably improved AM suppression characteristics with small input signals, as well as a very low frequency deviation between THD_{min} and AM_{min}.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	0	16	V
Reference current	I_{REF}	0	2	mA
IF input voltage	$V_{I\,IF\,rms}$	0	600	mV
DC voltages	$V_{9, 10, 11}$	0	V_{REF}	V
	$V_{14, 15, 16}$	0	V_{REF}	V
DC currents	$I_{1, 2, 4, 5, 7, 8}$	0	2	mA
Junction temperature	T_j		150	°C
Storage temperature range	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		80	K/W

Operating Range

Supply voltage	V_S	10.5	15.75	V
Ambient temperature	T_A	0	70	°C
Fequency	f_I	0.1	12	MHz

Characteristics

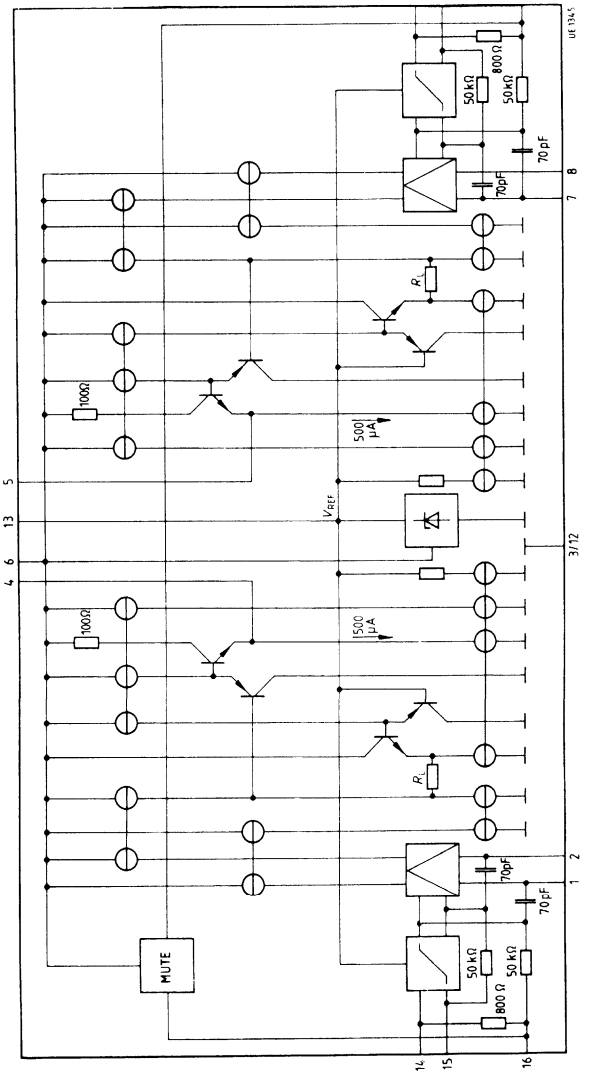
V_S = 12 V; T_A = 25 °C; $V_{I\,IF\,14\,rms}$ = 10 mV; $f_{IF\,11,14}$ = 5.5 MHz; f_{mod} = 1 kHz; Δf = ± 30 kHz (if not stated otherwise)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_S	25	35	42	mA	
Input voltage for limiter threshold	$V_{I\,11\,rms}$		50	100	µV	
	$V_{I\,14\,rms}$		50	100	µV	$V_{Q\,4,5}$ = – 3 dB
Output voltage	$V_{Q\,4\,rms}$	510	600	700	mV	
	$V_{Q\,5\,rms}$	510	600	700	mV	
DC voltage portion	$V_{Q\,4}$ =	4.8	6	6.2	V	
	$V_{Q\,5}$ =	4.8	6	6.2	V	Δf = 0; $THD = THD_{min}$
Total harmonic distortion	THD_4, THD_5		0.4	0.8	%	$THD = THD_{min}$
AM suppression	$\alpha_{AM\,4}$	55	60		dB	
$V_{I\,rms}$ =1 mV; m = 30%	$\alpha_{AM\,5}$	55	60		dB	$V_{I\,rms}$=1 mV; m = 30%
Cross-talk rejection	$C_{IF\,1\text{-}2} = V_{Q\,4}/V_{Q\,5}$	60			dB	$f_{IF\,11}$ = 5.5 MHz; Δf_{11} = 0 kHz; $V_{I\,11\,rms}$ = 4 mV; $V_{I\,14\,rms}$ =10 mV
	$C_{IF\,1\text{-}2} = V_{Q\,4}/V_{Q\,5}$	60			dB	$f_{IF\,11}$ = 5.74 MHz; Δf_{14} = 0 kHz; $V_{I\,11\,rms}$ = 4 mV; $V_{I\,14\,rms}$ =10 mV
Reference voltage	V_{13} =	5.4	6	6.6	V	
Switching voltage muting						
ON (AF off)	V_{16}	8		V_S	V	
OFF	V_{16}	0		3	V	

Design-Related Values

Input resistance	$R_{I\,1,2}$	20			kΩ	
	$R_{I\,7,8}$	20			kΩ	
Output resistance	$R_{Q\,4,5}$			100	Ω	
Input impedance	$Z_{I11,14}$		800		Ω	
IF residual voltage	$V_{Q\,4,5\,(IF)}$		15		mV	
Hum suppression	$\alpha_{Q\,hum}$		32		dB	f_S = 100 Hz; ΔV_S rms = 500 mV; $V_S/V_{Q\,4}$; $V_S/V_{Q\,5}$
Frequency deviation AM$_{min}$ – THD_{min}	Δf_{IF}		±10		kHz	

Block Diagram

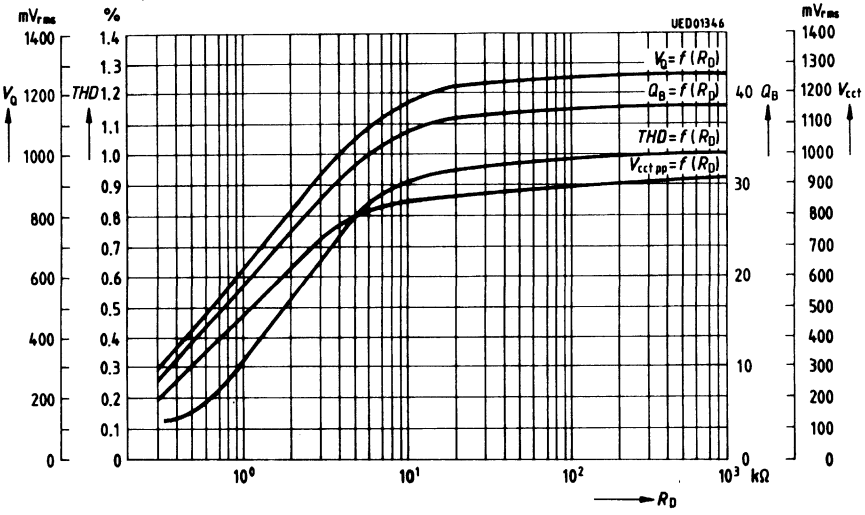


Pin Functions

Pin No.	Function
1, 2	Demodulator tank circuit connection IF 1 (high impedance input – slope of S-curve can be determined by external resistor between pins 1 and 2)
3	GND
4	AF output IF 1 (emitter follower)
5	AF output IF 2 (emitter follower)
6	Supply voltage
7, 8	Demodulator tank circuit connection IF 2 (high impedance input – slope of S-curve can be determined by external resistor between pins 1 and 2)
9	Operating point feedback of limiter amplifier and low end IF 2 (RF decoupling of IF amplifiers with appropriate capacitors is required!
10	Operating point feedback of limiter amplifier IF 2 (RF decoupling of IF amplifiers with appropriate capacitors is required!)
11	IF 2 input (input of limiter amplifier IF 2; internal resistor between pins 9 and 11 is typ. 800 Ω)
12	GND
13	Internal reference voltage (typ. 6 V)
14	IF 1 input (input of limiter amplifier IF 2; internal resistor between pins 14 and 15 is typ. 800 Ω)
15	Operating feedback of limiter amplifier IF 1 (RF decoupling of IF amplifiers with appropriate capacitors is required!)
16	Operating point feedback of limiter amplifier and low end IF 1 (RF decoupling of IF amplifiers with appropriate capacitors is required!)

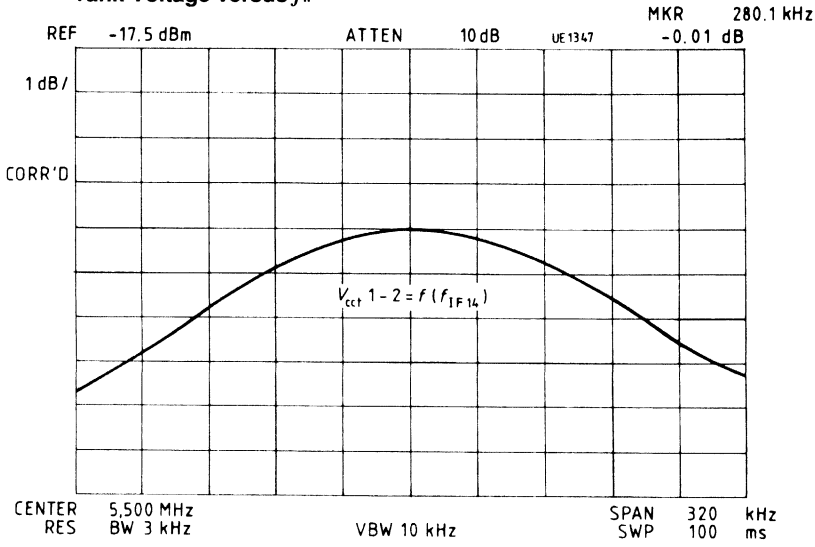
Diagrams

AF Output Voltage, Total Harmonic Distortion, Circuit Voltage versus Circuit Q_B



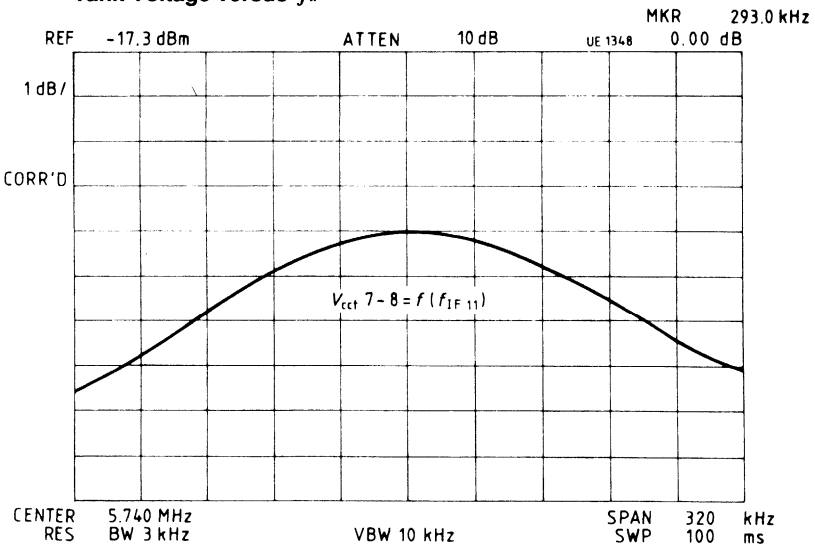
V_Q:	$V_{Q\,4}$ rms; $V_{Q\,5}$ rms
THD:	THD_4; THD_5
Measured at:	$f_{I\,IF}$ = 5.5 MHz; Δf = 30 kHz; f_{mod} = 1 kHz; $V_{I\,IF}$ = 10 mV
V_{cct}:	$V_{1,2} = V_{7,8}$
Measured at:	$f_{I\,IF}$ = 5.5 MHz; Δf = 0 kHz; $V_{I\,IF}$ = 10 mV
Q_B:	Q between connections 1, 2 and 7, 8
Measured at:	$f_{I\,IF}$ = 5.5 MHz/$\Delta f_{I\,IF}$ for 3 dB bandwidth, Δf = 0 kHz; $V_{I\,IF}$ = 10 mV
Circuit:	L = 10 turns 0.25 CuL; Vogt Coil Assembly 517 12 000 00 without cap C = 1 nF STYROFLEX Capacitor

Tank Voltage versus f_{IF}



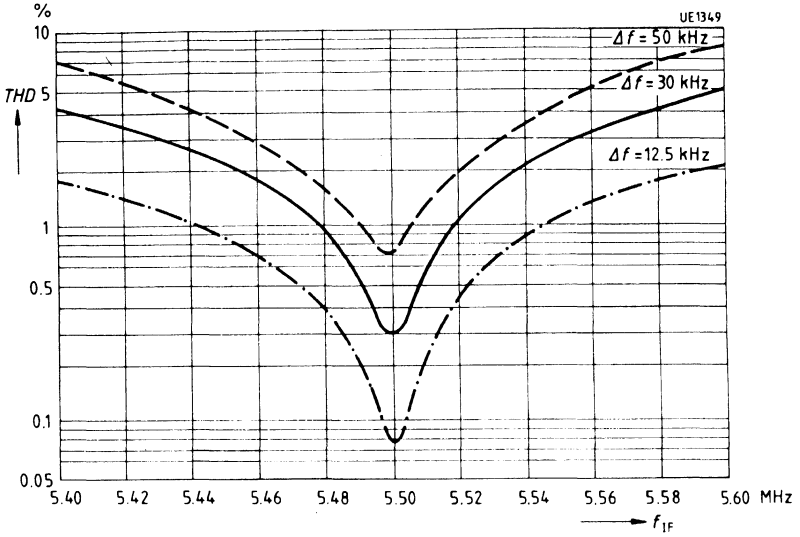
Q_B 1 - 2 = $f_{IF\,14}$ / Δf_{14} (- 3 dB) = 5.5 / 0.28 = 19.64
V_{ct} 1 - 2 max = 450 mV_{pp}

Tank Voltage versus f_{IF}

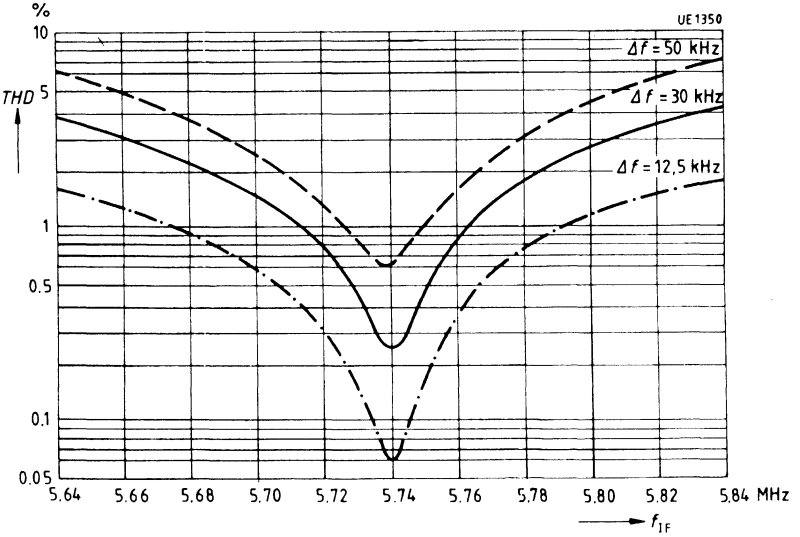


Q_B 7 - 8 = $f_{IF\,11}$ / Δf_{11} (- 3 dB) = 5.74 / 0.293 = 19.59
V_{ct} 7 - 8 max = 450 mV_{pp}

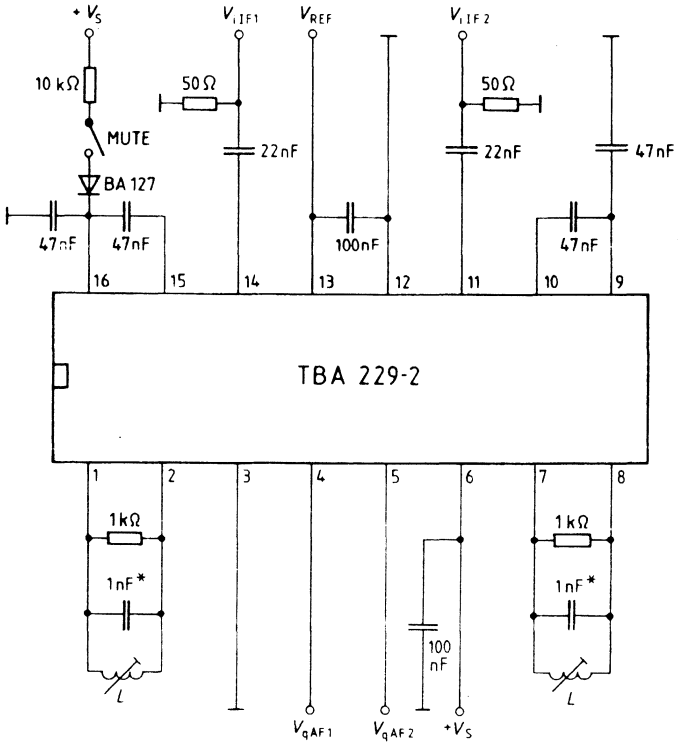
Total Harmonic Distortion versus Detuning (FM Operation)
$THD_4 = f(f_{IIF})$; V_I= 10 mV; V_S = 12 V; f_{mod} = 1 kHz,
Δf = 50 kHz, 30 kHz, 12.5 kHz



Total Harmonic Distortion versus Detuning (FM Operation)
compensated for minimum total harmonic distortion at f_{IF} = 5.5 MHz;
$THD = f(f_{IIF})$; V_I = 10 mV; V_S = 12 V; f_{mod} = 1 kHz,
Δf = 50 kHz; 30 kHz; 12.5 kHz



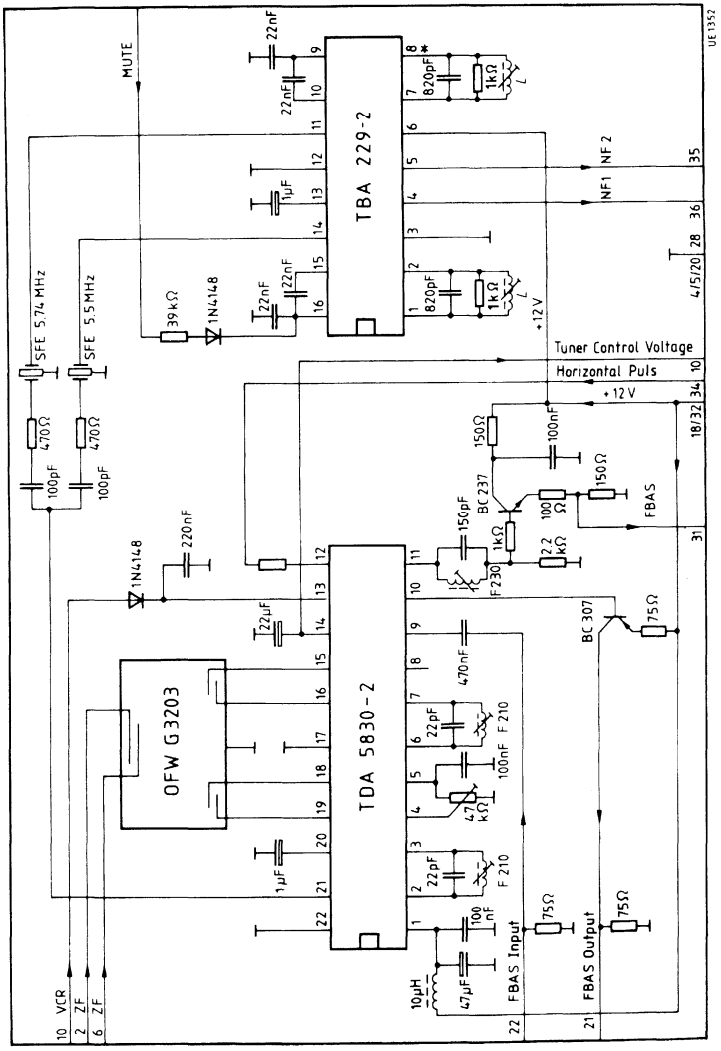
Test Circuit



L = 10 Turns 0.2 CuL; Q_B see page "Diagrams" UE 1351
e.g. Vogt Coil Assembly 517 12 000 00

* STYROFLEX Capacitor

Application Circuit



L = 10 turns 0.2 CuL; Q_B approx. 25
e.g. Vogt Coil Assembly 517 12 000 00

SIEMENS

PLL Stereo Decoder

TCA 4511-2

Preliminary Data

Bipolar IC

Features

- Good channel separation
- No need for coils
- Automatically adjustable bandwidth
- Good suppression of ARI subcarrier and pilot tone harmonics

Type	Ordering Code	Package
TCA 4511-2	Q67000-A8011	P-DIP-18

The TCA 4511 decodes the transmitter side stereo information in both L and R channels. Stereo transmission is shown by means of an indicator lamp. A continual blending of mono and stereo signals is possible. The switching frequencies are controlled by a phase-locked loop. The stereo decoder operates in time multiplex mode (switching) or in frequency multiplex (matrix) mode.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	18	V
Lamp voltage	V_{LP}	18	V
Current for stereo indicator lamp $V_{18} \times I_{LP} \leq 300$ mW	I_{LP}	50	mA
Minimum voltage at all pins	V	0	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 40 to 125	°C
Thermal resistance system-air junction-case	 $R_{th\,SA}$ $R_{th\,JC}$	 78 45	 K/W K/W

Operating Range

Supply voltage	V_S	8 to 18	V
Ambient temperature	T_A	– 25 to 85	°C

Characteristicsz
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Total current (FM operation) S1 closed	I_S		14	20	mA
Total current (AM operation) S1 open	I_S		10	15	mA
Lamp current adjustment range $V_{18} \times I_{LP} \leq 300$ mW	I_{LP}	10		25	mA
Lamp current short circuit $V_{18} \times I_{LP} \leq 300$ mW	I_{LP}			50	mA
Input Amplifier					
Op amp input signal	V_{16}			1.6	Vpp
Op amp output signal[1])	V_{14}		V_{16}		Vpp
Input resistance	R_I	90	125		kΩ
Degeneration resistance	R_F		10		kΩ
Reference voltage	V_{13}		1.75		V
Stereo Matrix					
Output voltage (stereo)[1, 6]) for modulated output	$V_{Q\,AF}$	0.9	1.2	1.6	Vpp
Output voltage (mono)[2, 6]) L or R modulated	$V_{Q\,AF}$	0.45	0.6	0.8	Vpp
Output resistance	R_Q		1.5	2	kΩ
Cross-talk attenuation[1]) f_{AF} = 1 kHz	a_{CR}	34	40		dB
Reduction 19 kHz / test circuit 1	a_{19}	30	32		dB
Reduction 38 kHz / test circuit 1	a_{38}	30	40		dB
Reduction 57 kHz / test circuit 1	a_{57}	30	45		dB
Reduction 76 kHz / test circuit 1	a_{76}	30	40		dB
Hum suppression[3])	a_{hum}	40	45		dB
Noise voltage[4])	V_{Qn}		30	80	µV
Total harmonic distortion[1, 6]) f_{AF} = 1 kHz	THD			0.5	%
Channel balance[2])	B			0.5	dB
Switching noise mono/stereo S1 closed/open	ΔV_9, ΔV_{10}			60	mV

1) For notes refer to page 390

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Oscillator					
Output resistance for f_{OSC} measurement	R_{Q8}		200		kΩ
Oscillator basic frequency	f_{OSC}		19		kHz
Capture and hold range[1])	$f_{C/H}$	± 0.4	± 1	± 2.0	kHz
Balancing resistance f_{OSC} = 19 kHz	R_{OSC}	13		18	kΩ
Oscillator in operation S1 closed	V_{18}	1.0			V
Switch off of the oscillator[8]) S1 open	V_{18}			0.4	V
Function of the oscillator I_{18} = 10 mA	V_{18}	0.9			V

1) For notes refer to page 390

Characteristics (cont 'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Phase Comparisons					
Input voltage[1])	V_5	0.5	0.7	0.9	Vpp
Input resistance	R_5		3.3		kΩ
Input voltage	V_5			1.6	Vpp
Stereo Switch					
Threshold stereo ON[5]) f = 19 kHz	V_{IPT}		30	55	mVpp
Threshold stereo OFF[5]) f = 19 kHz	V_{IPT}	12	15		mVpp
Hysteresis	H_y	3	6	9	dB
Mono/Stereo Blending					
Mono $V_H = V_8$ = 0.5 V[7])	a_{CR}	3	6	9	dB
Stereo $V_H = V_8$ = 0.9 V[7])	a_{CR}	34			dB

[1]) V_I pp = 1.2 V MPX; V_H 1 V; S1 closed; f_{AF} = 1 kHz
[2]) V_I pp = 1.2 V MPX; S1 open; f_{AF} = 1 kHz
[3]) V_S = 12 V + V_n; V_n rms = 200 mV; 200 Hz
[4]) CCIR DIN 45 405; unweighted; S1 open
[5]) S1 closed
[6]) After TP with f_{co} = 6.5 kHz; reduction 36 dB/octave
[7]) V_{16} pp = 0.75 V MPX; S1 closed; f_{AF} = 1 kHz
[8]) The oscillator is switched off, if pin 18 is connected with a voltage ≤ 0.4 V or S1 is open.

Circuit Description

The MPX input signal is corrected in amplitude and phase by an operational amplifier. For this purpose an RC circuit is connected at pin 15.

Subsequently, the (L + R) and (L - R) signals are processed in separate stages. The (L – R) signal is demodulated and can be reduced by the factor a through mono/stereo blending. In the final matrix circuit the aggregate signal (L + R) is added to the demodulated signal a (L – R) according to the following formulae:

$$(L + R) + a\,(L - R) = L\,(1 + a) + R\,(1 - a)$$
$$(L + R) - a\,(L - R) = L\,(1 - a) + R\,(1 + a)$$

$$\begin{array}{ccccc} 0 & \leq & a & \leq & 1 \\ \text{Mono} & & \text{Blending} & & \text{Stereo} \end{array}$$

The generated output signals are then forwarded to two external RC low-passes for deemphasis.

The required frequency to demodulate the L – R signal is obtained by a phase-locked loop (PLL) from the divider. By means of a pilot tone applied to pin 5, the oscillator is synchronized by phase comparison 1. An additional phase comparison 2 provides mono or stereo information. Based on this information, the indicator lamp is activated and lights up when a sufficiently strong signal is present at the input. Moreover, the (L – R) reduction is eliminated.

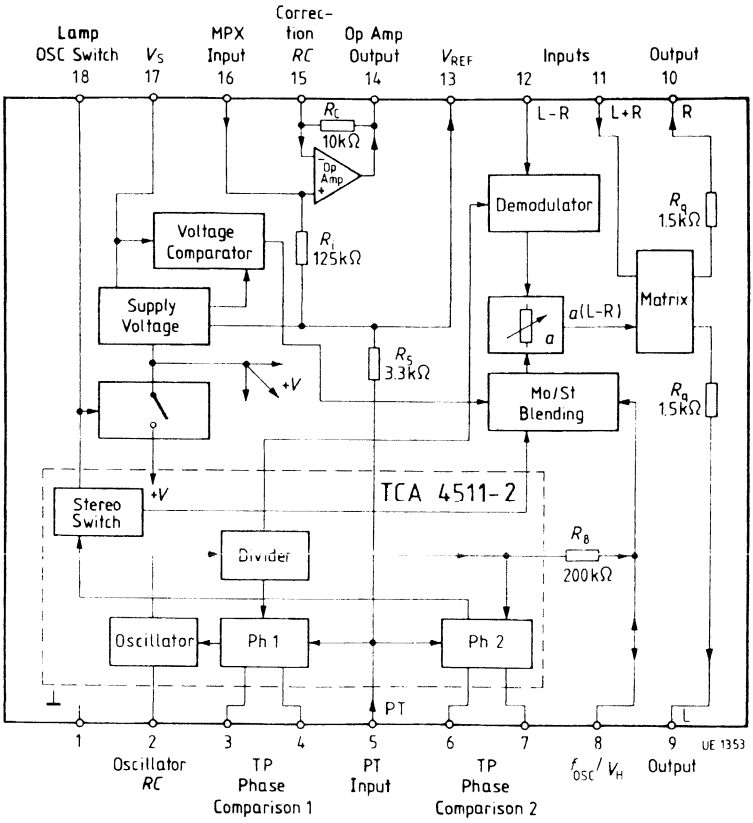
If switch S1 is open, the IC switches the oscillator off, whereby the stereo switch and the mono/stereo blending suppress the L – R signal. The supply current is thus reduced. Also, since the oscillator does not resonate when switch S1 is open, AM receiver signals can be forwarded without interference via the IC.

If pin 8 is not connected, the oscillator frequency can be measured. For normal operating functions, the blending voltage V_H is applied to pin 8 or pin 8 must be blocked by a capacitor. Otherwise, cross-talk is affected by the oscillator frequency.

Pin Functions

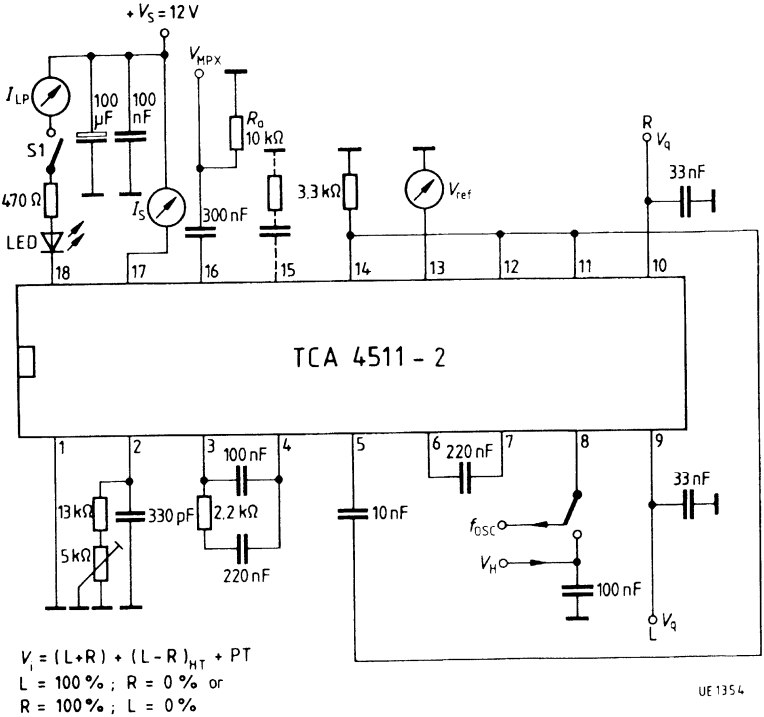
Pin No.	Function
1	GND
2	Oscillator *RC*
3	TP phase comparison 1
4	TP phase comparison 1
5	Pilot tone (PT) input
6	TP phase comparison 2
7	TP phase comparison 2
8	f_{OSC} output/St-Mo blending V_H
9	Output L
10	Output R
11	(L + R) input
12	(L – R) input
13	Reference voltage
14	Output op amp
15	– input op amp
16	+ input op amp
17	Supply voltage
18	Lamp connection/oscillator switch

Block Diagram



Test Circuit

Switching Operation

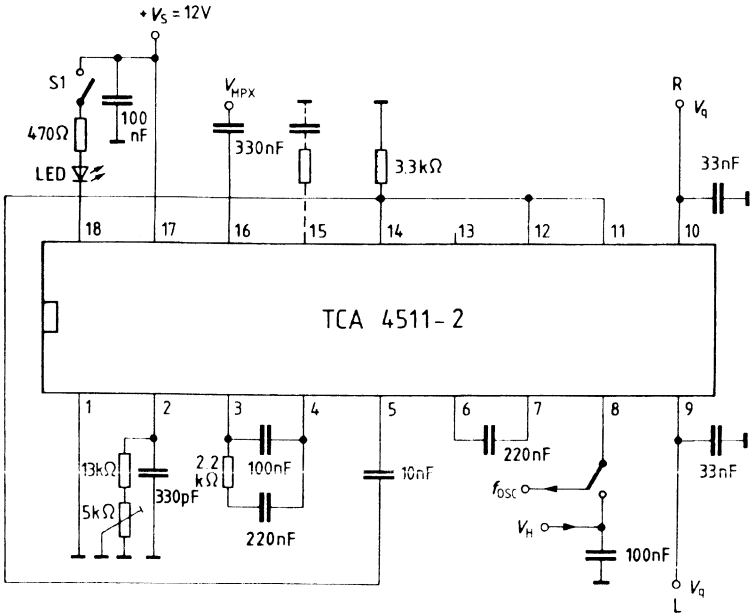


$V_i = (L+R) + (L-R)_{HT} + PT$
L = 100 % ; R = 0 % or
R = 100 % ; L = 0 %

S1 open = AM
S1 closed = FM

Application Circuit

Switching Operation



S1 open = AM
S1 closed = FM

UE 1355

SIEMENS

AM Amplifier for French Sound IF Standard

TDA 2148

Bipolar IC

Controlled AM IF amplifier with quasi-synchronous demodulator and integral mean value control for French sound IF applications.

Features

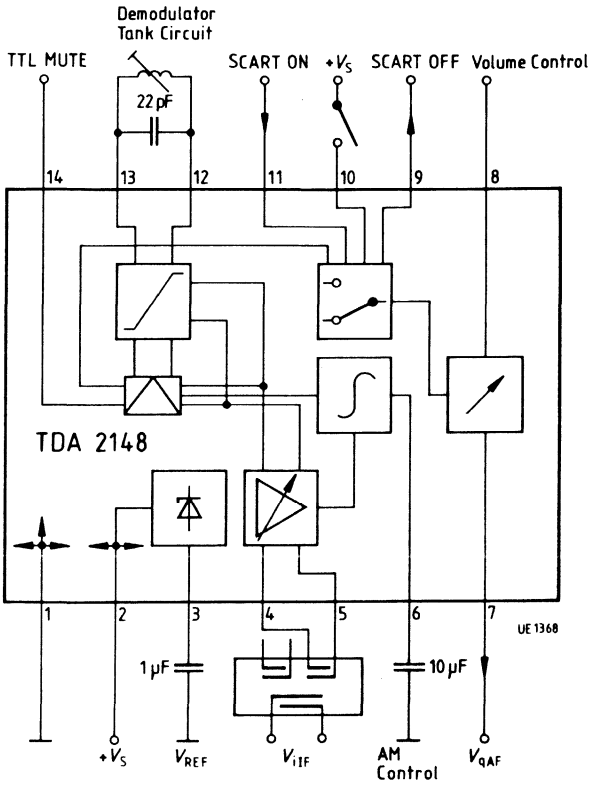
- High input sensitivity
- Few external components
- Low distortion
- Full SCART interface
- Partially compatible with TDA 2460

Type	Ordering Code	Package
TDA 2148	Q67000-A2476	P-DIP-14

Circuit Description

The component contains a four-stage, capacitatively coupled control amplifier and a quasi-synchronous demodulator according to the French sound IF standard. The control voltage is generated by means of an integral mean value control. The resulting AF signal is pre-amplified and routed to the SCART output as well as to the record / playback switch. This is followed by a volume control with a low-impedance AF output.

Block Diagram



Pin Functions

Pin No.	Function
1	GND
2	$+V_S$
3	Reference voltage
4	IF input
5	IF input
6	AGC time constant AM amplifier
7	AF output
8	Volume control for voltage AF output
9	SCART AF output
10	SCART recording/playback switch
11	SCART AF input
12	Demodulator tank circuit
13	Demodulator tank circuit
14	MUTE switch

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	16	V
Control voltage	V_6	4	V
DC voltages	$V_{4,5,6}$ $V_{10,11}$ $V_{12,13}$	0 to V_S 0 to V_S V_{REF} to V_S	V V V
DC currents	$I_{7,9}$	– 1 to 2	mA
Reference current	I_3	2	mA
IF input voltage m = 80%	$V_{I\,4,5\,rms}$	300	mV
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W

Operating Range

Supply voltage	V_S	10.5 to 15.75	V
Frequency	f	15 to 45	MHz
Ambient temperature	T_A	0 to 70	°C

Characteristics

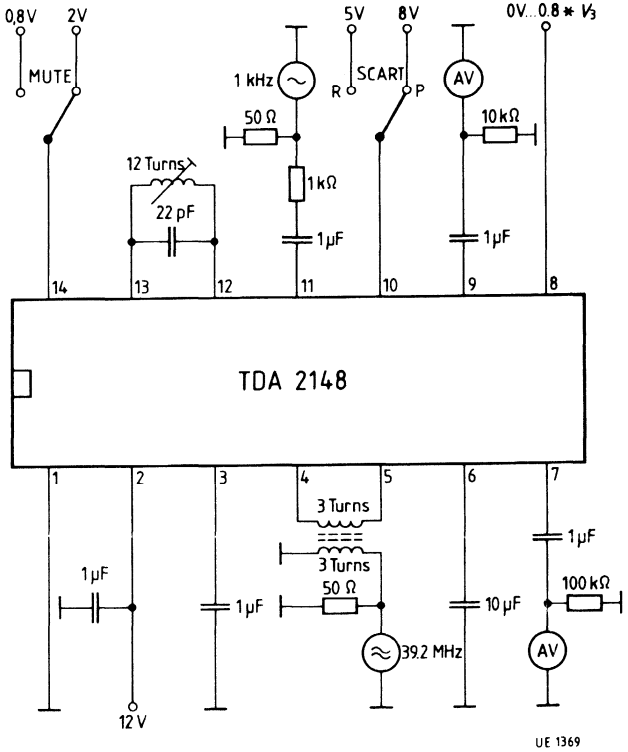
V_S = 12 V; T_A = 25 °C; f_{IIF} = 39.2 MHz; f_{mod} = 1 kHz

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption	I_S	25	38	50	mA
Reference voltage	V_3	5.4	6	6.6	V
Input voltage for control threshold V_{Q9} = ± 3 dB; m = 80%	$V_{I4,5}$	20	40	80	µV
AGC range V_{Q9} = ± 3 dB; m = 80%	ΔG	60	66		dB
SCART output voltage m = 80%; V_{IIF} = 1 mV;	V_{Q9}	700	800	900	mV
Controlled AF output voltage V_8 = 0.8 V_{REF}	V_{Q7}	650	800	950	mV
DC voltage portion V_{IIF} = 1 mV; m = 0%	V_9 V_7	3.5 5	4.0 6	4.5 7	V V
Total harmonic distortion V_{IIF} = 1 mV; V_8 = 0.8 V_{REF} m = 30% m = 80%	 THD_9 THD_7 THD_9 THD_7		 0.3 0.3 1 1	 1 1 2.5 2.5	 % % % %
Range for volume control V_8 = 0 V. . .0.8 V_{REF}	ΔG	80	85		dB
Gain SCART input/AF input V_8 = 0.8 V_{REF}	G_{11-7}	–1	0	1.5	dB
Input voltage SCART	$V_{I11\,rms}$	2			V

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C; $f_{I\,IF}$ = 39.2 MHz; f_{mod} = 1 kHz

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Design-Related Values					
Input resistance	$R_{I\,4,5}$		1.8		kΩ
Output resistance	$R_{Q\,12,13}$		6.6		kΩ
Input resistance	$R_{I\,11}$	20			kΩ
Input current	$I_{I\,8}$			15	µA
Output resistance	$R_{Q\,9}$			200	Ω
Output resistance	$R_{Q\,7}$			200	Ω
Cross-talk rejection V_{10} = 5 V; $V_{11\,rms}$ = 2 V	$\alpha_{11\text{-}7}$	60			dB
Control current ratio for high speed load circuit / integral control	Δi_6		140		
Switching Voltages					
SCART record	$V_{10\,L}$	0		5	V
playback	$V_{10\,H}$	8		V_S	V
MUTE OFF	$V_{14\,L}$	0		0.8	V
ON	$V_{14\,H}$	2		V_S	V
Switching Currents					
SCART record	$I_{10\,L}$	– 1		0	µA
playback $V_{10\,H}$ = 8 V	$I_{10\,H}$	30		150	µA
MUTE OFF	$I_{14\,L}$	0		3.5	µA
ON $V_{14\,H}$ = 2 V	$I_{14\,H}$	10		50	µA
ON $V_{14\,H}$ = 5 V	$I_{14\,H}$	80		250	µA

Test and Measurement Circuit



AV = Audivoltmeter

Simplified External Circuitry for the TDA 2148 Demodulator Circuit

The TDA 2148 AM (double side-band) demodulator circuit allows simplified external circuitry.

The new sound demodulator circuit, developed for application in television L standard and multistandard sets, provides the user with the following advantages:

Cost savings by not requiring the carrier select circuit (L, C) and the necessary tuning (time).

The circuit that is part of the carrier generation circuit, becomes unnecessary because of the excellent capture ratio features of the limiter.

Capture ratio defines the ability of a limiter amplifier, to distinguish a useable signal from an interference signal with a lower amplitude.

In this specific section, the modulation side-bands represent the interference signal and the carrier the useable signal (desired switching carrier).

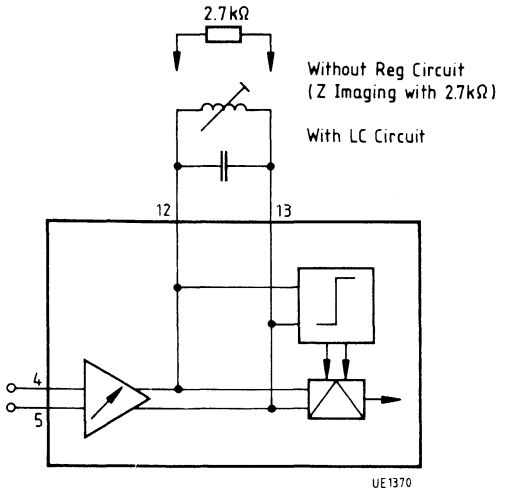
Even with a 100% modulation (France 80%) the distance from the side-bands to the carrier is 6 dB.

The system guarantees secure function. This is also shown by measurements with respect to:

harmonic distortion
noise
signal/noise ratio

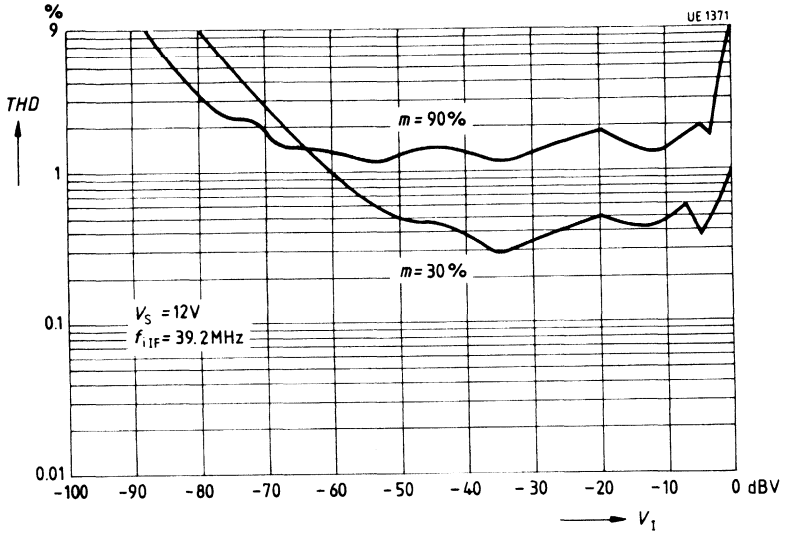
in a comparison with/without regenerative circuit. Only the control threshold shifts by 2 dB.

AM Demodulator Circuit



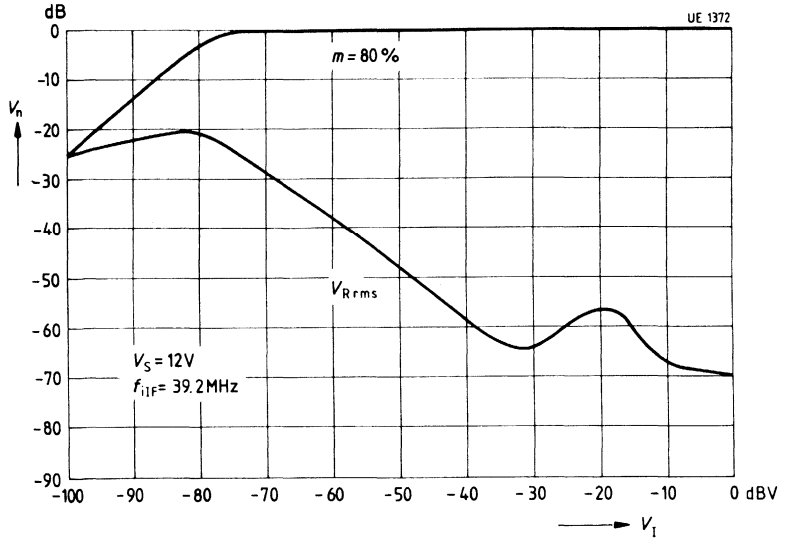
Circuit with LC Circuit

Total harmonic distortion versus input voltage
Standard circuit



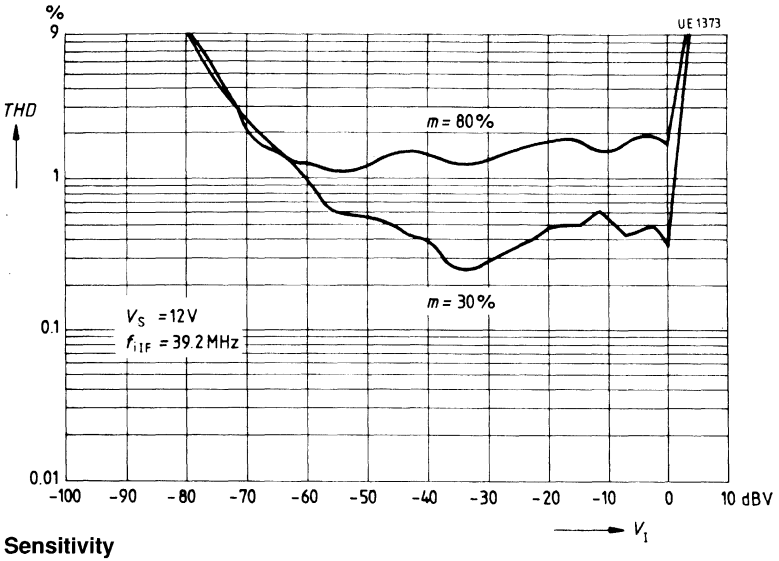
Sensitivity

Noise voltage versus input voltage
Standard circuit



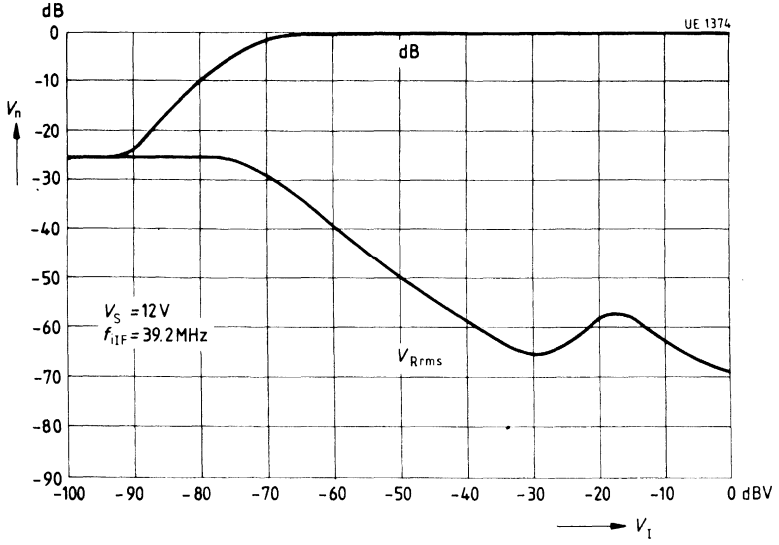
Circuit with R = 2.7 kΩ

Total harmonic distortion versus input voltage
Standard circuit



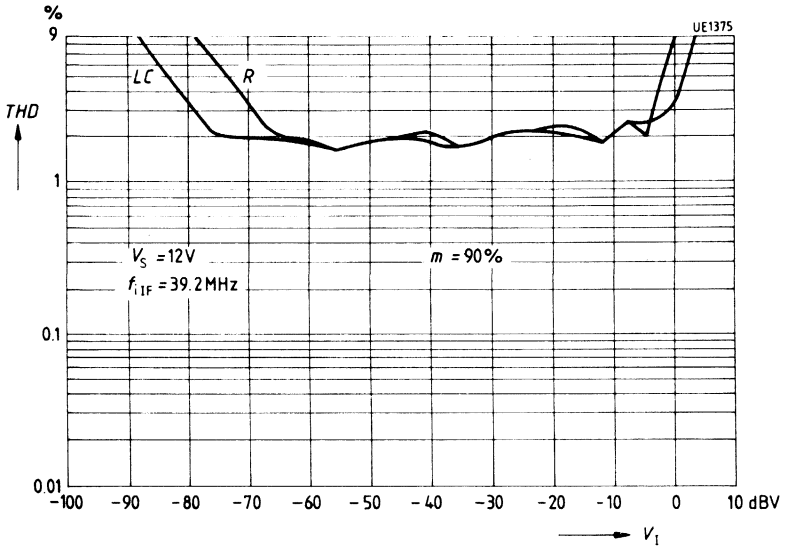
Sensitivity

Noise voltage versus input voltage
Standard circuit



Circuit with R = 2.7 kΩ

Total harmonic distortion versus input voltage



SIEMENS

Multistandard AM FM Sound IF IC — TDA 2460-2

Preliminary Data — **Bipolar IC**

Controlled AM IF amplifier including a quasi-synchronous demodulator and integral mean value control for French sound IF, limiter amplifier with FM demodulator, AF part with SCART input and output, volume control and AF output.

Features

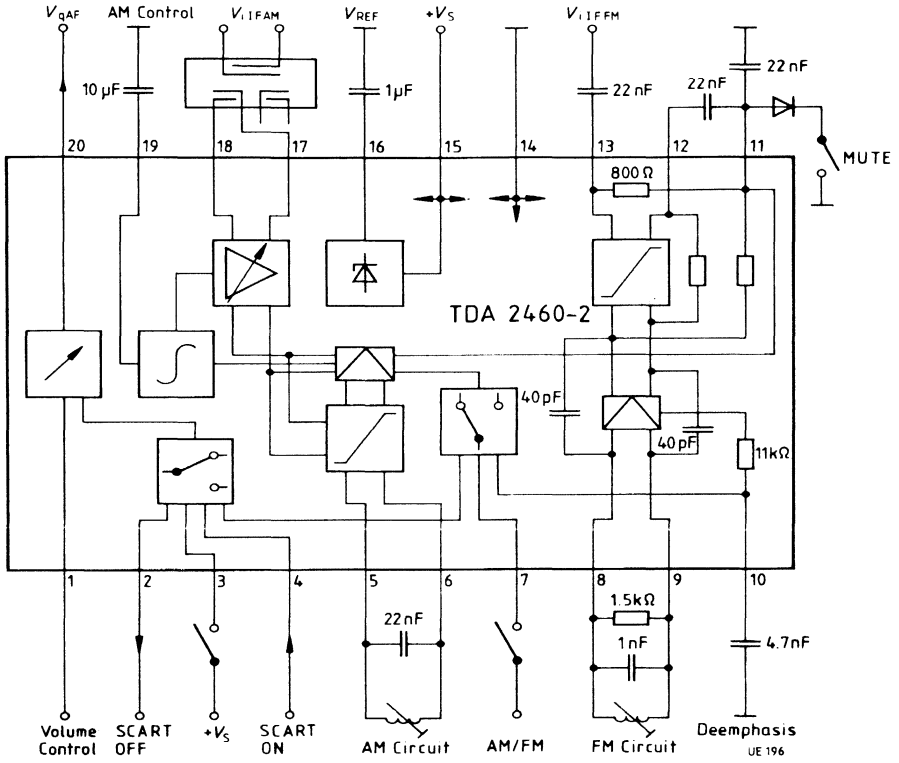
- Switch-over mode to CCIR standard for B/G and L systems
- Integral control for AF sound
- Standardized SCART interface
- High AM and FM sensitivity
- Low distortion factor

Type	Ordering Code	Package
TDA 2460-2	Q67000-A8200	P-DIP-20

Circuit Description

The component contains a four-stage, capacitatively coupled control amplifier, a quasi-synchronous demodulator, an integral mean value control voltage generator and an AF pre-amplifier according to the French sound IF standard. The FM section contains an eight-stage symmetrical limiter amplifier with a coincidence modulator and an AF pre-amplifier with connection for the deemphasis capacitor. The two AF sources are routed to the volume control via an analog switch of the SCART socket and a record/playback switch.

Block Diagram



Pin Definitions and Functions

Pin No.	Function
1	Volume control adjustment voltage for AF output
2	SCART AF output
3	SCART recording/playback switch
4	SCART AF input
5	Demodulator circuit AM
6	Demodulator circuit AM
7	AM/FM bidirectional switch
8	Demodulator circuit FM
9	Demodulator circuit FM
10	Deemphasis FM
11	Operation point feedback input FM and muting
12	Operation point feedback FM
13	AF input FM
14	GND
15	Supply voltage
16	Reference voltage
17	IF input AM
18	IF input AM
19	Control time constant AM amplifier
20	AF output

Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	16	V
Control voltage	V_{19}	4	V
Reference current	I_{REF}	2	mA
DC voltages	$V_{3,4,7,10}$ $V_{17,18,1}$ $V_{11,12,13}$ $V_{5,6}$	V_S V_S V_{REF} V_{REF} to V_S	V V V V
DC currents	$I_{2,20}$ $I_{8,9}$	– 1 to 2 2	mA mA
IF input voltage AM m = 80%	$V_{I\,17/18\,rms}$	300	mV
IF input voltage FM	$V_{I\,13\,rms}$	600	mV
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 55 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	58	K/W

Operating Range

Supply voltage	V_S	10.5 to 15.75	V
Frequency range AM	f_{AM}	15 to 45	MHz
Frequency range FM	f_{FM}	0.1 to 12	MHz
Ambient temperature	T_A	0 to 70	°C

Characteristics

V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption	I_S	48	61	75	mA
Supply voltage	V_{15}	10.5		15.5	V
AM Section					
f_{IIF} = 39.2 MHz; f_{mod} = 1 kHz					
Input voltage for AGC threshold m = 80%; V_2 (at $V_{17/18}$ = 1mV) – 3 dB	$V_{I\,17/18}$		40	80	µV
AGC range m = 80%; V_2 (at $V_{17/18}$ = 1 mV) ± 3 dB	ΔG	60	66		dB
Output voltage (SCART) V_{IIF} = 1 mV; m = 80%	$V_{Q\,2\,rms}$	700	800	900	mV
Controlled AF output voltage V_1 = 0.8 V_{REF}; V_{IIF} = 1 mV; m = 80%	$V_{Q\,20\,rms}$	650	800	950	mV
DC voltage V_{IIF} = 1 mV; m = 0	$V_{Q\,2}$ $V_{Q\,20}$	3.5 5	4.0 6	4.5 7	V V
Total harmonic distortion V_{IIF} = 1 mV; V_1 = 0.8 V_{REF}; m = 30% m = 80%	 THD_2 THD_{20} THD_2 THD_{20}		 0.3 0.3 1 1	 1 1 2.5 2.5	 % % % %

Characteristics (cont,d)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
FM Section f_{IIF} = 5.5 MHz; f_{mod} = 1 kHz					
Input voltage for limiter threshold (V_{Q2} = – 3 dB) Δf = ± 50 kHz	$V_{I13\,rms}$		40	80	µV
Output voltage (SCART) Δf = ± 50 kHz; V_{IIF} = 10 mV	$V_{Q2\,rms}$	850	1200		mV
Controlled AF output voltage V_I = 0.8 V_{REF}	$V_{Q20\,rms}$	850	1200		mV
DC voltage portion V_{IIF} = 10 MV; Δf = 0; THD_{min}	V_{Q2} V_{Q20}	3.6 5	4.1 6	4.6 7	V V
Total harmonic distortion Δf = ±12.5 kHz; V_{IIF} = 10 mV	THD_2		0.2	0.3	%
Total harmonic distortion controlled AF output V_1 = 0.8 V_{REF}	THD_{20}		0.2	0.3	%
AM suppression V_{IIF} = 500 µV; m = 30%	α_{AM}	60	70		dB

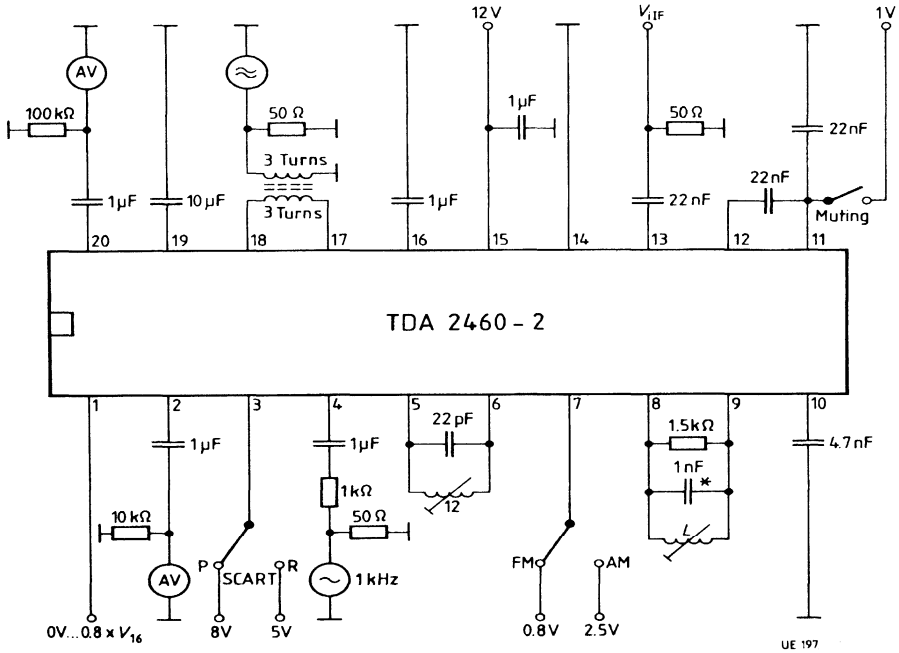
Characteristics
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
AF Section					
AGC range for volume control V_1 = 0 V. . .0.8 V_{REF}	ΔG	80	85		dB
Gain SCART input/AF output V_1 = 0.8 V_{REF}	$V_{4\text{-}20}$	– 1	0	1.5	dB
Input voltage SCART	$V_{I\,14\,rms}$	2			V
Switching voltage SCART Playback Record	 V_3 V_3	 8 0		 V_S 5	 V V
Switching voltage muting ON (AF off) OFF	 V_{11} V_{11}	 0 5		 1 V_S	 V V
Switching voltage FM AM	V_7 V_7	0 2.5		0.8 6	V V

Characteristics
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Design-Related Values					
Input resistance	$R_{I\,8,9}$	22			kΩ
Output resistance	$R_{Q\,2,20}$			200	Ω
Input impedance	$Z_{11,13}$		800		Ω
Frequency deviation AM$_{min}$ / THD_{min} f_{FM} section			± 10		kHz
Input resistance	$R_{17/18}$		1.8		kΩ
Output resistance	$R_{5/6}$		6.6		kΩ
Input resistance	R_4	20			kΩ
Input current	I_1			15	µA
Cross-talk rejection V_3 = 5 V; $V_{4\,rms}$ = 2 V	$\alpha_{4\text{-}20}$	60			dB
Control current ratio for high speed load circuit/integral	Δi_{19}		140		
Switching Currents					
SCART record	I_{3L}	– 1		0	µA
SCART playback V_3 = 8 V	I_{3H}	30		150	µA
MUTE OFF ON	I_{11H} I_{11L}	– 1 3		0 50	µA
AF/FM switch FM AM (V_7 = 5 V)	I_{7L} I_{7H}	– 1 80		0 250	µA

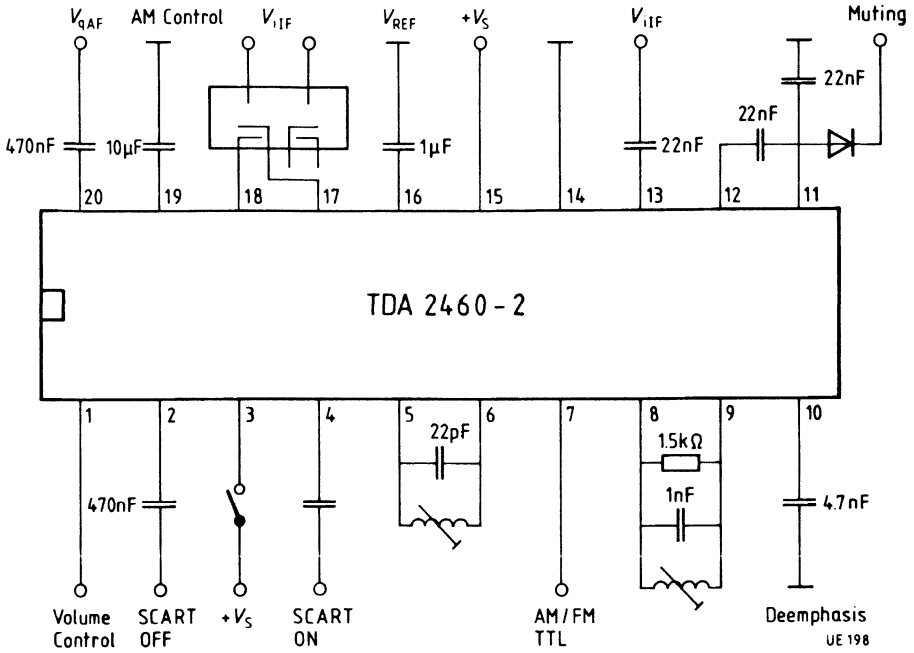
Test and Measurement Circuit



L = 10 Turns 0.2 CuL; Q_B approx. 25
e.g. Coil Assembly Vogt 5171200000

* STYROFLEX Capacitor
AV = Audio Voltmeter

Application Circuit



Simplified External Circuitry for the TDA 2460 Demodulator Circuit

The TDA 2460 AM (double side-band) demodulator circuit allows simplified external circuitry.

The new sound demodulator circuit, developed for application in television L standard and multistandard sets, provides the user with the following advantages:

Cost savings by not requiring the carrier select circuit (L, C) and the necessary tuning (time).

The circuit that is part of the carrier generation circuit becomes unnecessary because of the excellent capture ratio features of the limiter.

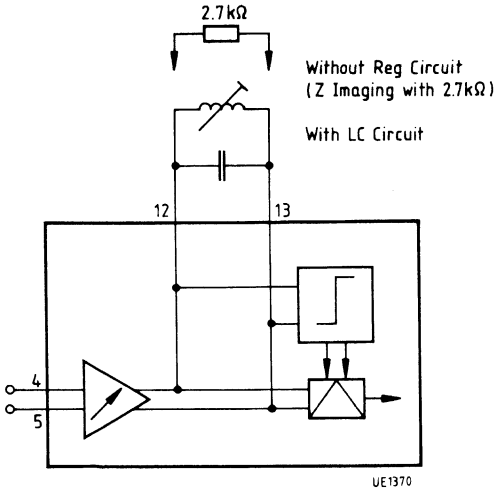
Capture ratio defines the ability of a limiter amplifier to distinguish a useable signal from an interference signal with a lower amplitude.

In this specific section, the modulation side-bands represent the interference signal and the carrier the useable signal (desired switching carrier).

Even with a 100% modulation (France 80%) the distance from the side-bands to the carrier is 6 dB.

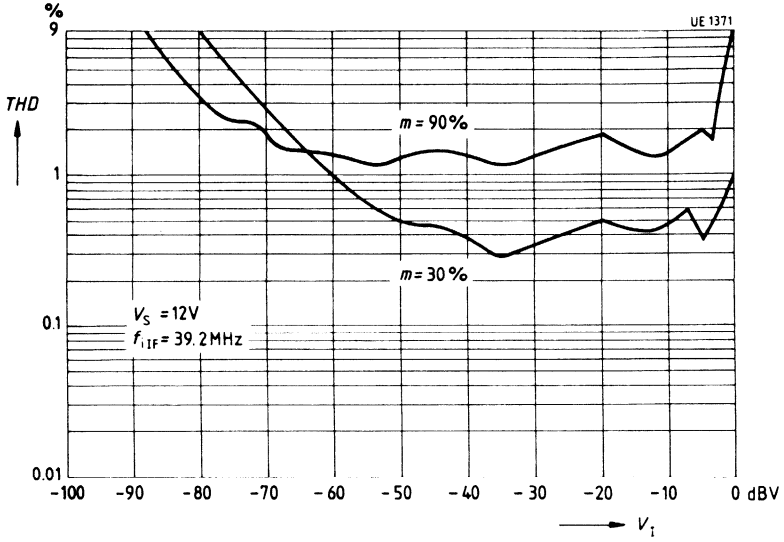
The system guarantees secure function. This is also shown by measurements with respect to:
harmonic distortion
noise
signal/noise ratio
in a comparison with/without regenerative circuit. Only the control threshold shifts by 2 dB.

AM Demodulator Circuit



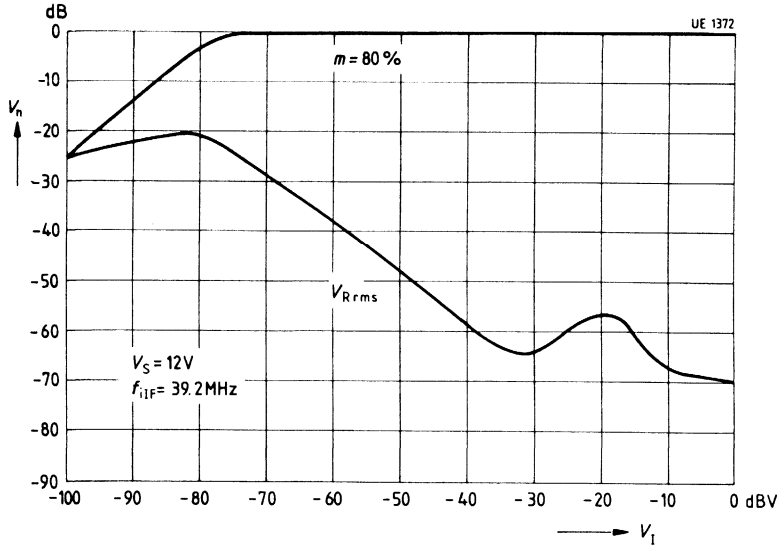
Circuit with LC Circuit

Total harmonic Distortion versus Input voltage
Standard Circuit



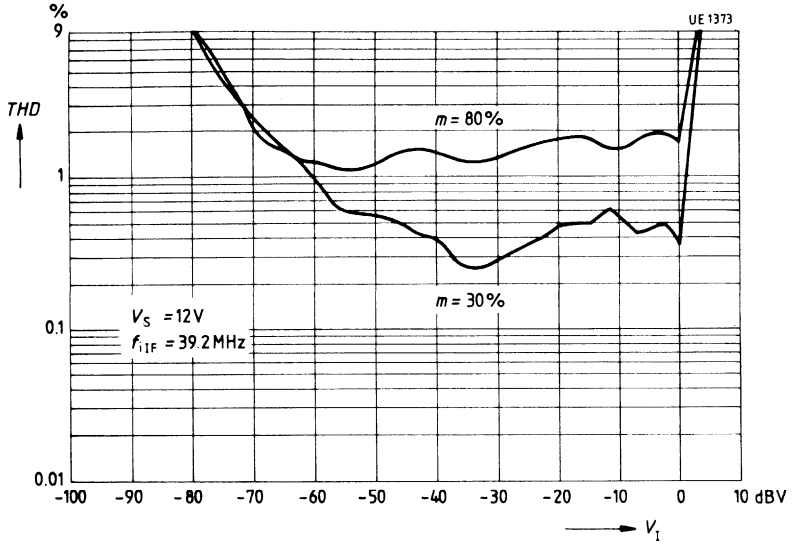
Sensitivity

Noise voltage versus input voltage
Standard circuit



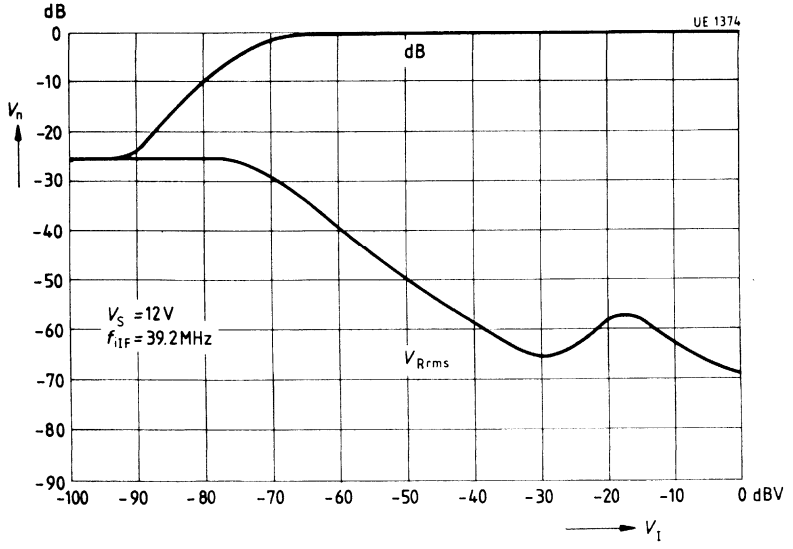
Circuit with R = 2.7 kΩ

Total harmonic distortion versus input voltage
Standard circuit



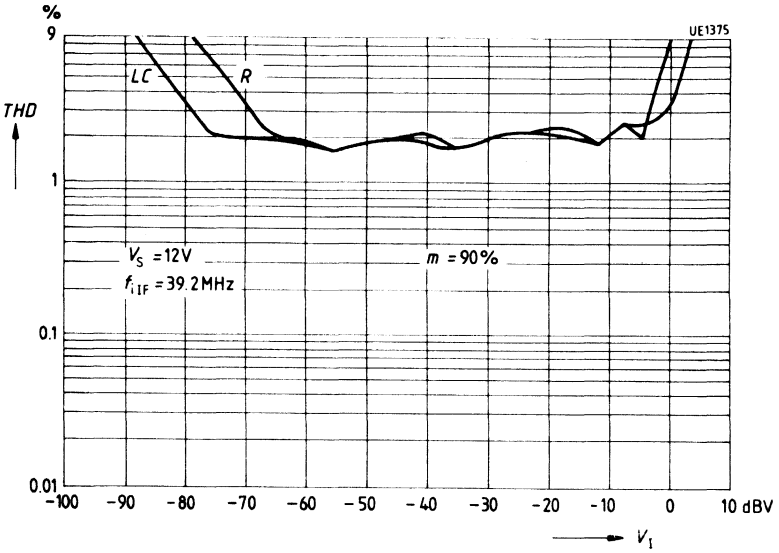
Sensitivity

Noise voltage versus input voltage
Standard circuit



Circuit with R = 2.7 kΩ

Total harmonic distortion versus input voltage



SIEMENS

AM Receiver for AM Stereo

TDA 4010

Preliminary Data

Bipolar IC

Features

- Internal demodulation
- Search tuning stop signal
- Low total harmonic distortion
- Minimal IF leakage at the AF output
- 2-stage integrated low pass
- Standard IF-output

Type	Ordering Code	Package
TDA 4010	Q67000-A8074	P-DIP-18

Circuit Description

Compared to TDA 4001 the TDA 4010 is an extended AM-receiver. This type is suitable for applications in car radios.
The IF-output $V_{Q\,IF}$ is at pin 15.

The monolithic integrated bipolar receiver has been designed to convert, amplify and demodulate AM-signals. In addition, the component provides a search tuning pulse.

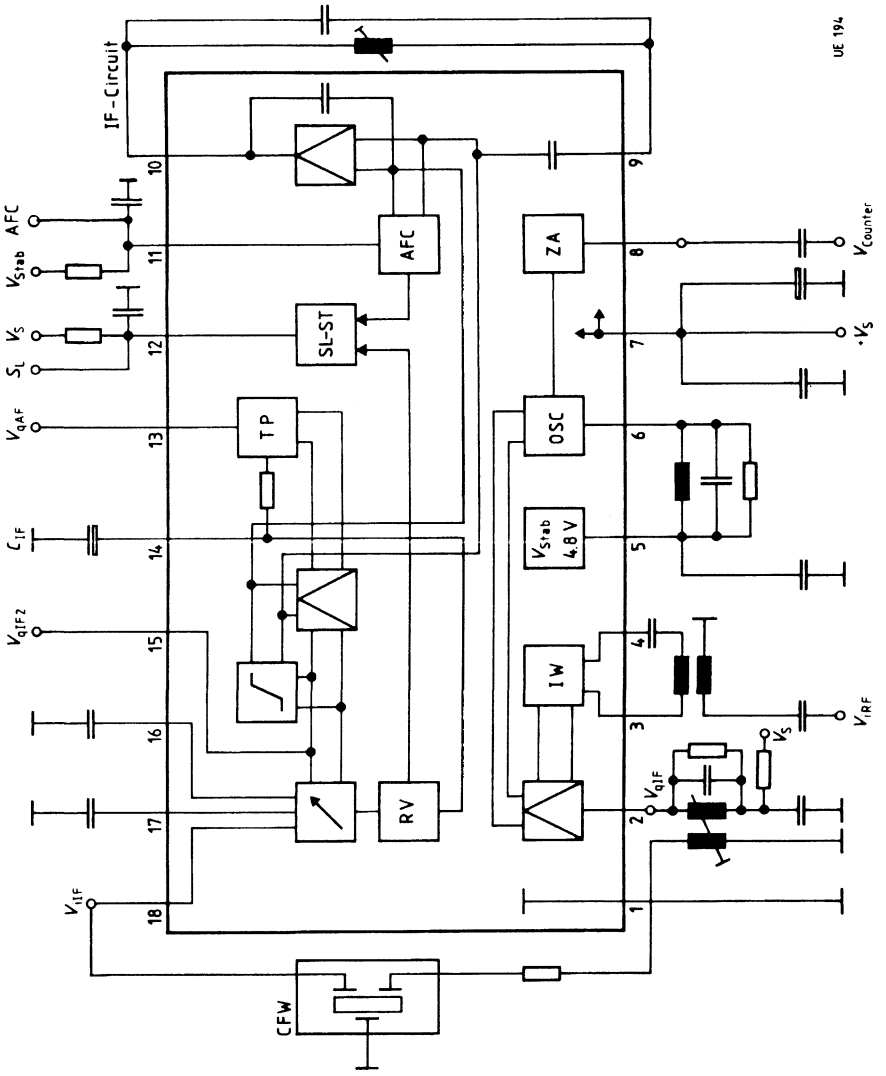
The search tuning stop pulses are processed from the input signal.

The standard AM-IF signal is available at the output of the IF-receiver.

The impedance converter forwards the input signal V_{iRF} to the symmetrical double balanced mixer. Subsequently the signal is converted to IF with the amplitude-controlled oscillator. An external filter forwards the IF signal to the controlled IF amplifier. The amplifier IF signal and the carrier signal will be converted to AF in the subsequent synchronous demodulator. The 2-stage low pass filter forwards the available AF to the AF output.

Via an additional limiter amplifier (LA), the AF uses the carrier signal to control the coincidence demodulator (CD). The output signal of the coincidence demodulator provides the stop pulse during exact tuning and sufficient field strengh.

Block Diagram



Pin Functions

Pin No.	Function
1	Ground
2	Mixer output, IF circuit
3	RF-input
4	RF-input
5	V_{Stab}
6	Oscillator
7	Supply voltage
8	Counter output
9	FM-demodulator circuit IF circuit
10	FM-demodulator circuit IF circuit
11	AFC-output
12	Search tuning stop output
13	AF-output
14	IF-time constant
15	Controlled IF-output
16	IF-operating point follow up device
17	IF-operating point follow up device
18	IF-input

Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Operating voltage	V_S		16.5	V
Current consumption	I_S		33	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C

Thermal Resistance

Chip ambient	$R_{th\,SU}$		78	K/W
Chip package	$R_{th\,SG}$			

Operating Range

Operating voltage	V_S	7	15	V
Temperature range	T_A	– 25	85	°C

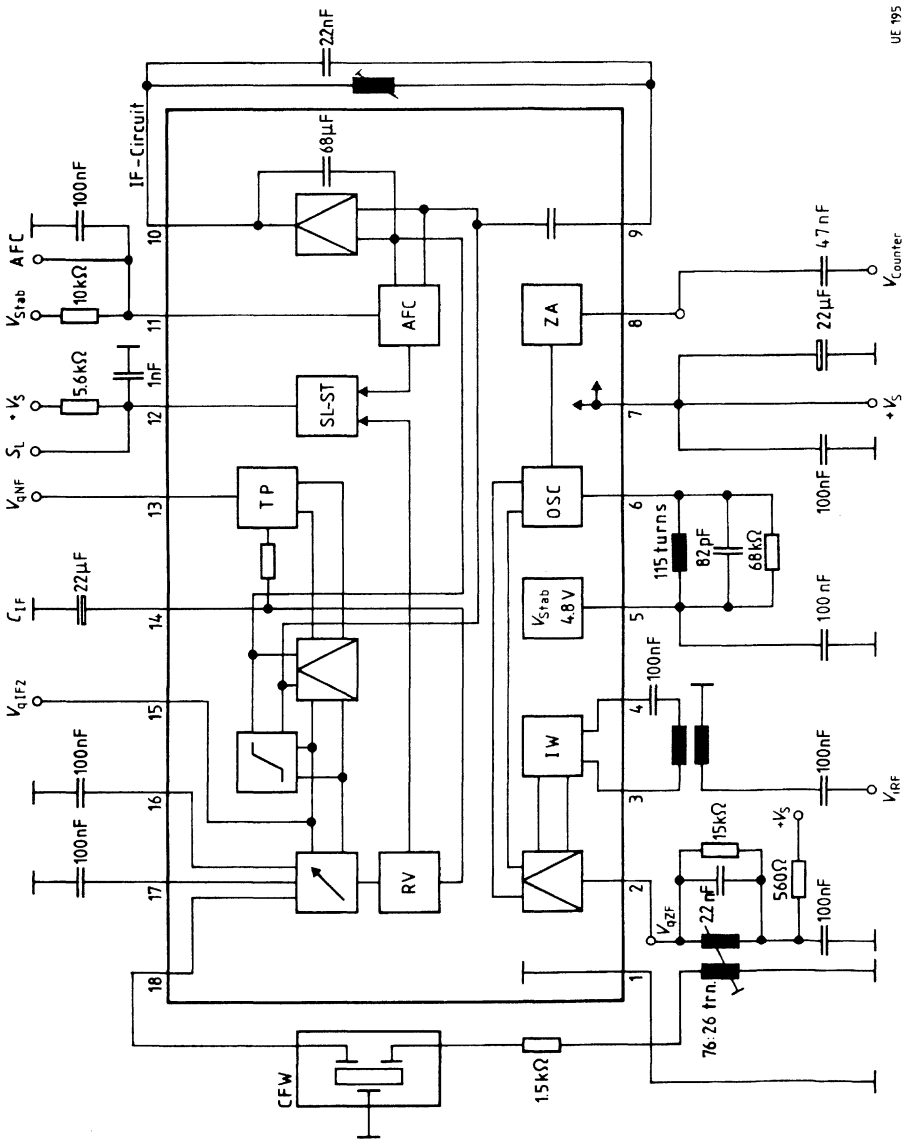
Characteristics
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_S	9	15	30	mA	
Reference voltage	V_{Stab}	4.2	4.8	5.4	V	
IF-output voltage	$V_{Q\,IF}$	600	800 300	1000	mV rms mV rms	m = 0.8 m = 0.3
Total harmonic distortion	THD	m = 0.8		2.5 1	% %	m = 0.8 m = 0.3
IF-output voltage	$V_{Q\,IF}$			3	dB	20xlg(V_{QNF}/30mV0: V_{QNF}/1mV)
Input sensitivity	$V_{I\,RF}$	30	30		µV rms	V_{qNF} for V_{iHF} = 1mV – 3dB
Signal-to-noise ratio	$\frac{S+N}{N}$		6		dB	m = 0.3 V_{iHF} = 10 µVrms
Signal-to-noise	$S+N$	44	46		dB	m = 0.3 V_{iHF} = 1mV
Oscillator voltage	V_{OSC}		100		mV pp	
Counter output voltage	V_{QC}			100	mV pp	
Control range (ΔV_{qIF} = 6dB)	a	60			dB	
3dB limit frequency of the integrated TP	f_g		5		kHz	

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
IF-suppresion	a_{IF}		40		dB	
Conversion gain	V_m		30		dB	
IF-output pin 15	V_{QIF}	8	10	22	mV rms	1MΩ/1.5pF
AFC-offset current without signal	I_{AFC}			± 25	µA	
AFC-offset current over control range	ΔI_{AFC}			± 25	µA	
AFC-current	I_{AFC}	± 60		± 100	µA	f_{IF} = 1MHz ± 3kHz
SLS-output voltage	V_{12}			0.4	V	f_{IF} = 455kHz
SLS-output voltage	V_{12}	11			V	f_{IF} = 0V
SLS-output voltage	V_{12}	11			V	f_{IF} > 455kHz + 3kHz
SLS-output voltage	V_{12}	11			V	f_{IF} > 455kHz – 3kHz
Input impedance	Z_{IRF}		10/1.5		kΩ//pF	pin 3, 4
Input impedance	Z_{IRF}		3.3/1.5		kΩ//pF	pin 18

Test Circuit



SIEMENS

Infrared Preamplifier

TDA 4050-B

Preliminary Data

Bipolar IC

Features

- Internal AGC
- Superior large signal stability
- Short-circuit proof signal output
- Simple connection for an active band filter
- Few external components

Type	Ordering Code	Package
TDA 4050-B	Q67000-A1373	P-DIP-8

Absolute Maximum Ratings

Parameter	Symbol	Limit Valued	Unit
Supply voltage	V_S	16[1)]	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	140	K/W

Operating Range

Supply voltage	V_S	9 to 16	V
Ambient temperature	T_A	0 to 70	°C
Input frequency	f_I	0 to 100	kHz

[1)] intermittently 17.5 V

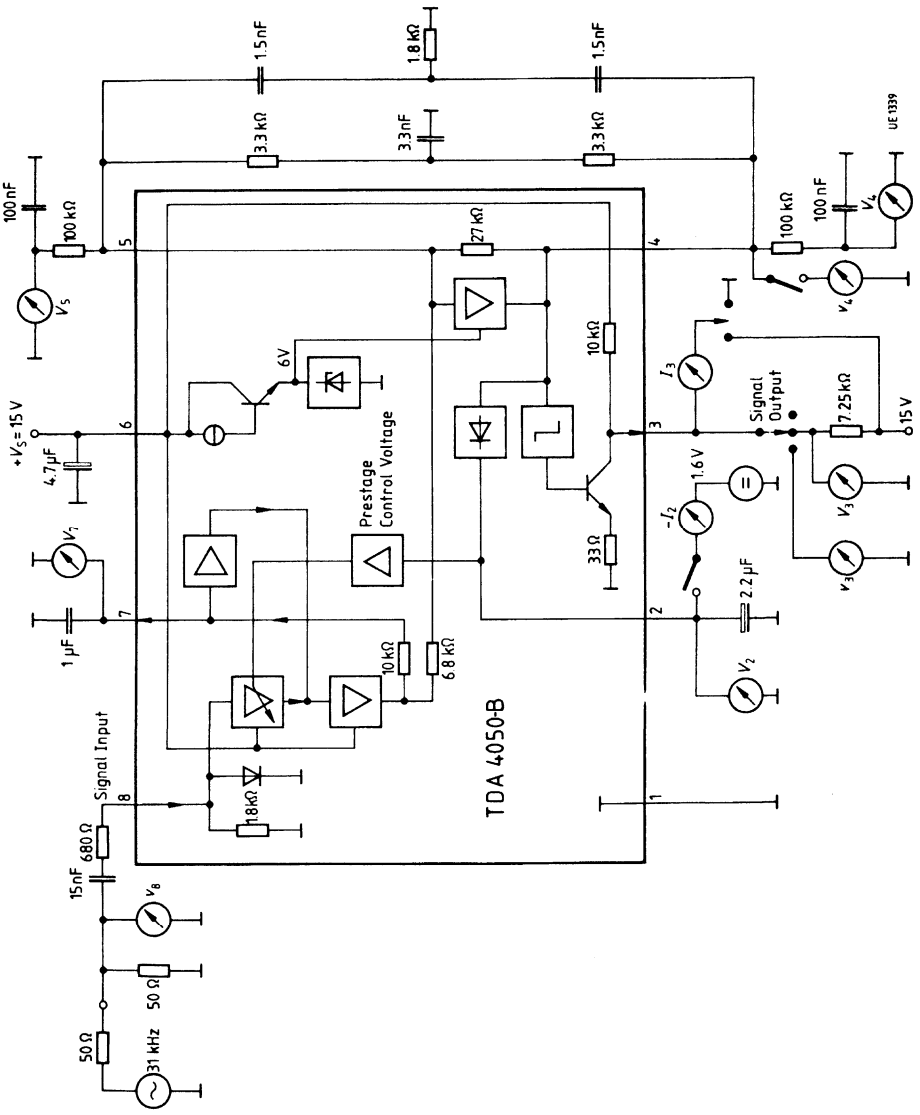
Characteristics
V_S = 15 V; T_A = 25 °C; f_{IR} = 31 kHz; referred to measurement circuit

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption ($R_L \geq 10$ kΩ)	I_6	6	9	12	mA
Input voltage for control start	$v_{8\,rms}$		50		μV
Input voltage for output signal	$v_{8\,rms}$			85	μV
Filter output voltage (in control range)	$v_{4\,rms}$	350	450	550	mV
Gain	$G_{4/8}$	74	77	85	dB
Gain	$G_{3/4}$		21		dB
Total control range	ΔG	74	77	85	dB
Control voltage without input signal	V_2	1325	1425	1525	mV
Control voltage ($v_{8\,rms}$ = 100 μV)	V_2	1.5		2.1	mV
Control voltage ($v_{8\,rms}$ = 10 mV)	V_2	1.9		2.45	V
Control voltage ($v_{8\,rms}$ = 1 V)	V_2	2.1		2.6	V
Operating points	$V_{4/5/7}$	2.2		2.8	V
Output current ($V_3 = V_S$)	I_{Q3}		20		mA
DC output voltage for L level	V_{3L}		150	500	mV
DC output voltage for H level	V_{3H}	14.6			V
Charge current $v_{8\,rms}$ = 100 mV; V_2 = 1.6 V	$-I_2$	0.4		1.0	mA
Discharge current $v_{8\,rms}$ from 1 mV to 0 T = 50 ms	I_2	0.4		3.0	μA
Input resistance	R_{I8}		1.8		kΩ
Output resistance	R_{Q3}		10		kΩ
Rated resistance of the double-T network at pin 4 (unbalanced to ground)	R_4	2			kΩ

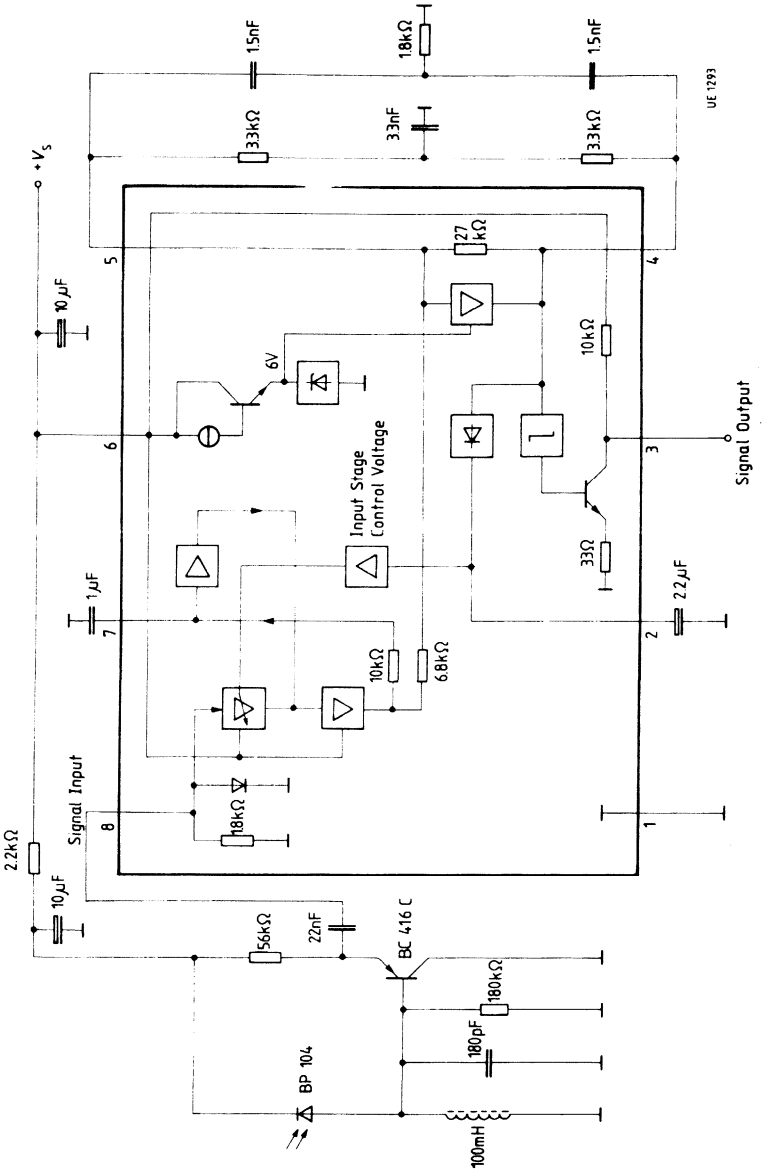
Pin Functions

Pin No.	Function
1	GND
2	Connection for capacitance for prestage control
3	Output threshold amplifier
4	Output active filter
5	Input active filter
6	Supply voltage, positive
7	Unlocking of operating point control
8	Signal input

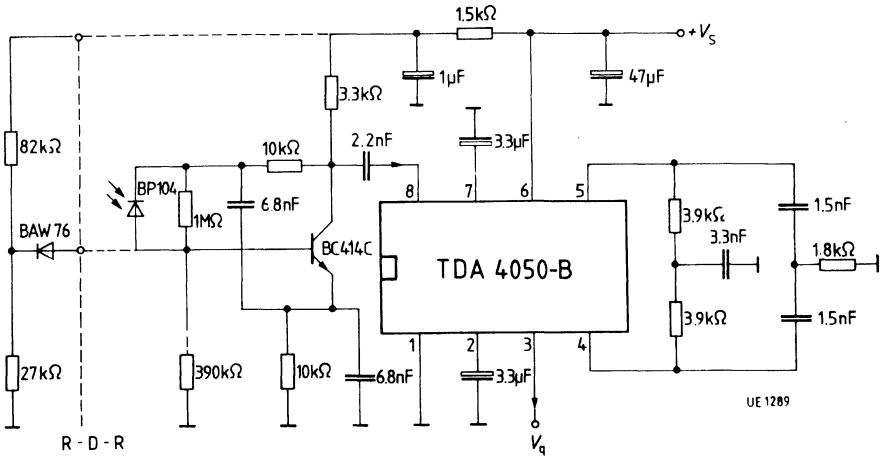
Measurement Circuit and Block Diagram



Application Circuit 1
incl. LC input selection



Application Circuit 2
without coil



Notes

Circuit 1 uses an LC resonant circuit and is of superior quality due to its high selectivity feature (approx. 3 kHz bandwidth at – 3 dB).

Circuit 2 offers the lower cost solution without coil incl. broadband input selection. Higher requirements as to steady radiation and large signal stability can be met by means of resistor-diode-resistor connection (RDR).

SIEMENS

Infrared Signal Receiver

TDA 4065

Preliminary Data

Bipolar IC

Features

- High input sensitivity
- Improved compensation for extraneous light (in range of normal indoor illuminance)
- Reduction of external circuitry to three components (IR diode and two capacitors)
- Built-in demodulator in P-DIP-8/P-DSO-8 package
- Integrated bandpass filter for 30 kHz
- Optimally attuned to SDA 2208-3 transmitter

Type	Ordering Code	Package
TDA 4065	Q67000-A8246	P-DIP-8
TDA 4065-X	Q67000-A8247	P-DSO-8

The digital signals received by an infrared detector diode have to be amplified and demodulated. These are the tasks of the integrated device, whose applications are primarily in radio, television and video engineering.

Functional Description and Application

Input INFRA

The input exhibits high impedance. The external IR diode leads with its cathode to the device. The anode is on ground. Only currents of the order of nanoamperes are required for driving. It is consequently advisable to place the infrared diode directly on the INFRA input.

Pin CS

Wiring with CS gives the internal preamplifier an RC highpass characteristic. In this way the low-frequency signals on the IR diode that are produced by the light of bulbs or daylight are damped.

Pin CREG

The gain of the preamplifier can be regulated. The larger the RF input signal, the more the gain is regulated downwards. The time constant is determined by CREG. The control characteristic is optimized to the instruction code of SDA 2208-3.

Pin CG

If the pin is wired to ground with a resistor, the preamplifier works with adjustable gain in open-loop control. Pin CREG is then on ground. In a heavily disturbed environment it may be of advantage to wire a capacitor to ground.

Output

This is a single-ended output (collector of NPN transistor) with a pullup resistor. For longer lines it may be necessary to connect a capacitor to ground on the output.

General

The pinning was selected to minimize any crosstalk between critical pins. This should also be taken into consideration in board layout. It may be necessary to block the supply voltage with a capacitor, especially because of the current swing produced by the output.

Circuit Description

An infrared diode usually detects - besides the required signal - the infrared spectrum of the incident daylight, the 100-Hz hum of incandescent lamps and parts of the spectrum of fluorescent lamps.

The current source shown in the block diagram compensates the unwanted, low-frequency diode currents and at the same time stabilizes the operating point at the input of the preamplifier.

Operation with closed-loop-control preamplifier:

In the internal, low-noise preamplifier the signal is boosted to produce sufficient amplitude for the demodulator. The gain of the preamplifier is regulated as a function of the input amplitude. If the signal amplitude is sufficiently greater than the noise amplitude (eg from a fluorescent lamp), this regulation of the gain will prevent the noise amplitude from overdriving the amplifier and causing the useful signal to be engulfed. Thus disturbed signals can also be evaluated (with restricted sensitivity). If no useful signal is received, no noise spikes will appear on the output in closed-loop control.

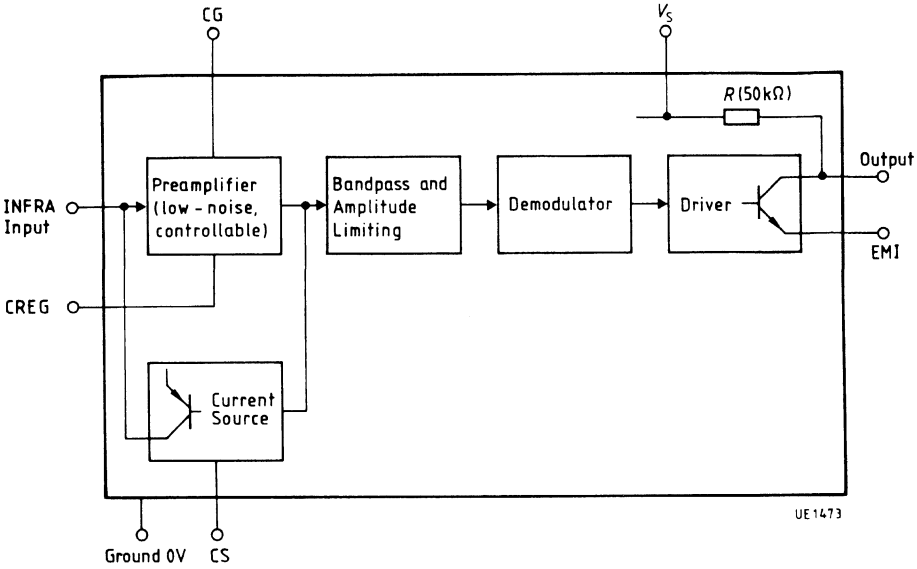
Operation with open-loop-control preamplifier:

With an instruction code that has a greater mark-to-space ratio than that wich is produced by SDA 2208-3, there may be a reduction in sensitivity in closed-loop control. Then there is the possibility of operating the device with open-loop control instead of closed-loop control. The preamplifier can handle large signal amplitudes and is proof against overdriving. For this reason the noise immunity is similar to that in closed-loop control. In open-loop control the sensitivity is independent of the instruction code that is used. If the greatest possible sensitivity is to be achieved, adjustment will be necessary in open-loop control. There may then be occasional noise spikes on the output.

The bandpass filter following the preamplifier enhances the signal/noise ratio of the signal. This reduces the edge jitter of the output signal.

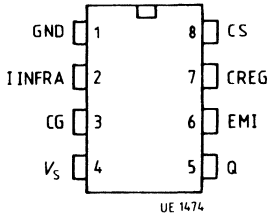
The demodulator charges or discharges an internal capacitance with constant currents. Charging occurs when a signal is applied. When the switching threshold on the capacitance is exceeded, the driver output becomes low. Falling below the switching threshold occurs with hysteresis. In the absence of an input signal the output is high.

Block Diagram

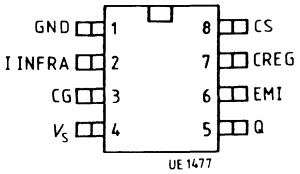


Pin Configuration
(top view)

P-DIP-8



P-DSO-8



Pin Definitions and Functions

Pin No.	Symbol	Function
1	GND	Ground 0V
2	I INFRA	Input INFRA
3	CG	CG
4	V_S	Supply voltage V_S
5	Q	Output
6	EMI	Emitter EMI
7	CREG	CREG
8	CS	CS

Absolute Maximum Ratings
T_A = 0 to 70 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.3	7	V	
Input INFRA	I_{INFRA}		10	mA	
Output	V_Q I_Q	– 0.3 0	7 3	V mA	Output disabled Output conducts
CS, CREG, CG	$I_{CS, CREG, CG}$		10	mA	
EMI	V_{EMI}	– 0.3	5	V	
Thermal resistance system-case P-DIP-8	$R_{th\ SC}$		100	K/W	
Storage temperature	T_{stg}	– 40	125	°C	

Operating Range

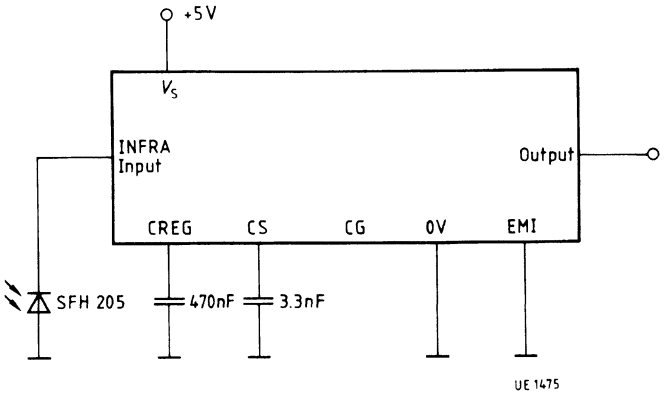
Supply voltage	V_S	3.5	6.5	V	
Current through current source on input INFRA	I_{Source}	0	700	µA	
Current through output transistor	I_{COL}	0	1	mA	
Frequency range (for carrier)	f	25	40	kHz	
Ambient temperature	T_A	0	70	°C	

Characteristics
V_S = 4.5 to 5.5 V; T_A = 0 to 70 °C

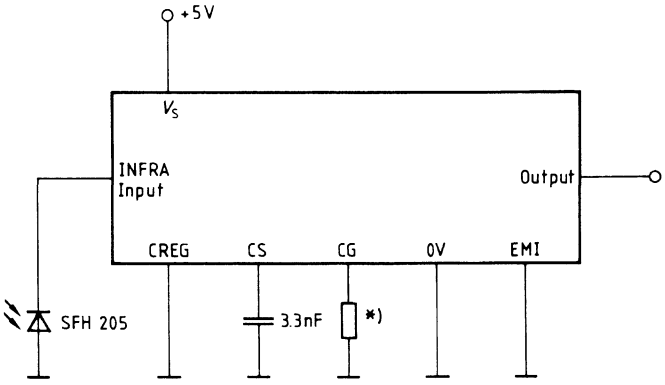
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_S		600		µA	Output open; I_Q=0 mA
Input sensitivity for secure signal on output	I_{Signal}		3		nA pp	Diode DC current $I_{Diode} = I_{Source}$ I_{Diode} < 1 µA f_C = 30 kHz
			5		nA pp	I_{Diode} < 10 µA
			6		nA pp	I_{Diode} < 30 µA
			7		nA pp	I_{Diode} < 100 µA
			10		nA pp	I_{Diode} < 500 µA
Output current (output HIGH)	I_Q			10	µA	0 < V_Q < 7 V
Output voltage (output LOW)	V_Q			0.4	V	0 < I_Q < 100 µA
Resistance	R		50		kΩ	

Application Circuit

Operation with Closed-Loop-Control Preamplifier



Operation with Open-Loop-Control Preamplifier



*) Approx. 30 to 100 kΩ,
depending on required gain

SIEMENS

FM IF IC with Search Tuning Stop Pulse, Field Strength Indicator, MUTE Setting and Multipath

TDA 4210-3

Bipolar IC

The TDA 4210-3 has been designed as FM IF component with a special demodulator for application in car radios. The sensitivity level of the input amplifier can be adjusted for applications with search tuning mode. In addition, a search tuning stop pulse is generated. Moreover, the included multipath identification circuit activates an interference suppression circuit in case of multipath interference. The TDA 4210-3 is especially suitable for application in car radios and home receivers which require a search tuning stop pulse and include an interference suppression circuit.

Features

- Multipath identification circuit
- 7-stage limiter amplifier
- Product demodulator
- AFC output
- Field strength dependent volume control
- Generation of search tuning stop pulse
- Adjustable limiter threshold
- Adjustable muting depth

Type	Ordering Code	Package
TDA 4210-3	Q67000-A8008	P-DIP-18

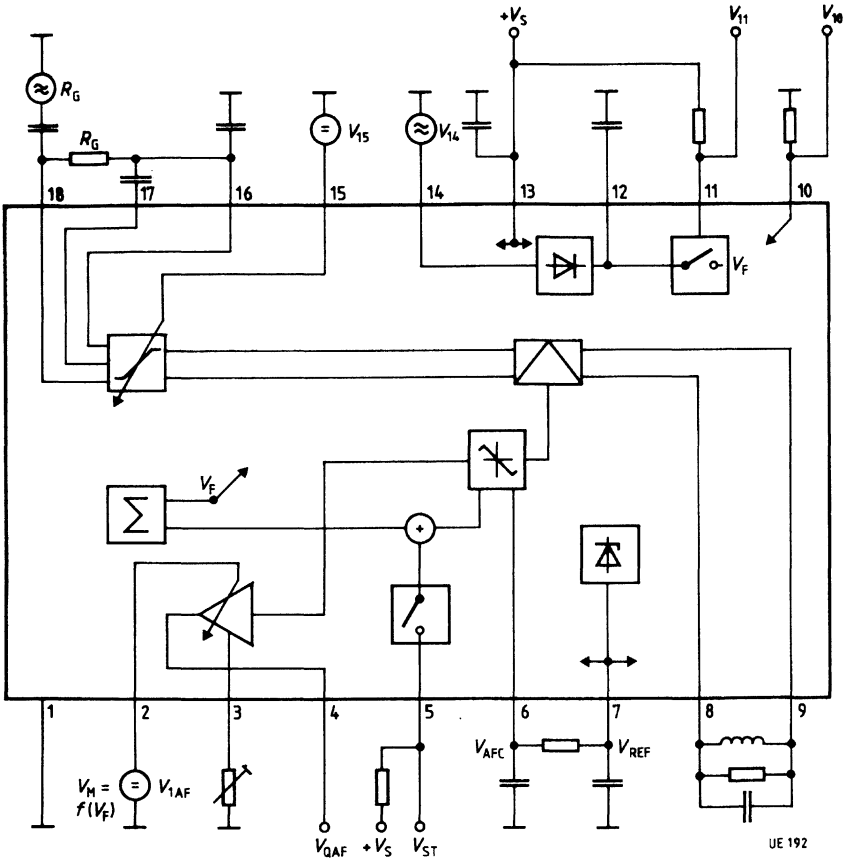
Circuit Description

The integrated circuit includes a 7-stage limiter amplifier with demodulator and non-controlled AF output. The limiter threshold can be raised by approx. 44 dB by means of external circuitry. Within this range the AF output signal can be continuously attenuated by 39 dB typical to eliminate the usually occurring noise products.

To suppress variable interference products, e.g. multipath interference, the TDA 4210-3 includes an identification circuit with an externally adjustable time constant.

Also included are a field strength output, an AFC output, as well as an open collector output. The latter will be activated at zero crossing of the detector S-curve.

Block Diagram



Pin Functions

Pin No.	Function
1	Ground capacitors for operating point feedback, V_S, and V_{REF} decoupling are to be connected directly to pin 1
2	MUTE input (usually derived from field strength output voltage)for DC voltage which attenuates the AF output voltage by the set muting depth (pin 4). Max. attenuation when $V_2 = 0$ V, no attenuation when $V_2 \geq 0.75$ V
3	Muting depth adjustment by connecting a resistor to ground the required muting depth can be set. Maximal attenuation of AF output voltage with R = 0 (approx. 46 dB), minimal attenuation with $R = \infty$ (approx. 7 dB)
4	AF output for demodulated FM-IF
5	Search tuning stop (ST) output is connected when the input field strength exceeds the search tuning stop pulse threshold and the input frequency lies within the search tuning stop pulse window.
6	AFC output: push-pull current output, referenced via a resistor connected to a fixed voltage source (e.g. V_{REF}). The voltage generated at the resistor is in proportion to the deviation from the nominal input frequency and can be applied for retuning purposes.
7	Reference voltage should be RF decoupled to pin 1. The AFC resistor and the potentiometer for the limiter threshold are referenced to V_{REF}.
8/9	Demodulator tank circuit driven via two integrated capacitors (approx. 40 pF ± 25%). The circuit voltage should be approx. 200 mV (peak-to-peak)
10	Field strength output supplies a DC voltage proportional to the input level, which quickly adjusts to changes in the input voltage
11	Identification output designed as an open NPN collector output, which connects an additional time constant in parallel to pin 2 during multipath interference, or activates another circuit to suppress variable interference.
12	Demodulator time constant determines the response and hold time of the identification circuit.
13	Supply voltage to be RF decoupled to pin 1
14	Identification input high impedance input ($R_i \sim 10$ kΩ). This input receives variable interference forwarded on the field strength voltage via a high-pass filter.
15	Input for setting limiter threshold with a potential between V_{REF} and 0 V, the limiter threshold can be varied by approx. 44 dB.
16/17	Operating point feedback to be RF decoupled. For efficient push-push suppression, pin 16 should be blocked against pin 17 and latter to ground (pin 1).
18	IF input: frequency modulated IF voltage is injected at pin 18.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ground	V_1	0	V
MUTE input	V_2	V_S	V
Muting depth	V_3	V_7	V
AF output	V_4	V_S	V
Search tuning stop signal output	I_5	5	mA
AFC output	V_6	V_S	V
Reference voltage output	I_7	5	mA
Phase shift	V_8	V_S	V
Phase shift	V_9	V_S	V
Field strength	I_{10}	5	mA
Identification output	I_{11}	5	mA
Demodulator time constant	I_{12}	1	mA
Supply voltage	V_S	18	V
Identification input	V_{14}	V_7	V
Limiter threshold	V_{15}	V_7	V
Operating point feedback	$V_{16,17}$	V_7	V
IF input	V_{18}	V_7	V
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	– 55 to 125	°C

Operating Range

Supply voltage	V_S	7.5 to 15	V
IF section demodulator	f_{IF}	0.4 to 15	MHz
Overall frequency	f	0.4 to 15	MHz
AF (V_{QAF} = 1 dB)	f_{AF}	0.02 to 150	kHz
Ambient temperature	T_A	– 25 to 85	°C

Characteristics

V_S = 8.5 V; $V_{I\,IF\,rms}$ = 10 mV; $f_{I\,IF}$ = 10.7 MHz; Δf = ± 75 kHz; f_{mod} = 1 kHz; Q_B ≈ 20; T_A = 25 °C; adjustment when I_7 = 0; test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_{13}		27	33	mA	
Field strength output voltage	V_{10} V_{10}	3.0	3.8 0	 0.1	V V	$V_{I\,IF\,rms}$ = 50 mV $V_{I\,IF\,rms}$ = 0 V
AF output voltage	$V_{Q\,4\,rms}$	270	380	520	mV	
Total harmonic distortion during FM IF mode	THD		0.7	1.5	%	I_{AFC} = 0
Input voltage for limiter threshold	$V_{I\,IF\,rms}$		15	30	µV	$V_{Q\,4}$-3 dB
AM suppression	a_{AM}	60			dB	m = 30%
Signal-to-noise ratio	$a_{S/N}$	70			dB	
Current deviation of AFC output	ΔI_7		± 110		µA	$f = f_{IF}$ ± 50 kHz
AFC offset	Δf_{off}			± 15	kHz	V_I= 20 µV...10 mV
Search tuning stop window	Δf_{ST}		± 18		kHz	$R_{6\text{-}7}$ = 22 kΩ
Search tuning stop threshold FM	$V_{I\,ST}$			70	µV	$V_6 = V_{S/2}$
Search tuning stop threshold AM	$V_{I\,ST}$			500	µV	$V_6 = V_{S/2}$
Stabilized voltage	V_7	3.6	4.1	4.6	V	
Adjustable range of limiter threshold via pin 15	$V_{I\,IF}$		44		dB	V_{15} = 0; $V_{15} = V_{REF}$
AF MUTE	a_{AF} a_{AF}	3 31	7 39	11 47	dB dB	V_2 = 0; $R_{3\text{-}1} = \infty$ V_2 = 0; $R_{3\text{-}1}$ = 0
AF MUTE switch-off voltage	V_2		0.5	0.75	V	
MP sensitivity for full drive at pin 1	$V_{I\,14\,rms}$		5		mV	f = 20 kHz
Charge current pin 12	I_{12}		3		mA	pin 14 to ground
Discharge current pin 12	I_{12}		10		µA	pin 14 open, V_{12} < 1 V

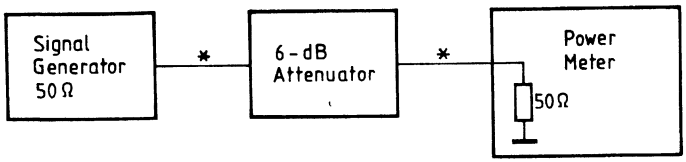
Additional Data with Respect to Application

(data does not apply to series measurement)

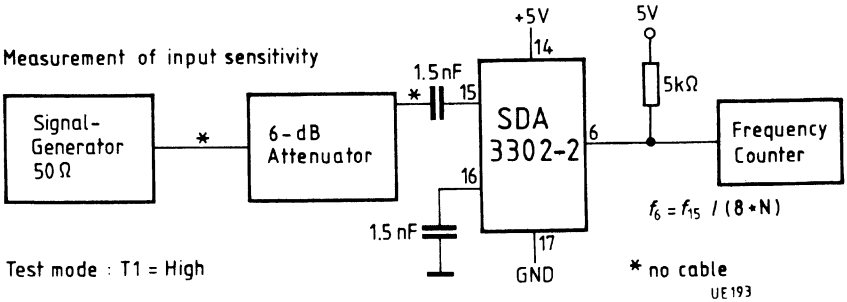
DC voltage AF output	$V_{Q\,5}$	2.8	3.8	4.8	V	
Internal DC current of emitter follower output	I_4	0.75	1		mA	
Input resistance for demodulator circuit	$R_{9\text{-}10}$	27	35		kΩ	
Search tuning stop "LOW	V_6			1.3	V	
Search tuning stop "HIGH"	V_6	7			V	

Measurement Circuit

Calibration of signal generator



Measurement of input sensitivity



SIEMENS

Audio Processor — TDA 4390

Preliminary Data — **Bipolar IC**

TDA 4390 is a complete stereo sound system controlled on an I^2C bus. The device comprises two function blocks:

1. Stereo Sound Processing
a) Four stereo AF inputs
b) Possibility for connecting equalizer, compander, noise rejection, etc
c) Maximum gain, adjustable to 0 dB or 6 dB
d) Treble/bass control
e) Two independent volume controls per channel (balance, fader)

2. Control Section
a) I^2C bus interface
b) Control of entire audio processing

Type	Ordering Code	Package
TDA 4390	Q67000-A8257	P-DIP-28

Circuit Description
Signal Section

In the signal section the sound signals are switched according to the sound sources that are required, these usually being VHF and AM stereo sound broadcasts, stereo tape and AUX (CD). The gain can be set to 0 dB or 6 dB. This section terminates in a stereo output to which other external circuits such as an equalizer, compander or noise-rejection systems can be connected.

In the continuation of the signal path there is a bass control with an increment of 2 dB over a setting range of +18/– 12 dB. The corner frequency for each channel is determined by an external capacitance. A steeper characteristic can be produced for the bass control with more elaborate external circuitry. The treble control, the corner frequency of which is also determined by an external capacitance, has an increment of 2 dB for a setting range of ±12 dB. The signal path is terminated by the volume control, which can be adjusted separately for left, right, front and back. 57 steps with an increment of 1.25 dB mean a setting range of 70 dB, the 57th increment activating the muting. Functions such as balance, fader or loudness are implemented by appropriate software in the tone or volume controls.

Control Section

All functions are controlled on an I²C bus interface. The currently valid data are stored in a latch block. The telegram structure is as follows:
Start condition – Chip address – Any number of data bytes – Stop condition

The following conditions apply to the data bytes:
Before the actual data byte (with the setting information) a subaddress byte which is interpreted by the I²C bus as a data byte however, must **always** be transmitted.

Example: the volume at back right is to be increased by several increments

Right	**Wrong**
Start condition	Start condition
Chip address 84 (hex)	Chip address 84 (hex)
Subaddress volume 03 (hex)	Subaddress volume 03 (hex)
Volume increment 8 08 (hex)	Volume increment 8 08 (hex)
Subaddress volume 03 (hex)	Volume increment 9 09 (hex)
Volume increment 9 09 (hex)	Volume increment 10 0A (hex)
Subaddress volume 03 (hex)	Stop condition
Volume increment 10 0A (hex)	

Different subaddresses can be accessed within a telegram (ie without renewing the start condition).

Chip Address

	MSB	.	.	.	.	.	.	LSB
	1	0	0	0	0	1	0	0
Altered from serial production to:	1	0	0	0	0	0	1	0

Subaddress Bytes

	MSB	.	.	.	.	.	.	LSB
Volume front left	X	X	X	X	X	0	0	0
Volume front right	X	X	X	X	X	0	0	1
Volume back left	X	X	X	X	X	0	1	0
Volume back right	X	X	X	X	X	0	1	1
Treble/bass	X	X	X	X	X	1	0	1
Switching byte	X	X	X	X	X	1	1	1

Setting Bytes

a) Volume loudspeakers left / right / front / back

	MSB	.	.	.	.	.	.	LSB
Maximum volume	X	X	1	1	1	1	1	1
Max. 1	X	X	1	1	1	1	1	0
Max. 16	X	X	1	1	0	0	0	0
Max. 55	X	X	0	0	1	0	0	0
MUTE	X	X	0	0	0	1	1	1
MUTE	X	X	0	0	0	0	0	0
MUTE	X	X	0	0	0	X	X	X
Power on	0	0	0	0	0	0	0	1

b) Treble / Bass

	MSB	.	.	.	.	.	.	LSB
Linear	1	0	0	0	1	0	0	1
Max. treble, lin. bass	0	0	1	0	1	0	0	1
Max. treble, lin. bass	0	0	0	X	1	0	0	1
Min. treble, lin. bass	1	1	1	0	1	0	0	1

If no signal input is activated, this is interpreted as muting. There is no mutual lockout of the inputs for multiple selections.

Lin. treble, min. bass	1	0	0	0	1	1	1	1
Max. treble, max. bass	0	0	0	X	0	0	0	0
Min. treble. min. bass	1	1	1	X	1	1	1	1

	MSB			LSB	MSB			LSB
	Treble			Treble	Bass			Bass

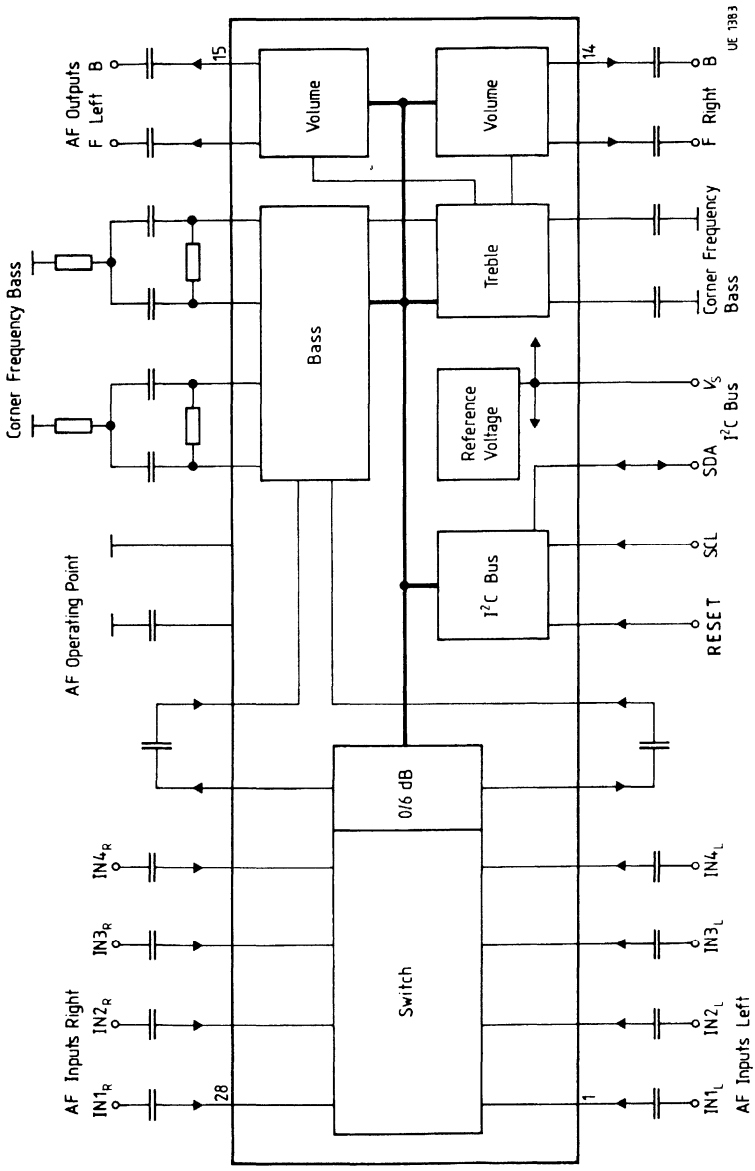
c) Switching byte

MSB							LSB
MUTE	IN1	IN2	IN3	IN4	Gain	X	X

MUTE = 0	All AF outputs on; power on
MUTE = 1	All AF outputs muted
IN1 = 0	IN1 stereo inputs inactive; power on
IN1 = 1	IN1 stereo inputs activated
IN2 = 0	IN2 stereo inputs inactive; power on
IN2 = 1	IN2 stereo inputs activated
IN3 = 0	IN3 stereo inputs inactive; power on
IN3 = 1	IN3 stereo inputs activated
IN4 = 0	IN4 stereo inputs inactive; power on
IN4 = 1	IN4 stereo inputs activated
Gain = 0	Gain of switch section 0 dB; power on
Gain = 1	Gain of switch section 6 dB

If no signal input is activated, this is interpreted as muting. There is no mutual lockout of the inputs for multiple selections.

Block Diagram



Pin Functions

Pin No.	Function
1	AF input 1 left
2	AF input 2 left
3	AF input 3 left
4	AF input 4 left
5	AF output switch section left
6	AF input control section left
7	Reset (all functions in power-on status); active high
8	I^2C bus SCL
9	I^2C bus SDA
10	$+V_S$ (supply voltage)
11	Corner frequency treble left
12	Corner frequency treble right
13	AF output right front
14	AF output right back
15	AF output left back
16	AF output left front
17	Corner frequency bass right; (network output)
18	Corner frequency bass right; (network input)
19	Corner frequency bass left; (network output)
20	Corner frequency bass left; (network input)
21	Ground
22	Blocking AF operating point
23	AF input control section right
24	AF output switch section right
25	AF input 4 right
26	AF input 3 right
27	AF input 2 right
28	AF input 1 right

Absolute Maximum Ratings

T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{10}	0	14	V
Max. DC voltage	V_1	0	V_{10}	V
Max. DC voltage	V_2	0	V_{10}	V
Max. DC voltage	V_3	0	V_{10}	V
Max. DC voltage	V_4	0	V_{10}	V
Max. DC voltage	V_6	0	V_{10}	V
Max. DC voltage	V_7	0	V_{10}	V
Max. DC voltage	V_8	0	V_{10}	V
Max. DC voltage	V_{11}	0	V_{10}	V
Max. DC voltage	V_{12}	0	V_{10}	V
Max. DC voltage	V_{18}	0	V_{10}	V
Max. DC voltage	V_{20}	0	V_{10}	V
Max. DC voltage	V_{22}	0	V_{10}	V
Max. DC voltage	V_{23}	0	V_{10}	V
Max. DC voltage	V_{25}	0	V_{10}	V
Max. DC voltage	V_{26}	0	V_{10}	V
Max. DC voltage	V_{27}	0	V_{10}	V
Max. DC voltage	V_{28}	0	V_{10}	V
Max. DC current	I_5	0	2	mA
Max. DC current	I_9	0	2	mA
Max. DC current	I_{13}	0	2	mA
Max. DC current	I_{14}	0	2	mA
Max. DC current	I_{15}	0	2	mA
Max. DC current	I_{16}	0	2	mA
Max. DC current	I_{17}	0	2	mA
Max. DC current	I_{19}	0	2	mA
Max. DC current	I_{24}	0	2	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		53	K/W

Operating Range

Supply voltage	V_S	7.5	13.2	V
Ambient temperature	T_A	– 40	85	°C
Input-frequency range	f_1	0.01	20	kHz

Characteristics
V_S = 10 V; T_A = 25 °C
AF reference level 0 dB = 150 mV rms unless stated otherwise

I²C bus
preset: Start-84(82)-00, 3F-01, 3F-02, 3F-03, 3F-05, 89-07, 40-Stop
Chip addr.-Vol63-Vol63-Vol63-Vol63-Tone lin-IN1
Basic setting for each specification item is always preset. Only settings that differ are stated under test conditions. *Italics* are only for explanation of hex codes, with switching bits only, set bits or functions are stated.

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Current consumption	I_{10}		35		mA		1
Signal Section							
Gain	$G_{5\text{-}1}$	– 1	0	1	dB		1
Gain	$G_{24\text{-}28}$	– 1	0	1	dB		1
Gain	$G_{5\text{-}1}$	5	6	7	dB	07,44; *gain=6 dB*	1
Gain	$G_{24\text{-}28}$	5	6	7	dB	07,44; *gain=6 dB*	1
Analog values apply for feeding in on pins 2-4 and 25-27							
Max. gain	$G_{15\text{-}6}$	– 2	0	2	dB		1
Max. gain	$G_{16\text{-}6}$	– 2	0	2	dB		1
Max. gain	$G_{13\text{-}23}$	– 2	0	2	dB		1
Max. gain	$G_{14\text{-}23}$	– 2	0	2	dB		1
Min. gain	$G_{15\text{-}6}$		-70		dB	00,08 – 02,08 *vol 8*	1
Min. gain	$G_{16\text{-}6}$		-70		dB	00,08 – 02,08 *vol 8*	1
Min. gain	$G_{13\text{-}23}$		-70		dB	01,08 – 03,08 *vol 8*	1
Min. gain	$G_{14\text{-}23}$		-70		dB	01,08 – 03,08 *vol 8*	1
Wow & flutter	$\Delta G_{13\text{-}14}$			± 2	dB	01,3F – 01,24 03,3F – 03,24 *vol 63-66*	1
Wow & flutter	$\Delta G_{15\text{-}16}$			± 2	dB	00,3F – 00,24 02,3F – 02,24 *vo l63-66*	1
Wow & flutter	$\Delta G_{13\text{-}16}$			± 2	dB	00,3F – 00,24 01,3F – 01,24 *vol 63-66*	1
Wow & flutter	$\Delta G_{14\text{-}15}$			± 2	dB	02,3F – 02,24 03,3F – 03,24 *vol 63-66*	1

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Increment vol 13	ΔG_{13}	0	1.25	2.5	dB	01,X – 01, (X ± 1) *vol X – vol (X ± 1)*	1
Increment vol 14	ΔG_{14}	0	1.25	2.5	dB	03,X – 03, (X ± 1) *vol X – vol (X ± 1)*	1
Increment vol 15	ΔG_{15}	0	1.25	2.5	dB	02,X – 02, (X ± 1) *vol$_{KH}$X -vol$_{KH}$ (X ± 1)*	1
Increment vol 16	ΔG_{16}	0	1.25	2.5	dB	00,X – 00, (X ± 1) *vol X – vol (X ± 1)*	1
Bass emphasis	$G_{15\text{-}6}$	16	18		dB	05,80; f_1 = 40 Hz *bass max, treble lin*	1
Bass emphasis	$G_{16\text{-}6}$	16	18		dB	05,80; f_1 = 40 Hz *bass max, treble lin*	1
Bass emphasis	$G_{13\text{-}23}$	16	18		dB	05,80; f_1 = 40 Hz *bass max, treble lin*	1
Bass emphasis	$G_{14\text{-}23}$	16	18		dB	05,80; f_1 = 40 Hz *bass max, treble lin*	1
Bass deemphasis	$G_{15\text{-}6}$		– 12		dB	05,8F; f_1 = 40 Hz *bass min, treble lin*	1
Bass deemphasis	$G_{16\text{-}6}$		– 12		dB	05,8F; f_1 = 40 Hz *bass min, treble lin*	1
Bass deemphasis	$G_{13\text{-}23}$		– 12		dB	05,8F; f_1 = 40 Hz *bass min, treble lin*	1
Bass deemphasis	$G_{14\text{-}23}$		– 12		dB	05,8F; f_1 = 40 Hz *bass min, treble lin*	1
Bass increment	ΔG_{13}	1	2	3	dB	05,8X – 05,8 (X ± 1) *bass X – bass (X ± 1)*	1
Bass increment	ΔG_{14}	1	2	3	dB	05,8X – 05,8 (X ± 1) *bass X – bass (X ± 1)*	1
Bass increment	ΔG_{15}	1	2	3	dB	05,8X – 05,8 (X ± 1) *bass X – bass (X ± 1)*	1
Bass increment	ΔG_{16}	1	2	3	dB	05,8X – 05,8 (X ± 1) *bass X – bass (X ± 1)*	1
Treble emphasis	$G_{15\text{-}6}$	10	12		dB	05,09; f_1 = 15 kHz *treble max, bass lin*	1
Treble emphasis	$G_{16\text{-}6}$	10	12		dB	05,09; f_1 = 15 kHz *treble max, bass lin*	1
Treble emphasis	$G_{13\text{-}23}$	10	12		dB	05,09; f_1 = 15 kHz *treble max, bass lin*	1
Treble emphasis	$G_{14\text{-}23}$	10	12		dB	05,09; f_1 = 15 kHz *treble max, bass lin*	1
Treble deemphasis	$G_{15\text{-}6}$		– 12		dB	05,F9; f_1 = 15 kHz *treble min, bass lin*	1
Treble deemphasis	$G_{16\text{-}6}$		– 12		dB	05,F9; f_1 = 15 kHz *treble min, bass lin*	1
Treble deemphasis	$G_{13\text{-}23}$		– 12		dB	05,F9; f_1 = 15 kHz *treble min, bass lin*	1
Treble deemphasis	$G_{14\text{-}23}$		– 12		dB	05,F9; f_1 = 15 kHz *treble min, bass lin*	1

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Treble increment	ΔG_{13}	1	2	3	dB	05,X9 – 05, (X ± 1) 9 *treble X – treble (X ± 1)*	1
Treble increment	ΔG_{14}	1	2	3	dB	05,X9 – 05, (X ± 1) 9 *treble X – treble (X ± 1)*	1
Treble increment	ΔG_{15}	1	2	3	dB	05,X9 – 05, (X ± 1) 9 *treble X – treble (X ± 1)*	1
Treble increment	ΔG_{16}	1	2	3	dB	05,X9 – 05, (X ± 1) 9 *treble X – treble (X ± 1)*	1
Tone linearity	ΔG_{13}			± 2	dB	05,89; f_1 = 40 Hz – 15 kHz *treble, bass lin*	1
Tone linearity	ΔG_{14}			± 2	dB	05,89; f_1 = 40 Hz – 15 kHz *treble, bass lin*	1
Tone linearity	ΔG_{15}			± 2	dB	05,89; f_1 = 40 Hz – 15 kHz *treble, bass lin*	1
Tone linearity	ΔG_{16}			± 2	dB	05,89; f_1 = 40 Hz – 15 kHz *treble, bass lin*	1
Channel separation	$\Delta G_{14\text{-}15}$	60			dB	V_6 or V_{23} = 300 mV rms	1
Channel separation	$\Delta G_{13\text{-}16}$	60			dB	V_6 or V_{23} = 300 mV rms	1
Crosstalk attenuation switch	a input dist / output wanted	80			dB	$V_{1/\text{wanted}}$ = 0 $V_{1/\text{dist}}$ = 300 mV rms	1

Feed in on pins 1-4 and 25-28, measure on pins 5 and 24

Attenuation in muting	$a_{1\text{-}5}$	80			dB	01,00 – 03,00 *vol0*; V_1 = 300 mV rms	1
Attenuation in muting	$a_{1\text{-}5}$	80			dB	07,C0; V_1=300 mV rms MUTE *active*	1
Attenuation in muting	$a_{1\text{-}5}$	80			dB	07,00; V_1 = 300 mV rms *notselect*	1

Analog values apply for feeding in on pins 2, 3, 4

Attenuation in muting	$a_{28\text{-}24}$	80			dB	00,00 – 03,00 *vol0*; V_{28} = 300 mV rms	1
Attenuation in muting	$a_{28\text{-}24}$	80			dB	07,C0; V_{28} = 300 mV rms MUTE *active*	1
Attenuation in muting	$a_{28\text{-}24}$	80			dB	07,00; V_{28} = 300 mV rms *not select*	1

Analog values apply for feeding in on pins 25, 26, 27

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Max. input voltage	V_1	1500			mV_{rms}	THD_5 = 1%	1
Max. input voltage	V_1	750			mV_{rms}	THD_5 = 1%; 07,44	1
Analogous values apply for feeding in on pins 2, 3, 4							
Max. input voltage	V_{28}	1500			mV_{rms}	THD_{24} = 1%	1
Max. input voltage	V_{28}	750			mV_{rms}	THD_{24} = 1%; 07,44	1
Analog values apply for feeding in on pins 25, 26, 27							
Max. input voltage	V_6	300			mV_{rms}	$THD_{15,16}$ < 1% 05,XX *random tone*	1
Max. input voltage	V_{23}	300			mV_{rms}	$THD_{13,14}$ < 1% 05,XX *random tone*	1
Max. output voltage	V_{13}	2.4			V_{rms}	THD_{13} < 1%	1
Max. output voltage	V_{14}	2.4			V_{rms}	THD_{14} < 1%	1
Max. output voltage	V_{15}	2.4			V_{rms}	THD_{15} < 1%	1
Max. output voltage	V_{16}	2.4			V_{rms}	THD_{16} < 1%	1
Distortion factor	THD_5		0.01	0.05	%	V_1 = 150 mV_{rms}	1
Distortion factor	THD_{24}		0.01	0.05	%	V_{28} = 150mV_{rms}	1
Analog values apply for feeding in on pins 2-4 and 25-27							
Distortion factor	THD_{13}		0.01	0.05	%	V_{28} = 150 mV_{rms}	2
Distortion factor	THD_{14}		0.01	0.05	%	V_{28} = 150 mV_{rms}	2
Distortion factor	THD_{15}		0.01	0.05	%	V_1 = 150 mV_{rms}	2
Distortion factor	THD_{16}		0.01	0.05	%	V_1 = 150 mV_{rms}	2
Analog values apply for feeding in on pins 2-4 and 25-27							
Distortion factor	THD_{13}		0.01	0.1	%	V_{28} = 150 mV_{rms} 01,2F; *vol 47*	2
Distortion factor	THD_{14}		0.01	0.1	%	V_{28}=150 mV_{rms}	2
Distortion factor	THD_{15}		0.01	0.1	%	03,2F; *vol 47* V_1 = 150 mV_{rms}	2
Distortion factor	THD_{16}		0.01	0.1	%	02,2F; *vol 47* V_1 = 150 mV_{rms}	2
Analog values apply for feeding in on pins 2-4 and 25-27							
Distortion factor	THD_{13}		0.05	0.2	%	V_{28} = 150 mV_{rms}; 05,XX *random tone*	1
Distortion factor	THD_{14}		0.05	0.2	%	V_{28} = 150 mV_{rms}; 05,XX *random tone*	1
Distortion factor	THD_{15}		0.05	0.2	%	V_1 = 150 mV_{rms}; 05,XX *random tone*	1
Distortion factor	THD_{16}		0.05	0.2	%	V_1 = 150 mV_{rms}; 05,XX *random tone*	1
Analog values apply for feeding in on pins 2-4 and 25-27							

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Unweighted signal/ noise ratio	$a_{S/N\,13}$	90	95		dB	$V_{N\,rms\,20\,Hz-20\,kHz}$ $V_{28} = 0.3V_{rms}$	2
Unweighted signal/ noise ratio	$a_{S/N\,14}$	90	95		dB	$V_{N\,rms\,20\,Hz-20\,kHz}$ $V_{28} = 0.3V_{rms}$	2
Unweighted signal/ noise ratio	$a_{S/N\,15}$	90	95		dB	$V_{N\,rms\,20\,Hz-20\,kHz}$ $V_1 = 0.3V_{rms}$	2
Unweighted signal/ noise ratio	$a_{S/N\,16}$	90	95		dB	$V_{N\,rms\,20\,Hz-20\,kHz}$ $V_1 = 0.3V_{rms}$	2

Analog values apply for feeding in on pins 2-4 and 25-27

Unweighted signal/ noise ratio	$a_{S/N\,13}$	70	80		dB	$V_{N\,rms\,20\,Hz-20\,kHz}$; $V_{28} = 0.3V_{rms}$ 01,27; *vol 39*	2
Unweighted signal/ noise ratio	$a_{S/N\,14}$	70	80		dB	$V_{N\,rms\,20\,Hz-20\,kHz}$ $V_{28} = 0.3V_{rms}$ 03,27; *vol 39*	2
Unweighted signal/ noise ratio	$a_{S/N\,15}$	70	80		dB	$V_{N\,rms\,20\,Hz-20\,kHz}$ $V_1 = 0.3V_{rms}$ 02,27	2
Unweighted signal/ noise ratio	$a_{S/N\,16}$	70	80		dB	$V_{N\,rms\,20\,Hz-20\,kHz}$ $V_1 = 0.3V_{rms}$ 00,27; *vol 39*	2

Analog values apply for feeding in on pins 2-4 and 25-27

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Unweighted noise voltage	$V_{N\,13}$		2	10	μV_{rms}	$V_{N\,rms}$ 20 Hz – 20 kHz 01,00 – 03,00 *vol 0*	2
Unweighted noise voltage	$V_{N\,14}$		2	10	μV_{rms}	$V_{N\,rms}$ 20 Hz – 20 kHz 01,00 – ,00 *vol 0*	2
Unweighted noise voltage	$V_{N\,15}$		2	10	μV_{rms}	$V_{N\,rms}$ 20 Hz – 20 kHz 00,00 – 02,00 *vol 0*	2
Unweighted noise voltage	$V_{N\,16}$		2	10	μV_{rms}	$V_{N\,rms}$ 20 Hz – 20 kHz 00,00 – 02,00 *vol 0*	2
DC jump Δ1 bit	ΔV_{13}			± 10	mV	01,X – 01, X ± 1 *vol X – vol (X ± 1)*	1
DC jump Δ1 bit	ΔV_{14}			± 10	mV	03,X – 03, X ± 1 *vol X – vol (X ± 1)*	1
DC jump Δ1 bit	ΔV_{15}			± 10	mV	02,X – 02, X ± 1 *vol X – vol (X ± 1)*	1
DC jump Δ1 bit	ΔV_{16}			± 10	mV	00,X – 00, X ± 1 *vol X – vol (X ± 1)*	1
DC jump Δ1 bit	ΔV_{13}			± 10	mV	05,X – 05, X ± 1 *tone X– tone (X ± 1)*	1
DC jump Δ1 bit	ΔV_{14}			± 10	mV	05,X – 05, X ± 1 *tone X– tone (X ± 1)*	1
DC jump Δ1 bit	ΔV_{15}			± 10	mV	05,X – 05, X ± 1 *tone X– tone (X ± 1)*	1
DC jump Δ1 bit	ΔV_{16}			± 10	mV	05,X – 05, X ± 1 *tone X– tone (X ± 1)*	1

Characteristics (cont'd)

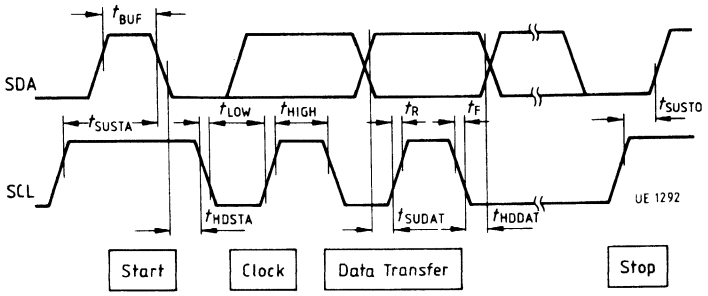
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Design Notes							
Input resistance	R_1	30			kΩ		
Input resistance	R_2	30			kΩ		
Input resistance	R_3	30			kΩ		
Input resistance	R_4	30			kΩ		
Input resistance	R_6	30			kΩ		
Input resistance	R_{23}	30			kΩ		
Input resistance	R_{25}	30			kΩ		
Input resistance	R_{26}	30			kΩ		
Input resistance	R_{27}	30			kΩ		
Input resistance	R_{28}	30			kΩ		
Output resistance	R_5			200	Ω		
Output resistance	R_{13}			200	Ω		
Output resistance	R_{14}			200	Ω		
Output resistance	R_{15}			200	Ω		
Output resistance	R_{16}			200	Ω		
Output resistance	R_{24}			200	Ω		
V_S = 8.5 V:							
Max. input voltage	V_6	200			mV_{rms}	$THD_{15,16} < 1\%$	1
Max. input voltage	V_{23}	200			mV_{rms}	05,XX *random tone* $THD_{13,14} < 1\%$	1
V_S = 12 V:							
Max. input voltage	V_6	400			mV_{rms}	$THD_{15,16} < 1\%$	1
Max. input voltage	V_{23}	400			mV_{rms}	05,XX *random tone* $THD_{13,14} < 1\%$	1

Characteristics (cont'd)

V_S = 10 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
I²C Bus (SCL, SDA)					
Edges SCL, SDA					
Rise time	t_r			1	µs
Fall time	t_f			300	ns
Shift Clock SCL					
Frequency	f_{SCL}	0		100	kHz
H-pulse width	t_H	4			µs
L-pulse width	t_L	4			µs
Start					
Setup time	t_{SUSTA}	4			µs
Hold time	t_{HDSTA}	4			µs
Stop					
Setup time	t_{SUSTO}	4			µs
Bus release	t_{BUR}	4			µs
Data Change					
Setup time	t_{SUDAT}	1			µs
Hold time	t_{HDDAT}	1			µs
Inputs SCL, SDA					
Input voltage	V_{IH}	2.4		5.5	V
	V_{IL}			1	V
Input current	I_{IH}			50	µA
	I_{IL}			100	µA
Output SDA (open-collector)					
Output voltage	V_{QH}	5.4			V
R_L=2.5 kΩ	V_{QL}			0.4	V
I_{QL}=3 mA					
Reset					
Reset inactive	V_{QRSL}	0.3		1	V
Reset active	V_{QRSH}	2.4		5.5	V
or pin open					

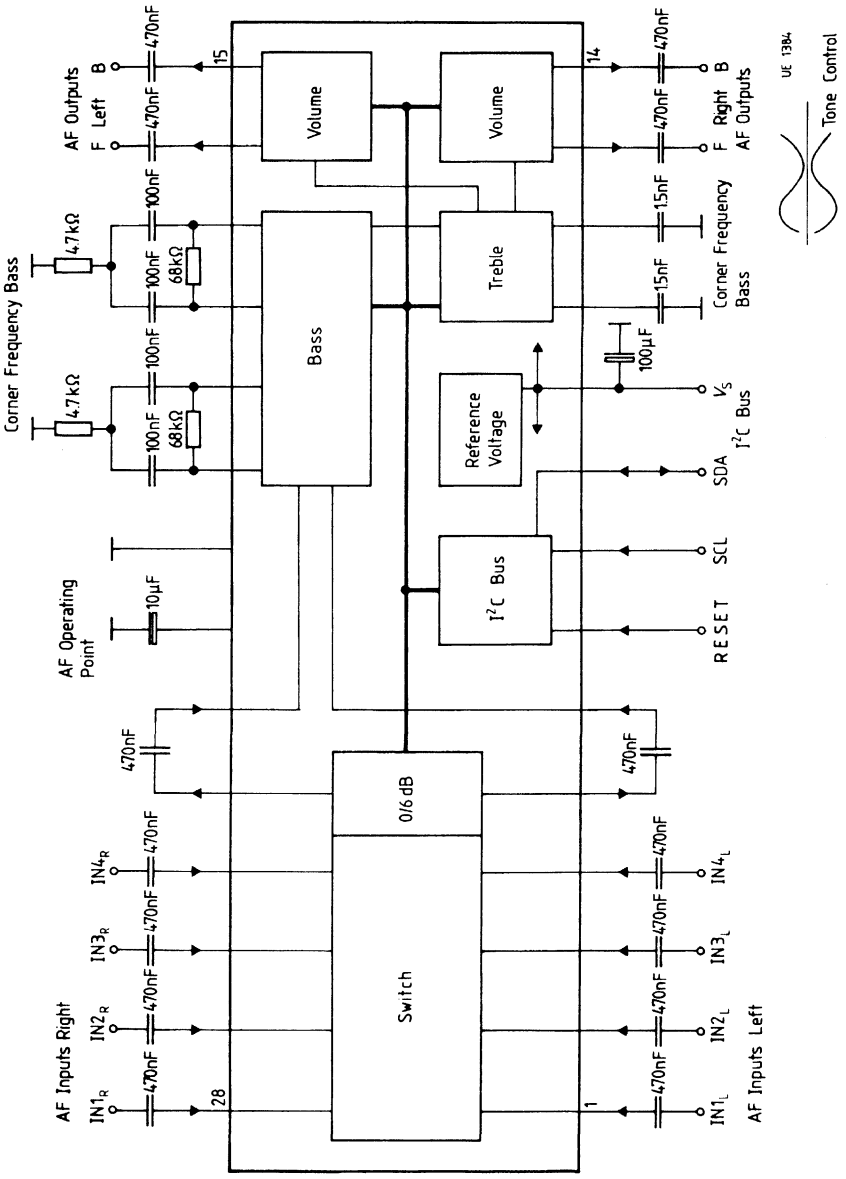
I²C Bus Time Diagram



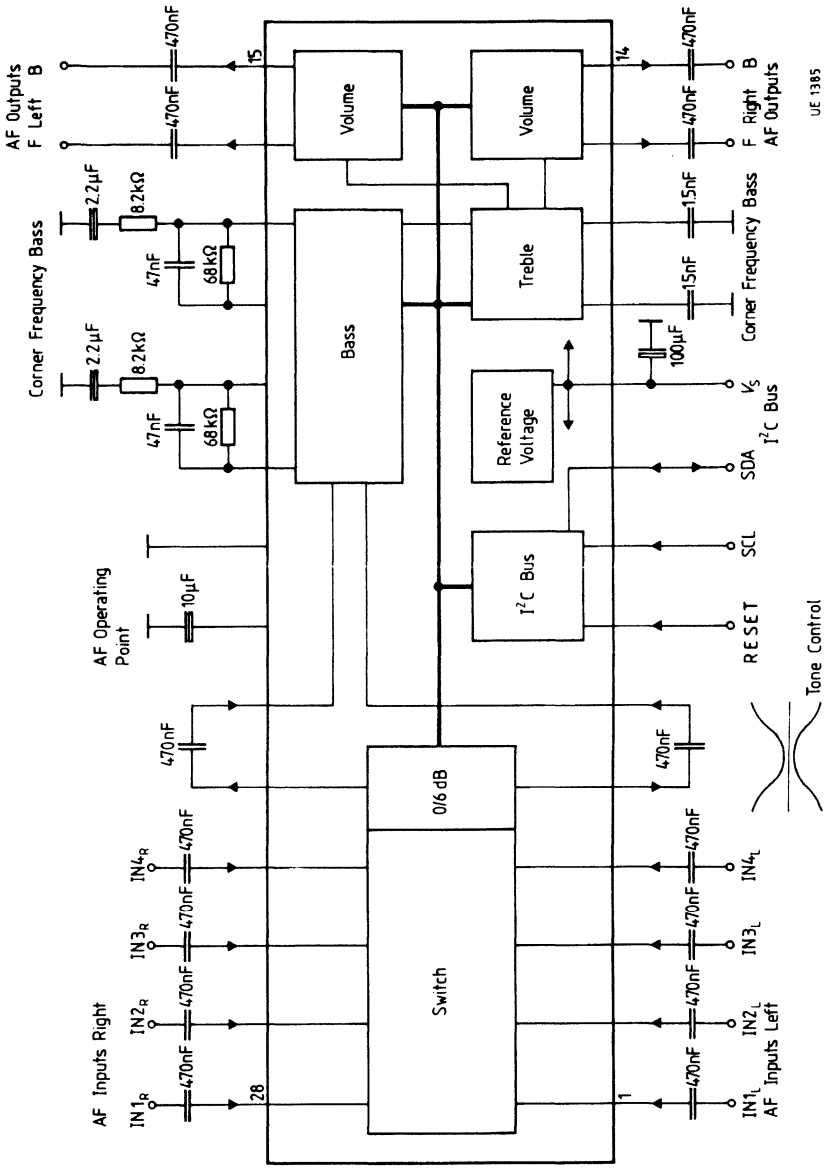
t_{SUSTA}	Set-up time (start)
t_{HDSTA}	Hold time (start)
t_{HIGH}	Pulse width (clock)
t_{LOW}	Pulse width (clock)
t_{SUDAT}	Set-up time (data transfer)
t_{HDDAT}	Hold time (data transfer)
t_{SUSTO}	Set-up time (stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

The listed times are referenced to the V_{IH} and V_{IL} values.

Application Circuit 1



Application Circuit 2



SIEMENS

Control ICs for Switched-Mode Power Supplies

TDA 4601

Bipolar IC

Features

- Direct control of the switching transistor
- Low start-up current
- Reversing linear overload characteristic
- Base current drive proportional to collector current
- Protective circuit in case of disturbance

Type	Ordering Code	Package
TDA 4601	Q67000-A2379	P-SIP-9
TDA 4601-D	Q67000-A2390	P-DIP-18 L9 (pin 6 and pins 10 to 18 grounded)

The integrated circuit TDA 4601/D is designed for driving, controlling and protecting the switching transistor in self-oscillating flyback converter power supplies as well as for protecting the overall power supply unit. In case of disturbance, the rise of the secondary voltage is prevented. In addition to the ICs application range including TV receivers, video tape recorders, hifi devices and active loudspeakers, it can also be used in power supply units for professional applications due to its wide control range and high voltage stability during increased load changes.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_9	0	20	V
Voltages				
Reference output	V_1	0	6	V
Zero passage identification	V_2	– 0.6	0.6	V
Control amplifier	V_3	0	3	V
Collector current simulation	V_4	0	8	V
Blocking input	V_5	0	8	V
Base current cut-off point	V_7	0	V_9	V
Base current amplifier output	V_8	0	V_9	V
Currents				
Zero passage identification	I_{I2}	– 5	5	mA
Control amplifier	I_{I3}	– 3	3	mA
Collector current simulation	I_{I4}	0	5	mA
Blocking input	I_{I5}	0	5	mA
Base current cut-off point	I_{Q7}	– 1	1.5	A
Base current amplifier output	I_{Q8}	– 1.5	0	A
Junction temperature	T_j		125	°C
Storage temperature range	T_{stg}	– 40	125	°C
Thermal resistances:				
system-air TDA 4601	$R_{th\,SA}$		70	K/W
system-case TDA 4601	$R_{th\,SC}$		15	K/W
system-air[1] TDA 4601 D	$R_{th\,SA}$		60	K/W
system-air[2] TDA 4601 D	$R_{th\,SA1}$		44	K/W
Operating Range				
Supply voltage	V_9	7.8	18	V
Case temperature TDA 4601	T_C	0	85	°C
Ambient temperature range[3] TDA 4601 D	T_A	0	70	°C

[1]) Case soldered on PC board without cooling surface
[2]) Case soldered on PC board with copper-clad 35 µm layer, cooling surface 25 cm²
[3]) $R_{th\,SA1}$ = 44 K/W and P_V = 1 W

Characteristics

T_A = 25 °C
according to measurement circuit 1 and diagram

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Start Operation					
Current consumption (V_1 not yet switched on)					
V_9 = 2 V	I_9			0.5	mA
V_9 = 5 V	I_9		1.5	2.0	mA
V_9 = 10 V	I_9		2.4	3.2	mA
Switching point for V_1	V_9	11.0	11.8	12.3	V
Normal Operation					
V_9 = 10 V; V_{cont} = -10 V; V_{clock} = ± 0.5 V; f = 20 kHz; duty cycle 1:2 after switch-on					
Current consumption					
V_{cont} = -10 V	I_9	110	135	160	mA
V_{cont} = 0 V	I_9	50	75	100	mA
Reference voltage					
I_1 < 0.1 mA	V_1	4.0	4.2	4.5	V
I_1 = 5 mA	V_1	4.0	4.2	4.4	V
Temperature coefficient of reference voltage	TC_1		10^{-3}		1/K
Control voltage V_{cont} = 0 V	V_3	2.3	2.6	2.9	V
Collector current simulation voltage					
V_{cont} = 0 V	V_4*)	1.8	2.2	2.5	V
V_{cont} = 0 V/– 10 V	ΔV_4*)	0.3	0.4	0.5	V
Clamping voltage	V_5	6.0	7.0	8.0	V
Output voltages					
V_{cont} = 0 V	V_{Q7}*)	2.7	3.3	4.0	V
V_{cont} = 0 V	V_{Q8}*)	2.7	3.4	4.0	V
V_{cont} = 0 V/– 10 V	ΔV_{Q8}	1.6	2.0	2.4	V
Feedback voltage	V_2*)		0.2		V

*) DC component only

Protective Operation
V_9 = 10 V; V_{cont} = – 10 V; V_{clock} = ± 0.5 V; f = 20 kHz;
duty cycle 1:2

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption V_5 < 1.9 V	I_9	14	22	28	mA
Switch-off voltage V_5 < 1.9 V	V_{Q7}	1.3	1.5	1.8	V
Switch-off voltage V_5 < 1.9 V	V_4	1.8	2.1	2.5	V
Blocking input Blocking voltage V_{cont} = 0 V	V_5	$\frac{V_1}{2} - 0.1$	$\frac{V_1}{2}$		V
Supply voltage blocked for V_8 V_{cont} = 0 V	V_9	6.7	7.4	7.8	V
V_1 off (with further reduction of V_9)	ΔV_9	0.3	0.6	1.0	V

Characteristics
T_A = 25 °C; according to measurement circuit 2

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Switching time (secondary voltage)	t_{on}		350	450	ms
Voltage variation S3 = closed ΔN_3 = 20 W	$\Delta V_{2\,sec}$		100	500	mV
Voltage deviation S2 = closed ΔN_2 = 15 W	$\Delta V_{2\,sec}$		500	1000	mV
Standby operation S_1 = open secondary useful load = 3 W	ΔV_{2sec} f	 70	20 75	30	V kHz

The cooling conditions have to be optimized with regard to maximum ratings (T_A; T_j; $R_{th\,JC}$; $R_{th\,SA}$).

Circuit Description

The TDA 4601 is designed for driving, controlling and protecting the switching transistor in flyback converter power supplies during start-up, normal and overload operations as well as during disturbed operation. In case of disturbance the drive of the switching transistor is inhibited and a secondary voltage rise is prevented.

I. Start-Up

The start-up procedures (on-mode) include three consecutive operating phases as follows:

1. **Build-Up of Internal Reference Voltage**

   The internal reference voltage supplies the voltage regulator and effects charging of the coupling electrolytic capacitor connected to the switching transistor. Current consumption will remain at $I_9 < 3.2$ mA with a supply voltage up to V_9 approx. 12 V.

2. **Enabling of Internal Voltage - Reference Voltage V_1 = 4 V**

   Simultaneously with V_9 reaching approx. 12 V, an internal voltage becomes available, providing all component elements, with the exception of the control logic, with a thermally stable and overload-resistant current supply.

3. **Enabling of Control Logic**

   In conjunction with the generation of the reference voltage, the current supply for the control logic is activated by means of an additional stabilization circuit. The integrated circuit is then ready for operation.

The start-up phase above described are necessary for ensuring the charging of the coupling electrolytic capacitor, which in turn supplies the switching transistor. Only then is it possible to ensure that the transistor switches accurately.

II. Normal Operating Mode / Control Operating Mode

At the input of pin 2 the zero passages of the frequency provided by the feedback coil are registered and forwarded to the control logic. Pin 3 (control input, overload and standby identification) receives the rectified amplitude fluctuations of the feedback coil. The control amplifier operates with an input voltage of approx. 2 V and a current of approx. 1.4 mA. Depending on the internal voltage reference, the overload identification limits inconjunction with collector current simulator pin 4 the operating

range of the control amplifier. The collector current is simulated by an external RC combination present at pin 4 and internally set threshold voltages. The largest possible collector current applicable to the switching transistor (point of return) increases in proportion to the increased capacitance (10 nF). Thus the required operating range of the control amplifier is established. The range of control lies between a DC voltage clamped at 2 V and a sawtooth - shaped rising AC voltage, which can vary up to a max. amplitude of 4 V (reference voltage). During secondary load reduction to approx. 20 W, the switching frequency is increased (approx. 50 kHz) at an almost constant pulse duty factor (1:3). During additional secondary load decreases to approx. 1 W, the switching frequency increases to approx. 70 kHz and pulse duty factor to approx. 1:11. At the same time collector peak current is reduced to < 1 A.

The output levels of the control amplifier as well as those of the overload identification and collector current simulator are compared in the trigger and forwarded to the control logic. Via pin 5 it is possible to externally inhibit the operations of the IC. The output at pin

pin 8 will be inhibited when voltages of $\leq \frac{V_{REF}}{2} - 0.1$ V are present pin at 5.

Flipflops for controlling the base current amplifier and the base current shut-down are set in the control logic depending on the start-up circuit, the zero passage identification as well as on the enabling by the trigger. The base current amplifier forwards the sawtooth-spahed V_4 voltage to the output of pin 8. A current feedback with an external resistor (R = 0.68 Ω) is present between pin 8 and pin 7. The applied value of the resistor determines the max. amplitude of the base driving current for the switching transistor.

III. Protective Operating Mode

The base current shut-down activated by the control logic clamps the output of pin 7 to 1.6 V. As a result, the drive of the switching transistor is inhibited. This protective measure is enabled if the supply voltage at pin 9 reaches a value ≤ 6.7 V or if voltages of

$\leq \frac{V_{REF}}{2} - 0.1$ V are present at pin 5.

In case of short-circuits occurring in the secondary windings of the switched-mode power supply, the integrated circuit continuously monitors the fault conditions. During secondary, completely load-free operation only a small pulse duty factor is set. As a result the total power consumption of the power supply is held at N = 6...10 W during both operating modes. After the output has been inhibited for a voltage supply of ≤ 6.7 V, the reference voltage (4 V) is switched off if the voltage supply is further reduced by ΔV_9 = 0.6 V.

Protective Operating Mode at Pin 5 in Case of Disturbance

The protection against disturbances such as primary undervoltages and/or secondary over- voltages (e.g. by changes in the component parameters for the switched-mode power supply) is realized as follows:

Protective Operating Mode with Continuous Fault Condition Monitoring

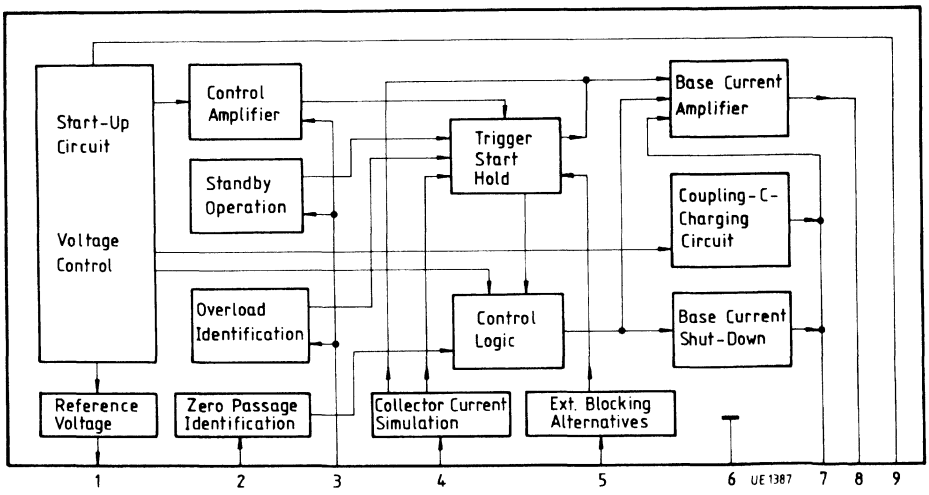
In case of disturbance the output pulses at pin 8 are inhibited by falling below the protective threshold V_5, with a typical value of $V_1/2$. As a result current consumption is reduced ($I_9 \geq 14$ mA at $V_9 = 10$ V).

With a corresponding **high-impedance** start-up resistor*), supply voltage V_9 will fall below the minimum shut-down threshold (5.7 V) for reference voltage V_1. V_1 will be switched off and current consumption is further reduced to $I_9 \leq 3.2$ mA at $V_9 \leq 10$ V.

Because of these reductions in current consumption, the supply voltage can rise again to reach the switch-on threshold of $V_9 \geq 12.3$ V. The protective threshold at pin 5 is released and the power supply is again ready for operation.

In case of continuing problems of disturbance ($V_5 \leq V_1/2$ -0.1 V) the switch-on mode is interrupted by the periodic protective operating mode described above, i.e. pin 8 is inhibited and V_9 is falling, etc.

Block Diagram



*) in application circuit 1 10 kΩ/3 W

IV. Switch-On in the Wide Range Power Supply (90 Vac to 270 Vac)
(application circuit 2)

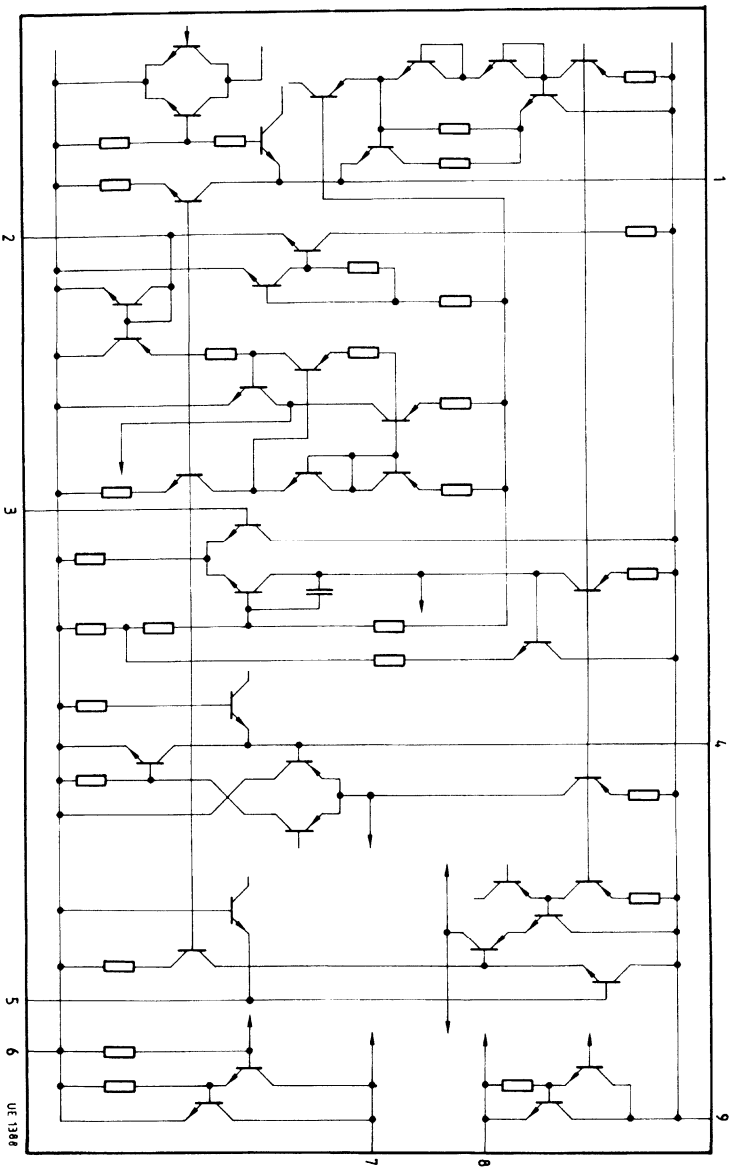
Self-oscillating flyback-converters designed as wide range power supplies require a power source independent of the rectified line voltage for TDA 4601. Therefore the winding polarity of winding 11/13 corresponds to the secondary side of the flyback converter transformer. Start-up is not as smooth as with an immediately available supply voltage, because TDA 4601 has to be supplied by the start-up circuit until the entire secondary load has been charged. This leads to long switch-on times, especially if low line voltages are applied.

However, the switch-on time can be shortened by applying the special start-up circuit (dotted line). The uncontrolled phase of feedback control winding 15/9 is used for activating purposes. Subsequent to activation, the transistor T1 begins to block when winding 11/13 generates the current supply for TDA 4601. Therefore, the control circuit cannot be influenced during operation.

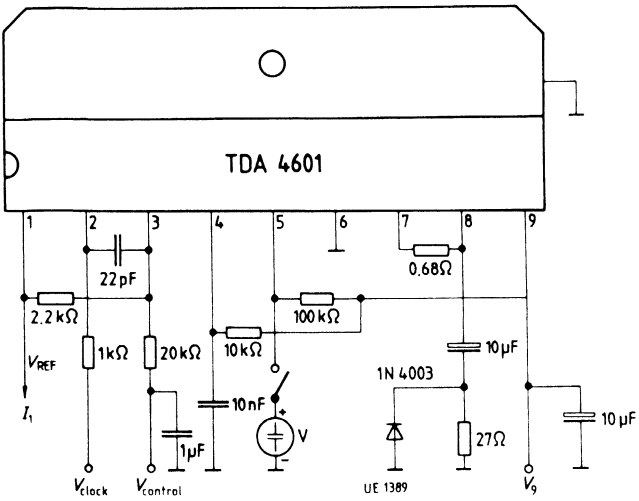
Pin Functions

Pin No.	Function
1	V_{REF} output
2	Zero passage identification
3	Input control amplifier, overload amplifier
4	Collector current simulation
5	Connection for additional protective circuit
6	Ground (rigidly connected to substrate mounting plate)
7	DC output for charging coupling capacitor
8	Pulse output - driving of switching transistor
9	Supply voltage

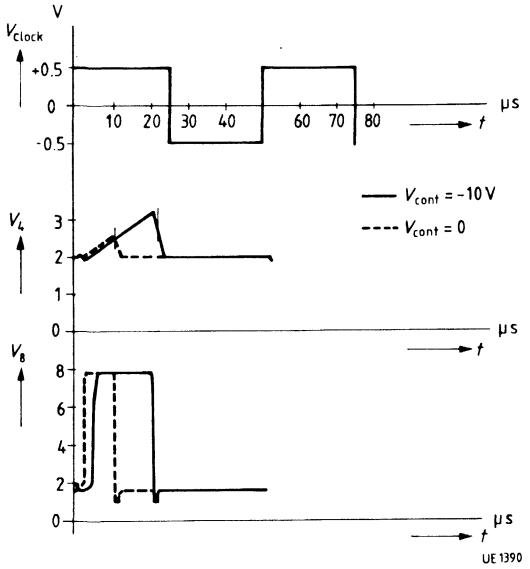
Circuit Diagram



Test and Measurement Circuit 1

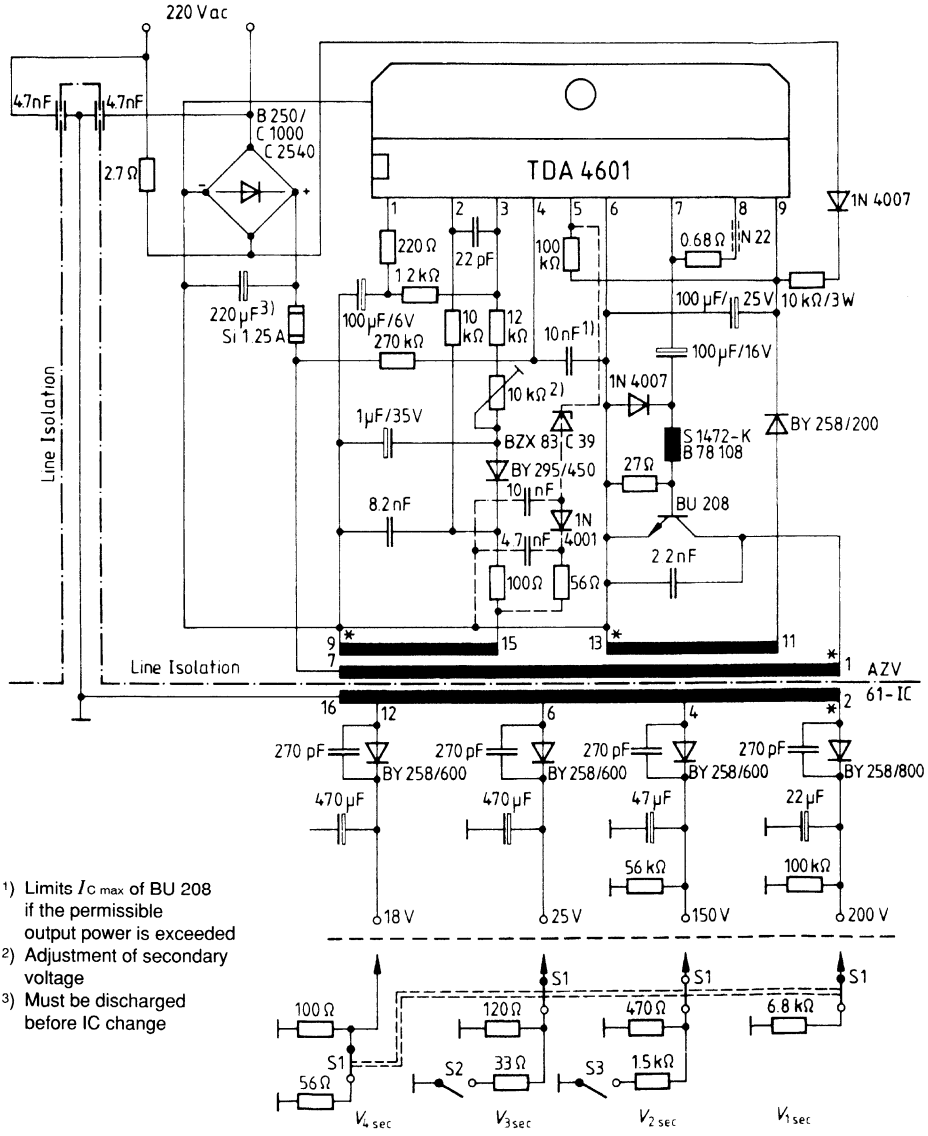


Test Diagram: Overload Operation



Application Circuit 1

Test and Measurement Circuit 2



1) Limits $I_{C\,max}$ of BU 208 if the permissible output power is exceeded
2) Adjustment of secondary voltage
3) Must be discharged before IC change

– – – Protective circuit against rise of secondary voltage in case of disturbance

Notes on application circuit 1

Protective Circuit against Secondary Voltage Rise even in Case of Disturbance

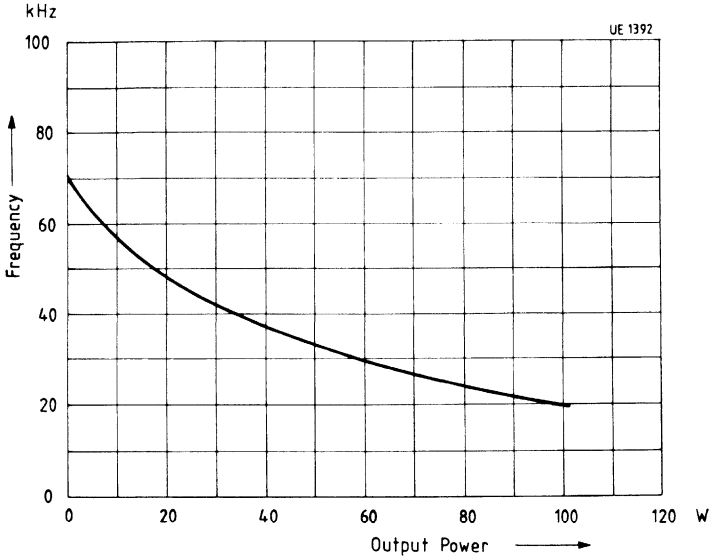
During standby this circuit type is necessary only under certain conditions. If switch S1 is open and the secondary side is loaded with no more than 1 to 5 W, a secondary voltage overshoot of approx. 20% will occur.

In case of disturbance (e.g. if the potentiometer is loosely contacted resulting in 10 kΩ (2), if the capacitor exhibits a 1 µF loss in capacitance, or if the 2 kΩ resistor increases to a high-impedance value of 32 kΩ), the protective effect of the standard turn-off is not active before the point of return has been reached. The result is that energy is pumped into the secondary side during disturbance, which will not ease off before is reached the point of return at worst and, entails an instantaneous doubling of the voltage to 300 V (endangering the secondary electrolytic capacitors).

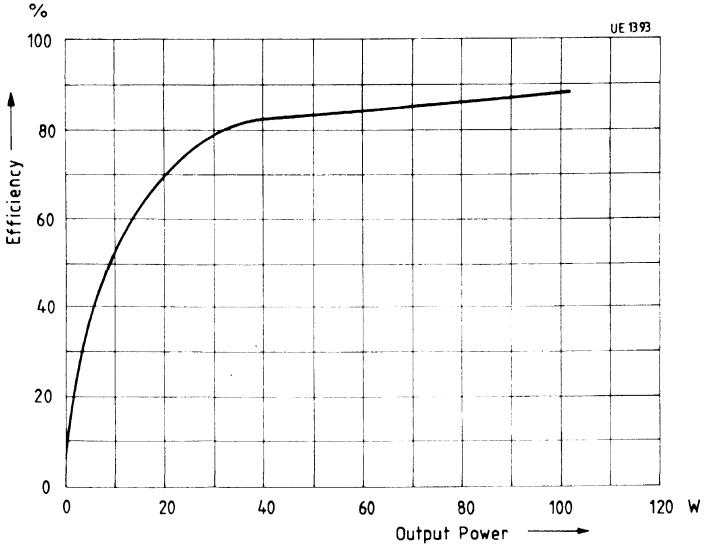
This additional protective circuit, which identifies the energy surge as voltage overshoot, is directly active at control winding 9/15. Through the 56 Ω resistor and the 1N4001 rectifier the negative portion is deducted and stored in the 10 µF capacitor. If the amplitude exceeds the voltage of Z-diode BZX 83/39, pin 5 is drawn below the turn-off threshold, inhibiting further control pulses at pin 8. During disturbance conditions the voltage overshoot on the secondary side will assume maximum values of approx. 30%.

Supplements to Test and Measurement Circuit 2

Efficiency versus output power

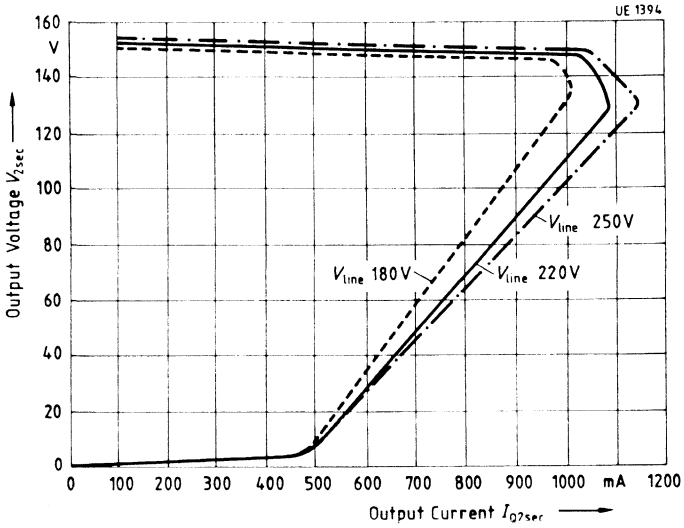


Efficiency versus output power

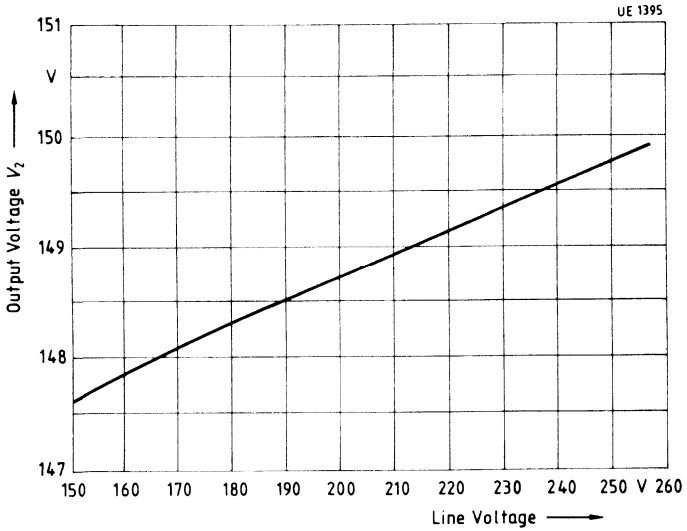


Supplements to Test and Measurement Circuit 2

Load characteristics $V_{2sec} = f(I_{2sec})$

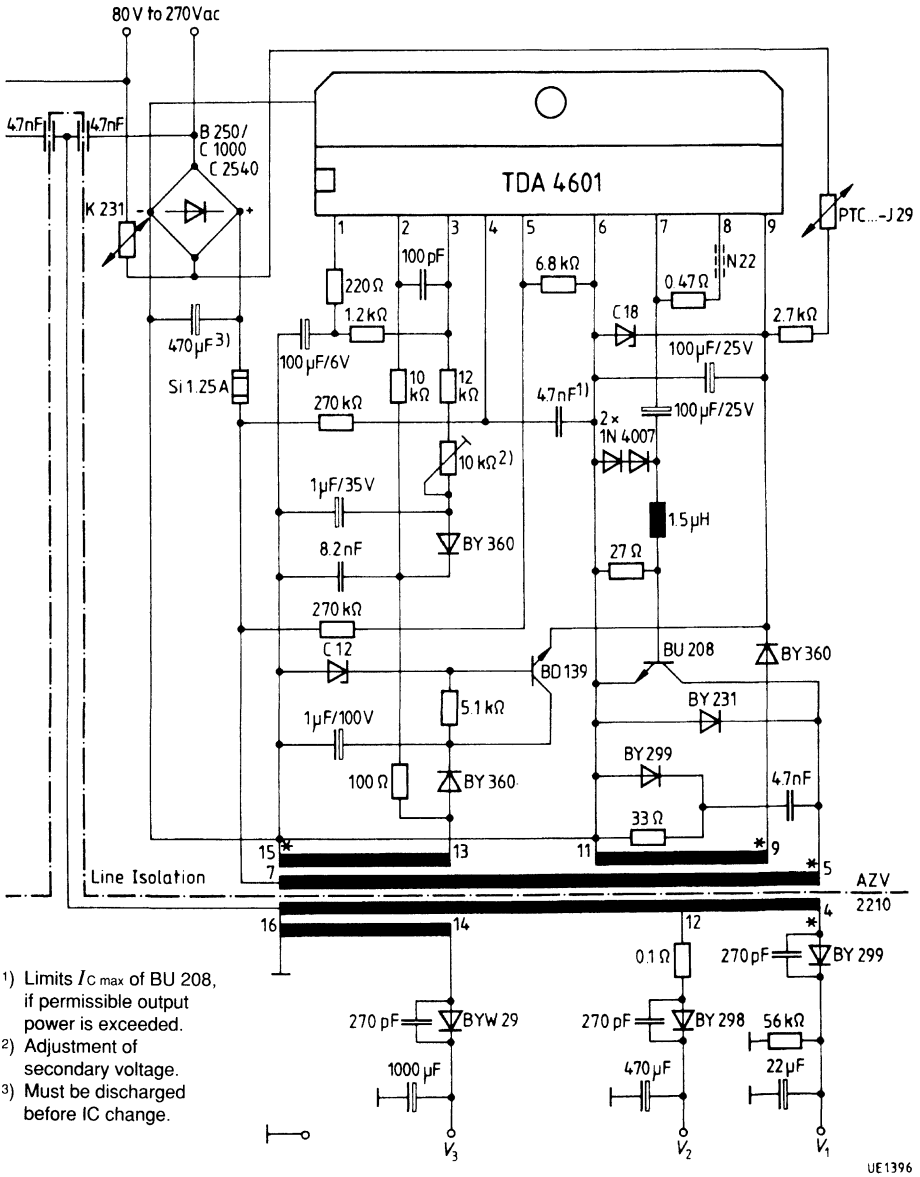


Output voltage V_{2sec} (Line change)



Application Circuit 2

Wide range from 80 to 270 Vac



1) Limits $I_{C\,max}$ of BU 208, if permissible output power is exceeded.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.

Notes on application circuit 2

Wide Range SMPS

Filtering of the rectified AC voltage has been increased up to 470 µF to ensure a constant and hum-free supply at V_{line} = 80 V AC. The stabilized phase is tapped for supplying the IC. In order to ensure good start-up conditions for the SMPS in the low voltage range, the non-stabilized phase of winding 13/15 is used as a starting aid (BD 139), which is turned off after start-up by means of Z-diode C12.

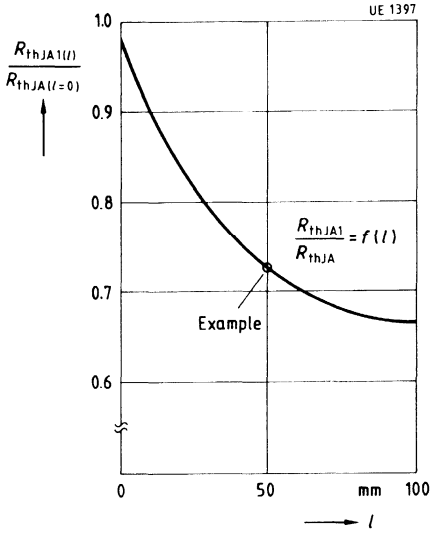
In comparison to the 220 Vac standard circuit, however, the collector-emitter circuit had to be altered to improve the switching behavior of BU 208 for the entire voltage range (80 to 270 Vac). Diode BY 231 is necessary to prevent inverse operation of BU 208 and may be integrated for switching times with a secondary power < 75 W (BU 208 D).

Compared to the IC TDA 4600-2, the TDA 4601 has been improved in turn-off during under- voltage at pin 5. The TDA 4601 is additionally provided with a differential amplifier input at pin 5, enabling precise turn-off at the output of pin 8 accompanied by hysteresis. For wide range SMPS, TDA 4601 is recommendable instead of TDA 4600-2. If a constant quality standard equal to that of the standard circuit is to be maintained, wide range SMPS (80 to 270 Vac) with secondary power of 120 W can only be implemented at the expense of time.

Thermal Resistance TDA 4601 D

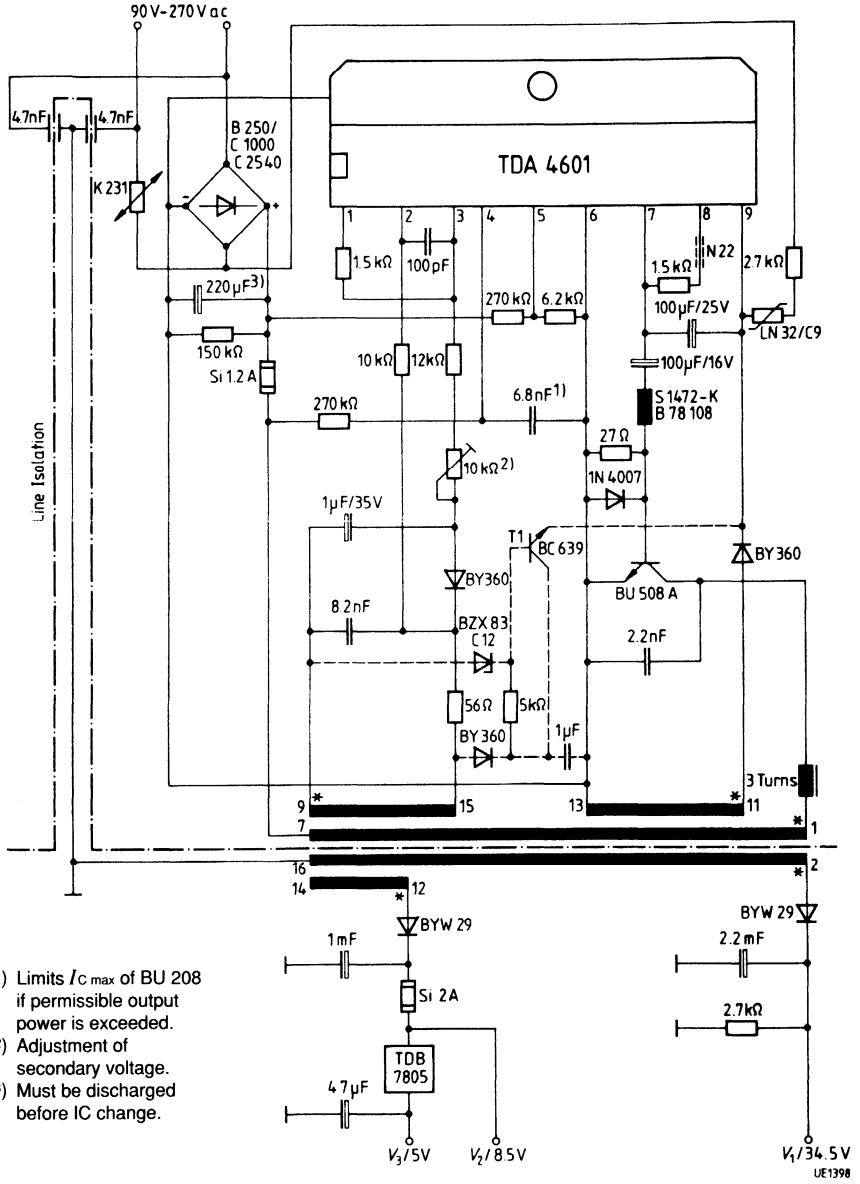
Standardized, ambient-related thermal resistance $R_{th\ JA1}$ versus length l of a square copper-clad cooling area (35 µm copper cladding)

$R_{th\,JA}$ (l = 0) = 60 K/W
T_A = 70 °C
P_d = 1 W
PC board in vertical position
Circuit in vertical position
Still air



Further Application Circuits

Application Circuit 3



1) Limits $I_{C\,max}$ of BU 208 if permissible output power is exceeded.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.

Notes on application circuit 3

Fully Insulated, Clamp-contacted PTC Thermistor Suitable for SMPS Applications at Increased Start-Up Currents

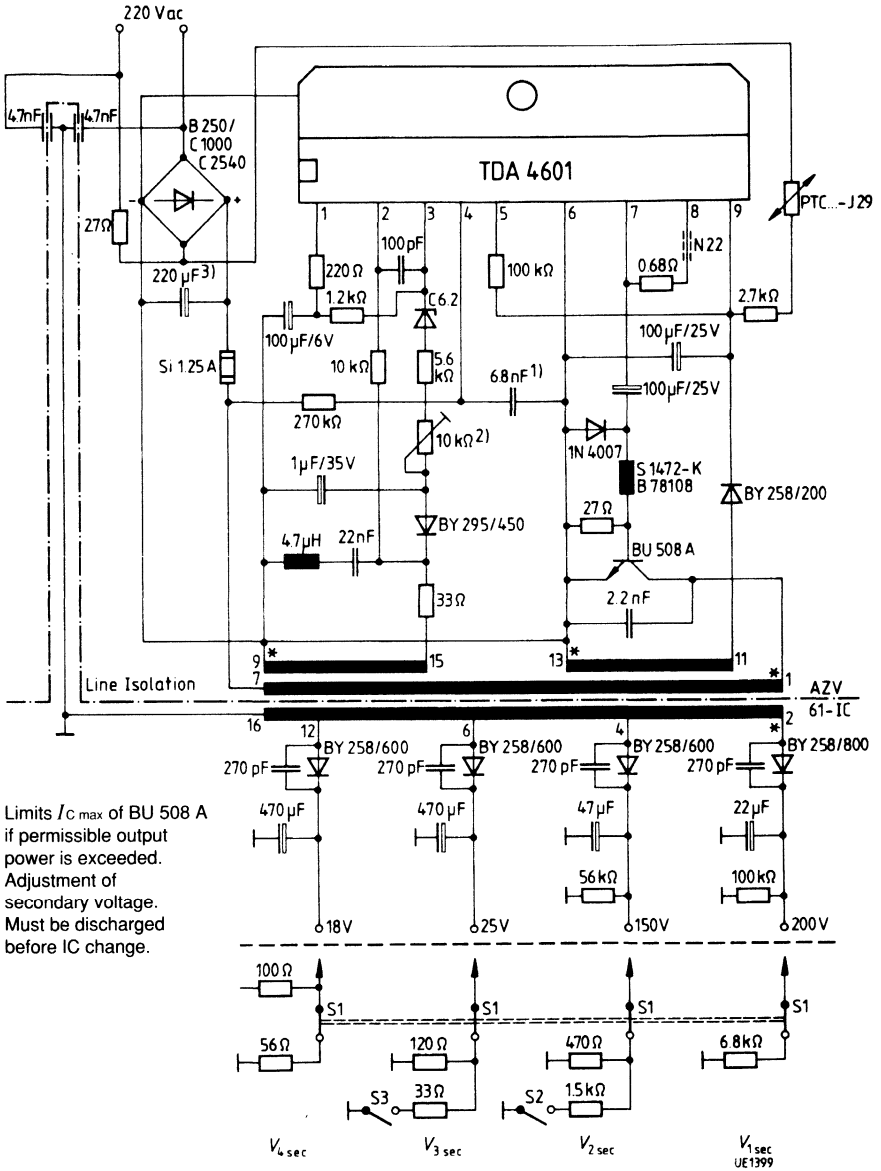
The newly developed PTC thermistor **Q63100-P2462-J29** is designed for applications in SMPS as well as in various other electronic circuits, which, for example, receive the supply voltage directly from the rectified line voltage and require an increased current during turn-on. Used in the flyback converter power supply of TV sets, an application proved millions of times over, the new PTC thermistor in the auxiliary circuit branch has resulted in a power saving of no less than 2 W. This increase in efficiency has a highly favorable effect on the standby operation of TV sets.

The required turn-on current needs only 6 to 8 s until the operating temperature of the PTC thermistor is reached. Low thermal capacitance of the PTC thermistor allows the circuit to be operated again after no more than 2 s. Another positive feature is the improved short-circuit strength. The clamp contacts permit more or less unlimited switching operations and thus guarantee high reliability. A flame-retardant plastic package and small dimensions are additional advantages of this newly developed PTC thermistor.

Technical Data

Parameter	Symbol	Limit Values	Unit
Breakdown voltage at T_A = 60 °C	$V_{BD\,rms}$	350	V
Resistance at T_A = 25 °C	R_{25}	5	kΩ
Resistance tolerance	ΔR_{25}	25	%
Trip current (typ.)	I_K	20	mA
Residual current at $V_{A\,max}$	I_R	2	mA
Max. application voltage	$V_{op\,max\,rms}$	265	V
Reference temperature (typ)	T_{REF}	190	°C
Temperature coefficient (typ)	TC	26	%/K
Max. operating current	I_{max}	0.1	A
Storage temperature range	T_{stg}	– 25 to 125	°C

Application Circuit 4



1) Limits $I_{C\,max}$ of BU 508 A if permissible output power is exceeded.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.

Notes on application circuit 4

Improved Load Control and Short-Circuit Characteristics

Turn-on is the same as for circuit 3.

To make the price more attractive, switching transistor BU 508 A was selected.

To ensure optimum standby conditions, the capacitance between pins 2 and 3 was increased to 100 pF.

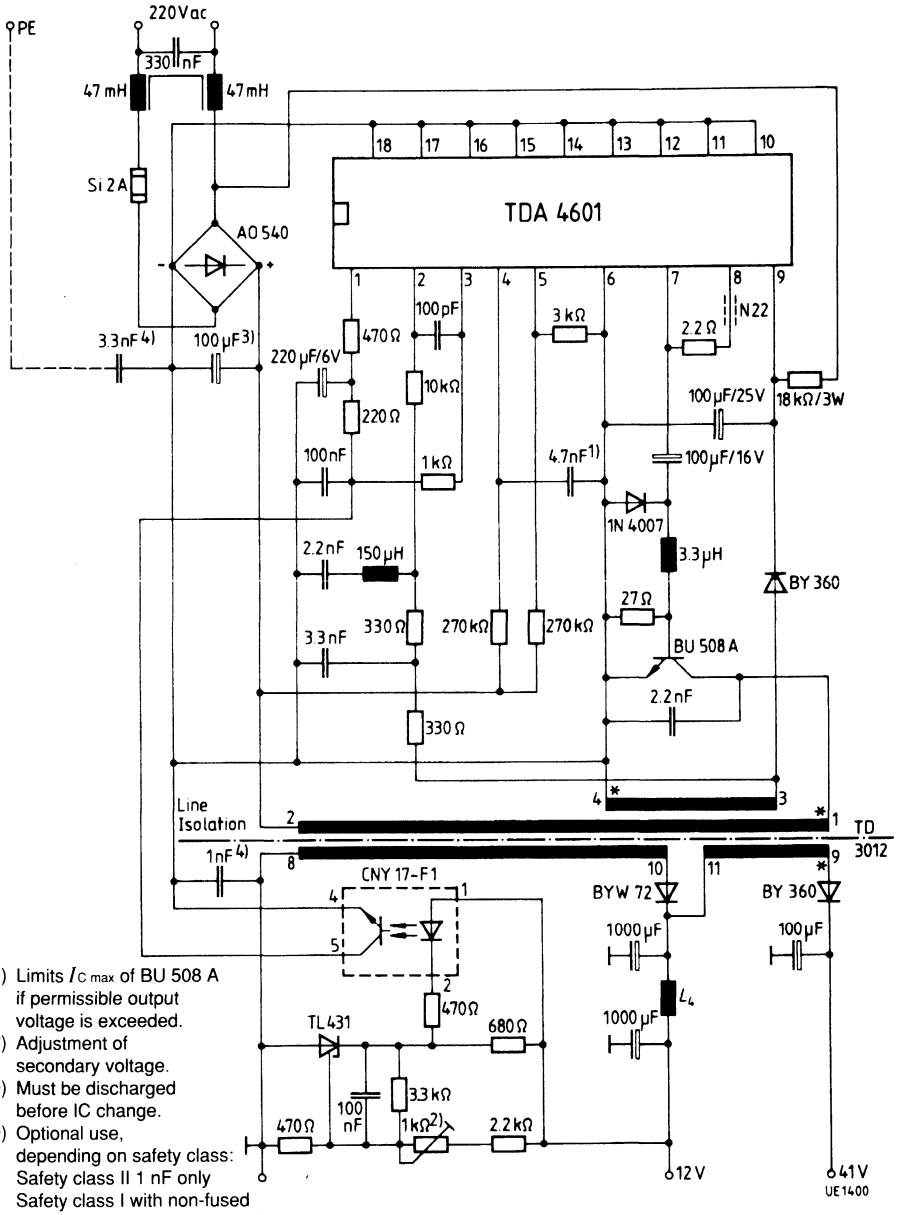
Z- diode C 6.2 transfers control voltage ΔV_{cont} directly to pin 3 resulting in improved load control.

Design and coupling conditions of various flyback transformers were sometimes a reason for overshoot spectra, which, despite the RC attenuating element 33 Ω × 22 nF and the 10 kΩ resistor, even penetrated across the feedback winding 9/15 to the zero passage indicator input (pin 2) and activated double and multiple pulses in the IC. Double and multiple pulses, however, lead to magnetic saturation in the flyback transformer and thus increase the risk of damaging the switched-mode power supply.

The larger the quantities of power to be passed, the more easily overshoots are generated. This can be observed around the point of return. The switched-mode power supply, however, reduces its own power to a minimum in all cases of overload or short-circuit. A series resonant circuit, whose resonance corresponds to the transformer's self-oscillation, was created by combination of the 4.7 µH inductance and the 22 nF capacitance. This resonant circuit short-circuits overshoots via a 33 Ω resistor.

$$\left(f = \frac{1}{2\,\pi\,\sqrt{LC}} \approx 500\ \text{kHz}\right)$$

Application Circuit 5



1) Limits $I_{C\,max}$ of BU 508 A if permissible output voltage is exceeded.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.
4) Optional use, depending on safety class: Safety class II 1 nF only Safety class I with non-fused grounded conductor 3.3 nF only

Notes on application circuit 5

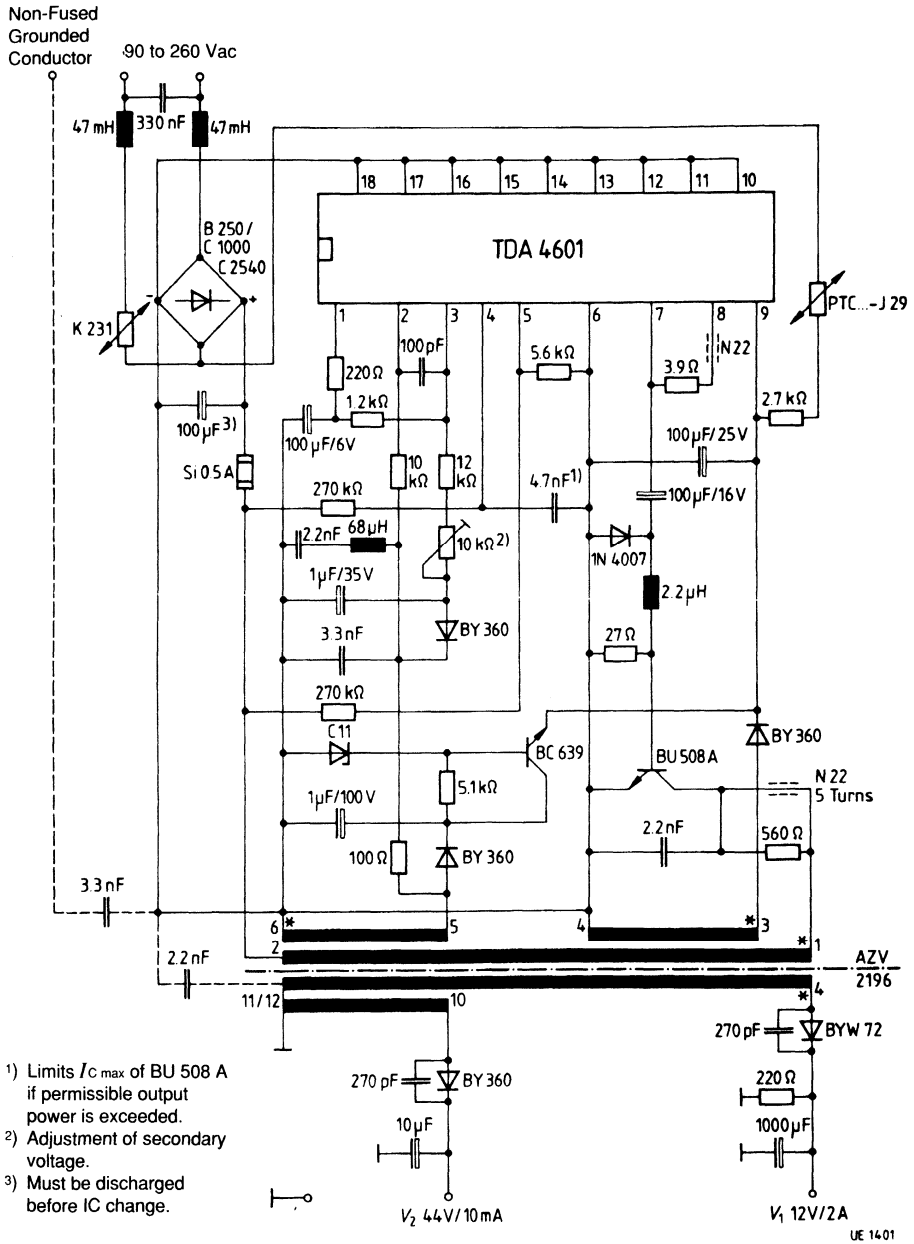
Highly Stable Secondary Side

Power supplies for commercial purposes require highly constant low voltages and high currents which, on the basis of the flyback converter principle, can be realized only under certain conditions, but, on the other hand, are implemented for economical reasons. An electrically isolated flyback converter with a highly stable secondary side must receive the control information from this secondary side. There are only two possibilities for meeting this requirement: either through a transformer which is magnetically isolated from the flyback converter or by means of an optocoupler. The development of CNY 17 has enabled the manufacture of a component suitable for electrical isolation and characterized by high reliability and long-term stability.

The IC TDA 4601 D is the sucessor of the TDA 4600 D. It is compatible with its predecessor in all operational functions and in the control of a self-oscillating flyback converter. Pin 3 is the input for the control information, where the latter is compared with the reference voltage prevailing at pin 1 and the control from the optocoupler and subsequently transformed into a frequency/pulse width control.

The previous feedback and control information winding is not necessary. The feedback information (zero passage) is obtained from winding 3/4 - supply winding. The time constant chain 330 Ω/3.3 nF and 330 Ω/2.2 nF was implemented in series with 150 µH to prevent interference at pin 2. The LC element forms a series resonant circuit for overshoots of the flyback converter and short-circuits them.

Application Circuit 6



1) Limits $I_{C\,max}$ of BU 508 A if permissible output power is exceeded.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.

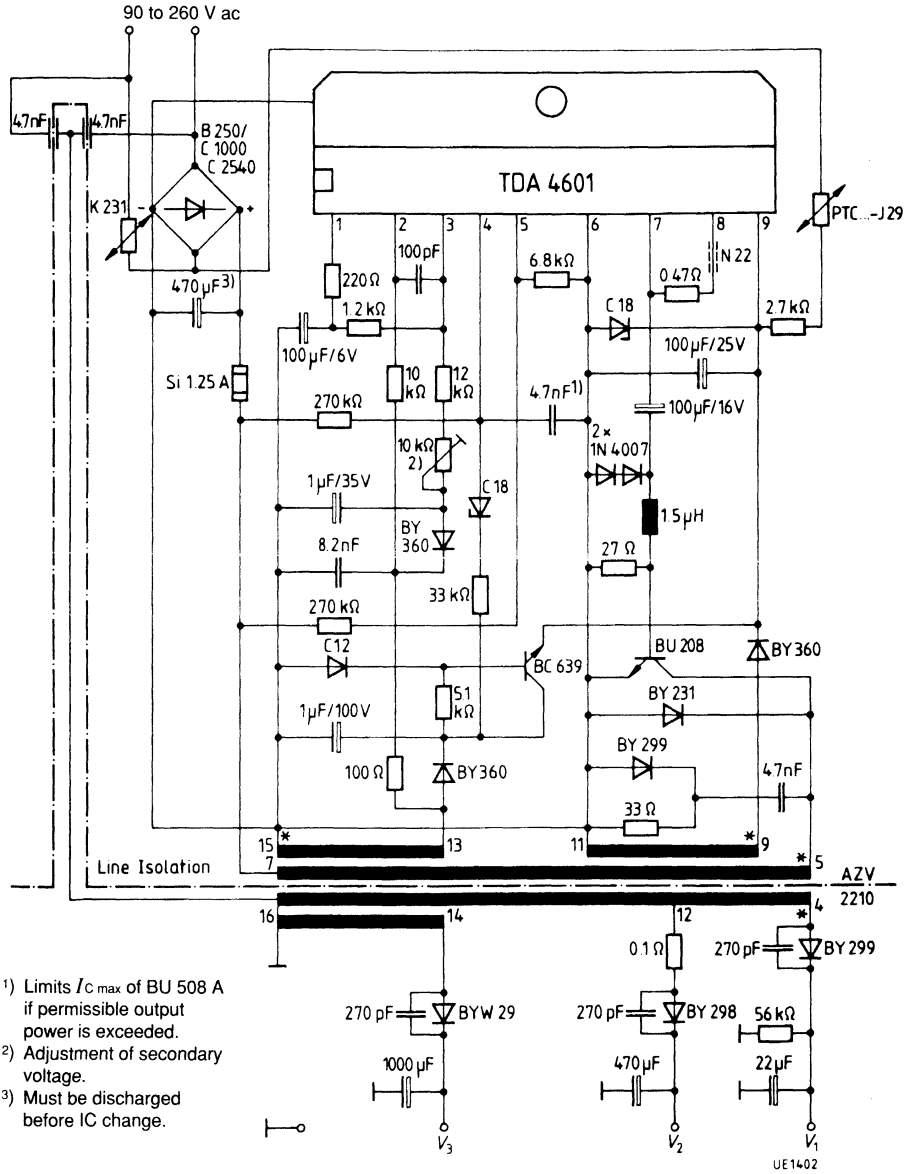
Notes on application circuit 6

Wide Range Plug SMPS up to 30 W

Due to their volume and weight, plug SMPS have so far been limited to a restricted primary voltage and a secondary power of no more than 6 W.

The line-isolated wide range flyback converter presented here has a variable frequency and is capable of producing a secondary power of 30 W. It is characterized by a compact design with an approx. weight of 400 g. The entire line voltage range of 90 to 260 V_{ac} is stabilized to ±1.5% on the secondary side. Load fluctuations between 0.1 and 2 A are regulated to within 5%. The output (secondary side) is overload, short-circuit, and open-loop proof.

Application Circuit 7



1) Limits $I_{C\,max}$ of BU 508 A if permissible output power is exceeded.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.

Notes on application circuit 7

Wide Range SMPS with Reducing Peak Collector Current $I_{C\ BU\ 208}$ for Rising Line Voltage (variable point of return)

Wide range SMPS have to be dimensioned at line voltages of 90 to 260 Vac. The difference between the maximum collector current $I_{C\ BU\ 208\ max}$ and the largest possible limit current $I_{C\ BU\ 208\ limit}$ which causes magnetic saturation of the flyback transformer and flows through the primary inductance winding 5/7 is to be determined at Vac_{min} ($I_{C\ BU\ 308\ limit} \geq 1.2 \times I_{C\ BU\ 208\ max}$). Then, the transmissible power of the flyback transformer and its value at Vac_{max} is to be determined. In the standard circuit the collector current $I_{C\ BU\ 208\ max}$ is almost constant at the point of return independent of the line voltage. The transmissible power on the secondary side, however, increases at the point of return in proportion to the rising rectified line voltage applied (**figures 1 and 2**).

In the wide range SMPS a line voltage ratio of 270/90 = 3/1 is obtained, causing doubling of the transmissible power on the secondary side, i.e. in the wide range SMPS a far too large flyback transformer had to be implemented.

.

The point of return protecting the SMPS against overloads or short circuits, is derived from the time constant at pin 4 $\tau 4 = 270\ k\Omega \times 4.7\ nF$. Thus, the largest possible pulse width is determined.

With the introduction of the 33 kΩ resistor this time constant is reduced as a function of the control voltage applied to winding 13/15, rectified by diode BY 360 and filtered by the 1 µF capacitance, which means that the pulse time becomes shorter. By means of the Z-diode C18 the line voltage level can be defined at which the influence of the time constant correction becomes noticeable. The change in the rectified voltage of winding 13/15 is proportional to the change in the rectified line voltage.

At the point of return $I_{C\ BU\ 208}$ the peak collector current has been reduced with the aid of the given values from 5.2 A at 90 Vac to 3.3 A at 270 Vac. The transmissible power at the point of return remains stable between 125 and 270 Vac due to the set activation point of the point of return correction (unbroken curve in **figure 2**).

Load Characteristics

Figure 1

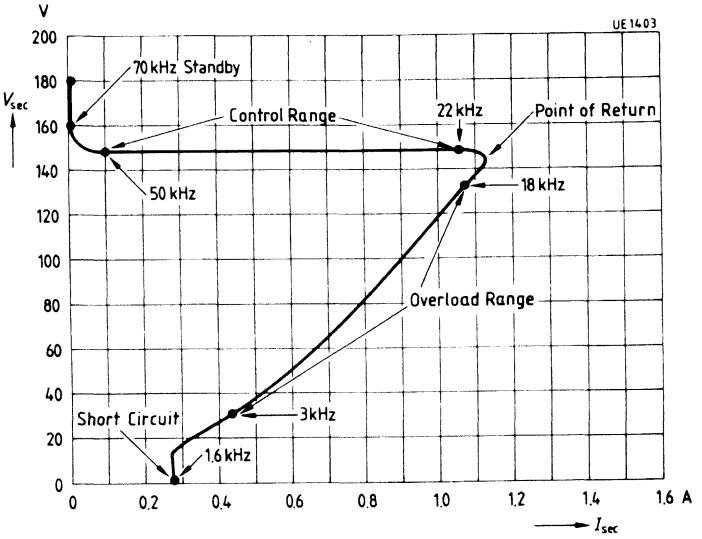
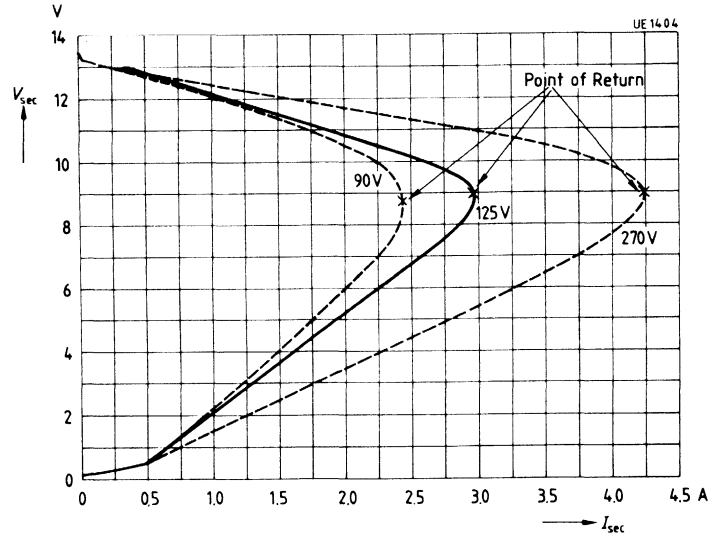


Figure 2



SIEMENS

Control IC for Switched-Mode Power Supplies using MOS Transistors

TDA 4605

Preliminary Data

Bipolar IC

Features

- Fold-back characteristic provides overload protection for external components
- Burst operation under short-circuit conditions
- Loop error protection
- Switch-off if line voltage is too low (undervoltage switch-off)
- Line voltage compensation of overload point
- Soft-start for quiet start-up
- Chip over-temperature protection (thermal shutdown)
- On-chip parasitic transformer oscillation suppression circuitry

Type	Ordering Code	Package
TDA 4605	Q67000-A8078	P-DIP-8

The IC TDA 4605 controls the MOS power transistor and performs all necessary regulation and monitoring functions in free running flyback converters. Since good load regulation over a wide load range is attained, this IC is applicable for consumer and industrial power supplies.

The serial circuit of power transistor and primary winding of the flyback transformer is connected to the input voltage. During the switch - on period of the transistor, energy is stored in the transformer and during the switch - off period it is fed to the load via the secondary winding. By varying switch-on time of the power transistor, the IC controls each portion of energy transferred to the secondary side such that the output voltage remains nearly independent of load variations.
The required control information is taken from the input voltage during the switch-on period and from a regulation winding during the switch off period.

In the different load ranges the switched-mode power supply (SMPS) behaves as follow:

No-load operation: The power supply unit oscillates at its resonant frequency typ. 100 kHz to 200 kHz. Depending upon the transformator windings the output voltage can be slightly above nominal value.

Nominal operation: The switching frequency declines with increasing load and decreasing AC voltage. The duty factor primarly depends on the AC voltage. The output voltage is load-dependent only.

Overload point: Maximal output power is available at this point of the output characteristic

Overload: The energy transfered per operation cycle is limited at the top. Therefore the output voltage declines by secondary overloading.

Circuit Description

1 Application Circuit

Application Circuit shows a flyback converter for video recorders with a power rating of 50 W. The circuit is designed as a wide-range power supply for AC line voltages of 90 to 270 V. The AC input voltage is rectified by bridge rectifier GR1 and smoothed by C_1. The NTC limits the rush in current.

In the period before the switch-on threshold is reached the IC is supplied via resistor R_1; during the start-up phase it uses the energy stored in C_2, under steady-state conditions the IC receives its supply voltage from transformer winding n_1 via diode D1. The switching transistor T1 is a BUZ 90. The parallel-connected capacitor C_3 and the inductance of primary winding n_2 determine the system resonance frequency. The R_2 - C_4 - D2 circuitry limits overshoot peaks, and R_3 protects the gate of T1 against static charges.

While T1 conducts, the current rise in the primary winding depends on the winding's nductance and the V_{C1} voltage. A voltage reproduction of the current rise is tabbed using the R_4 - C_5 network and forwarded into pin 2 of the IC. The RC time constant of R_4, R_5 must be dimensioned correctly in order to prevent driving the transformer core into saturation.

The R_{10}/R_{11} divider ratio provides the line voltage threshold controlling the undervoltage control circuit in the IC. The voltage present at pin 3 also determines the overload. Detection of overload together with the current characteristic at pin 2 controls the on period of T1. This keeps the cutoff point stable even with higher AC line voltages.

Regulation of the switched-mode power supply is via pin 1. The control voltage of winding n_1 during the off-period of T1 is rectified by D3, smoothed by C_6 and stepped down at an adjustable ratio by R_5, R_6 and R_7. The R_8 - C_7 network suppresses parasitic overshoots (transformer oscillation). The peak voltage at pin 2, and thus the primary peak current, is adjusted by the IC so that the voltage applied across the control winding, and hence the output voltages, are at the desired level.

When the tranformer has supplied its energy to the load, the control voltage passes through zero. The IC detects the zero crossing via series resistors R_9 connected to pin 8. But zero crossings are also produced by transformer oscillation after T1 has turned off if output is short-circuited. Therefore the IC ignores zero crossings occurring within a specified period of time after T1 turn-off.

The capacitor C_8 connected to pin 7 causes the power supply to be started with shorter pulses to keep the operating frequency outside the audible range during start-up.

On the secondary side, five output voltages are produced across winding n_3 to n_7 rectified by D4 to D8 and smoothed by C_9 to C_{13}. Resistors R_{12}, R_{14} and R_{19} to R_{21} are used as bleeder resistors. Fusable resistors R_{15} to R_{18} protect the rectifiers against short circuits in the output circuits, which are designed to supply only small loads.

2 Block Circuit Diagram

Pin1 The regulating voltage forwarded to this pin is compared with a stable internal reference voltage V_R in the **regulating and overload amplifier.** The output of this stage is fed to the stop comparator.

Pin2 A voltage proportional to the drain current of the switching transistor is generated there by the external RC combination in conjunction with the **primary current transducer.** The output of this transducer is controlled by the logic and referenced to the internal stable voltage V_{2B}. If the voltage V_2 exceeds the output voltage of the regulating amplifier, the logic is reset by the stop comparator and consequently the output of pin 5 is switched to low potential. Further inputs for the logic stage are the output for the **start impulse generator** with the stable reference potential V_{St} and the **supply voltage monitor.**

Pin3 The down-divide primary voltage applied there stabilizes the overload point. In addition the logic is disabled in the event of low voltage by comparison with the internal stable voltage V_V in the **primary voltage monitor** block.

Pin4 Ground

Pin5 In the output stage the output signals produced by the logic are shifted to a leved suitable for MOS power transistors.

Pin6 From the supply voltage V_6 are derived a stable internal reference V_{REF} and the switching threshold V_{6A}, V_{6E}, V_{6max} and V_{6min} for the **supply voltage monitor.** All reference values (V_R, V_{2B}, V_{ST}) are derived from V_{REF}. If $V_6 > V_{VE}$, the V_{REF} is switched on and switched off when $V_6 < V_{6A}$. In addition, the logic is released only for $V_{6min} < V_6 < V_{6max}$.

Pin7 The output of the overload amplifier is connected to pin 7. A load on this output causes a reduction in maximal impulse duration. This function can be used to implement a soft start, when pin 7 is connected to ground by a capacitor.

Pin8 The zero detector controlling the logic block recognizes the transformer being discharged by positive to negative zero crossing of pin 8 voltage and enables the logic for a new pulse. Parasitic oscillations occurring at the end of a pulse cannot lead to a new pulse (double-pulsing), because an internal circuit inhibits the zero detector for a finite time t_{UL} after the end of each pulse.

3 Start-Up Behaviour

The start-up behaviour of the application circuit per sheet 504 is represented on sheet 506 for a line voltage barely above the lower acceptable limit voltage value (without soft start). After applying the line voltage at the time t_0 the following voltages built up:

- V_6 corresponding to the half-wave charge current over R_1
- V_2 to $V_{2\,max}$ (typically 6.6V)
- V_3 to the value determined by the divider R_{10}/R_{11}.

The current drawn by the IC in this case is less than 1.6 mA. If V_6 reaches the threshold V_{6E} (time point t_1), the IC switches on the internal reference voltage. The currentdraw max. rises to 12 mA. The primary current- voltage reproducer regulates V_2 down to V_{2B} and the starting impulse generator generates the starting impulses from time point t_5 to t_6. The feedback to pin 8 starts the next impulse and so on. All impulses including the starting impulse are controlled in width by regulating voltage of pin 1. When switching on this corresponds to a short-circuit event, i.e. $V_1 = 0$. Hence the IC starts up with "short-circuit impulses" to assume a width depending on the regulating voltage feedback (the IC operates in the overload range). The maximum pulse width is reached at time point t_2 ($V_2 = V_{2\,max}$). The IC operates at the overload point. Thereafter the peak values of V_2 decrease rapidly, as the IC is operating within the regulation range. The regulating loop has built up. If voltage V_6 falls below the switch-off threshold $V_{6\,min}$ before the reversal point is reached, the starting attempt is aborted (pin 5 is switched to low). As the IC remains switched on, V_6 further decreases to V_6. The IC switches off; V_6 can rise again (time point t_4) and a new start-up attempt begins at time point t_1. If the rectified alternating line voltage (primary voltage) collapses during load, V_3 can fall below V_{3A}, as is happening at time point t_3 (switch-on attempt when voltage is too low). The primary voltage monitor then clamps V_3 to V_{3S} until the IC switches off ($V_6 < V_{6A}$). Then a new start-up attempt begins at time point t_1.

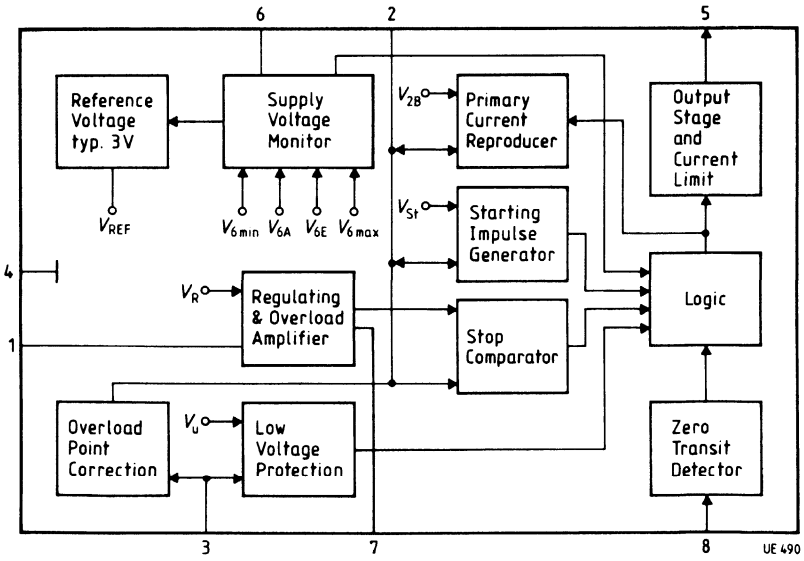
4 Regulation, Overload and No-Load Behaviour

When the IC has started up, it is operating in the regulation range. The potential at pin 1 typically is 400 mV. If the output is loaded, the regulation amplifier allows broader impulses (V_5 = H). The peak voltage value at pin 2 increases up to $V_{2S\,max}$. If the secondary load is further increased, the overload amplifier begins to regulate the pulse width downward. This point is referred to as the overload point of the power supply. As the IC supply voltage V_6 is directly proportional to the secondary voltage, if goes down in accordance with the overload regulation behaviour. If V_6 falls below the value $V_{6\,min}$, the IC goes into burst operation. As the time constant of the half-wave charge-up is relatively large, the short-circuit power remains small. The overload amplifier cuts back to the pulse width t_{pk}. This pulse widht must remain possible, in order to permit the IC to start-up without problems from the virtual short circuit, which every switching on with $V_1 = 0$ represents. If the secondary side is unloaded, the loading impulses (V_5 = H) become shorter. The frequency increases up to the resonance frequency of the system. If the load is further reduced, the secondary voltages and V_6 increase. When $V_6 = V_{6\,max}$, the logic is blocked. The IC converts to burst operation. This renders the circuit absolutely safe under no-load conditions.

5 Behaviour when Temperature Exceeds Limit

An integrated temperature protection disables the logic when the chip temperature becomes too high. The IC automatically interrogates the temperature and starts as soon as the temperature decreases to permissible values.

Block Diagram



Pin Definitions and Functions

Pin No.	Function
1	**Regulating voltage:** Information input concerning secondary voltage. By comparing the regulating voltage - obtained from the regulating winding of the transformer - with the internal reference voltage, the output impulse width on pin 5 is adapted to the load of the secondary side (normal, overload, short circuit, no load)
2	**Primary current simulation:** Information input regarding the primary current. The primary current rise in the primary winding is simulated at pin 2 as a voltage rise by means of external RC element. When a value is reached that is derived from the regulating voltage at pin 1, the output impulse at pin 5 is terminated. The RC element serves to set the maximum power at the overload point set.
3	**Primary voltage detector:** Input for primary voltage monitor. When the line voltage is too low the IC is switched off by comparing V_3 with an internal reference. Voltage at pin 3 is used for overload point compensation. Overload point compensation will work 7 times the under voltage limit set.
4	**Ground**
5	**Output:** Push-pull-output provides ± 1 A for rapid charge and discharge of the gate capacitance of the power MOS transistor
6	**Supply voltage:** Supply voltage input. From it a stable internal reference voltage V_{REF} and the switching thresholds V_{6A}, V_{6E}, $V_{6\,max}$ and $V_{6\,min}$ for the supply voltage detector is formed. If $V_6 > V_{6E}$ then V_{REF} is switched on and swiched off when $V_6 < V_{6A}$. In addition the logic is only enable for $V_{6min} > V_6$
7	**Soft-Start:** Input for soft start. Start up will begin with short pulses by connecting a capacitor from pin 7 to ground.
8	**Zero detector:** Input for the oscillation feedback. After starting oscillation, every zero transit of the feedback voltage (falling edge) triggers an output impulse at pin 5. The trigger threshold is at + 50 mV typical.

Absolute Maximum Ratings

T_A = 25 °C

Parameter		Symbol	Limit Values		Unit	Remarks
			min.	max.		
Voltages	pin1	V_1	– 0.3	3	V	
	pin2	V_2	– 0.3		V	
	pin3	V_3	– 0.3		V	
	pin5	V_5	– 0.3	V_6	V	
	pin6	V_6	– 0.3	20	V	Supply voltage
	pin7	V_7	– 0.3	6	V	
Currents	pin1	I_1		3	mA	
	pin2	I_2		3	mA	
	pin3	I_3		3	mA	
	pin4	I_4	– 1.5		A	$t_p \leq 50\mu s; v \leq 0.1$
	pin5	I_5	– 1.5	1.5	A	$t_p \leq 50\mu s; v \leq 0.1$
	pin6	I_6		1.5	A	$t_p \leq 50\mu s; v \leq 0.1$
	pin7	I_7		3	mA	
	pin8	I_8	– 3	3	mA	
Junction temperature		T_j		125	°C	
Storage temperature		T_{stg}	– 40	125	°C	

Operating Range

Supply voltage	V_6	8	14	V	IC "on"
Ambient temperature	T_A	– 20	85	°C	
Heat resistance					
Junction environment	$R_{th\ J\text{-}E}$		100	K/W	
Junction package	$R_{th\ J\text{-}G}$		70	K/W	measured at pin 4

Characteristics

T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Start-Up Hysteresis							
Start-up current	I_{6E0}	0.5	1.1	1.6	mA	$V_6 = V_{6E}$	1
Switch-on voltage	V_{6E}	11	12	13	V		1
Switch-off voltage	V_{6A}	6.4	6.9	7.4	V		1
Switch-on current	I_{6E1}	7	9	12	mA	$V_6 = V_{6E}$	1
Switch-off current	I_{6A1}	6.5	8	10	mA	$V_6 = V_{6A}$	1
Voltage Clamp (V_6 = 10V, IC switched off)							
at pin 2 ($V_6 < V_{6E}$)	V_{2max}	5.6	6.6	7.6	V	I_2 = 1mA	1
at pin 3 ($V_6 < V_{6E}$)	V_{3max}	5.6	6.6	7.6	V	I_3 = 1mA	1
Regulation Range							
Regulation input voltage	V_{1R}	370	400	430	mV		2
Voltage gain regulation range	$-V_R$	47	50	53	dB	V_R = d (V_{2S} - V_{2B})/dV_1	2
Regulation transmittance	R_R		20		kΩ	R_R = d (V_{2S} - V_{2B})/-dI_2	2
Primary Current Reproducer							
Basic value	V_{2B}	0.90	1.00	1.15	V		2
Input resistance $R_{2B} = \Delta V_{2B}/\Delta I_{2B}$	R_{2B}		25	40	Ω	V_3 = 1.5V; 1.2V < V_2 < 3V 0.1mA < I_{2B} < 3mA	2
Slew rate falling edge	dV_2/dt		– 1		V		2

Characteristics (cont 'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Overload Range and Short Circuit Operation							
Overload range lower limit	V_{1U}	60	230	290	mV		2
Voltage gain in overload range	$V_{Ü}$	1	2	3		$V_{Ü}$ = d ($V_{2S} - V_{2B}$)/dV_1	2
Input current in short circuit operation	$-I_1$	90	120	180	µA	V_1 = 0V	2
Peak value in overload range	$V_{2Ü}$		3.0		V	$V_1 = V_{1R}$ –10mV	2
Peak value in short circuit operation	V_{2K}	2.2	2.6	3.0	V	V_1 = 0V	2
Generally Valid Data (V_6 = 10V)							
Overload Point Correction							
Overload point correction current	$-I_2$	400	660	850	µA	V_3' = 4V;V_2' = 0V	1
Zero Transition Detector Voltage							
Positive clamp	V_{8P}	0.70	0.75	0.80	V	I_8 = 1mA	2
Negative clamp	V_{8N}	– 0.15	– 0.22	– 0.25	V	I_8 = – 1mA	2
Threshold value	V_{8S}	40	50		mV		2
Input current	$-I_8$		2	4	µA	V_8 = 0	2

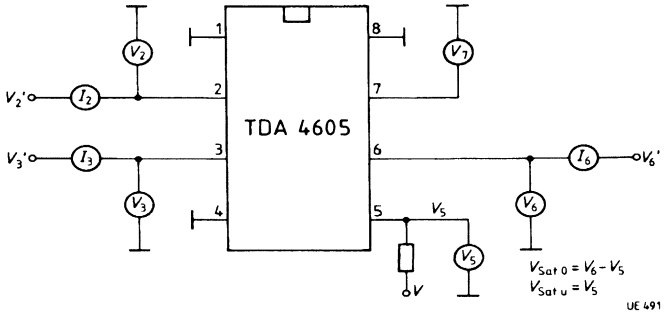
Characteristics (cont 'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Delay time between V_8 and V_5	t_{d2}	0.2	0.4	0.7	µs		2
Zero detector disable time	t_{UL}	2	2	6	µs		
Output Stage							
Saturation voltages S in position 1							
Output sourcing	V_{Sat0}		1.5	2.0	V	$I_5 = -0.1A$	1
Output sourcing	V_{Sat0}		2.5	3.0	V	$I_5 = -1A$	1
Output sinking	V_{SatU}		1.0	1.2	V	$I_5 = 0.1A$	1
Output sinking	V_{SatU}		1.4	1.8	V	$I_5 = 0.5A$	1
Output slew rate							
Rising slope	$+ dV_5/dt$		50		V/µs		2
Falling slope	$- dV_5/dt$		80		V/µs		2
Soft-Start							
Open circuit	V_7	2.2	2.6	2.9	V	$V_1 = 0$	2
Input resistance	R_{7L}	4	6	9	kΩ	$0.5V \leq V_7 \leq 3V$	2
Peak voltage	V_{2S}	1.0	1.2	1.4	V	$V_7 = 0$	2
Protection Circuit							
Undervoltage protection for V_6 voltage at pin 5 = $V_{5\,min}$ if $V_6 < V_{6\,min}$ (defintion: $V_{6\,min} = V_{6A} + \Delta V_6$)	ΔV_6		100		mV		2
Overvoltage protection for V_6 voltage at pin 5 = $V_{5\,min}$ if: $V_6 > V_{6\,max}$	V_{6max}	14	15	16	V		2

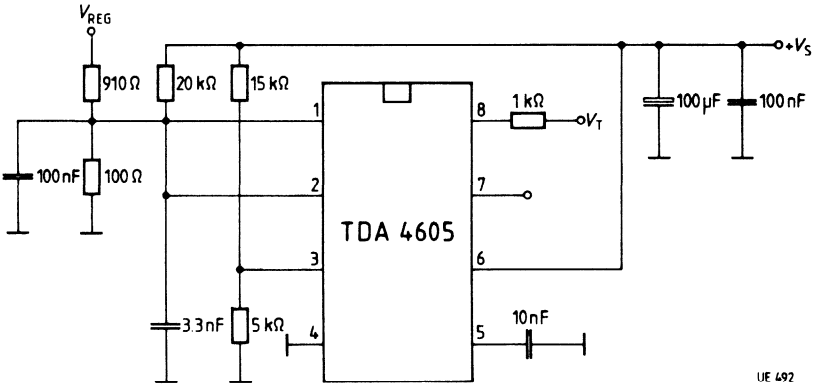
Characteristics (cont 'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Undervoltage protection for V_{AC} voltage at pin 5 = $V_{5\,min}$ if $V_3 < V_{3A}$	V_{3A}	925	1000	1075	mV	V_2' = 0V	1
Over temperature chip temperature for $V_{5\,min}$	T_j		125		°C		2
Voltage at pin 3 when protection function occured; (V_3 will be clamped until $V_6 < V_{6A}$)	V_{3S}		0.4	0.8	V	I_3 = 1mA	1
Burst operation quiescient current	I_6		8		mA	$V_3 = V_2$ = 0V	1

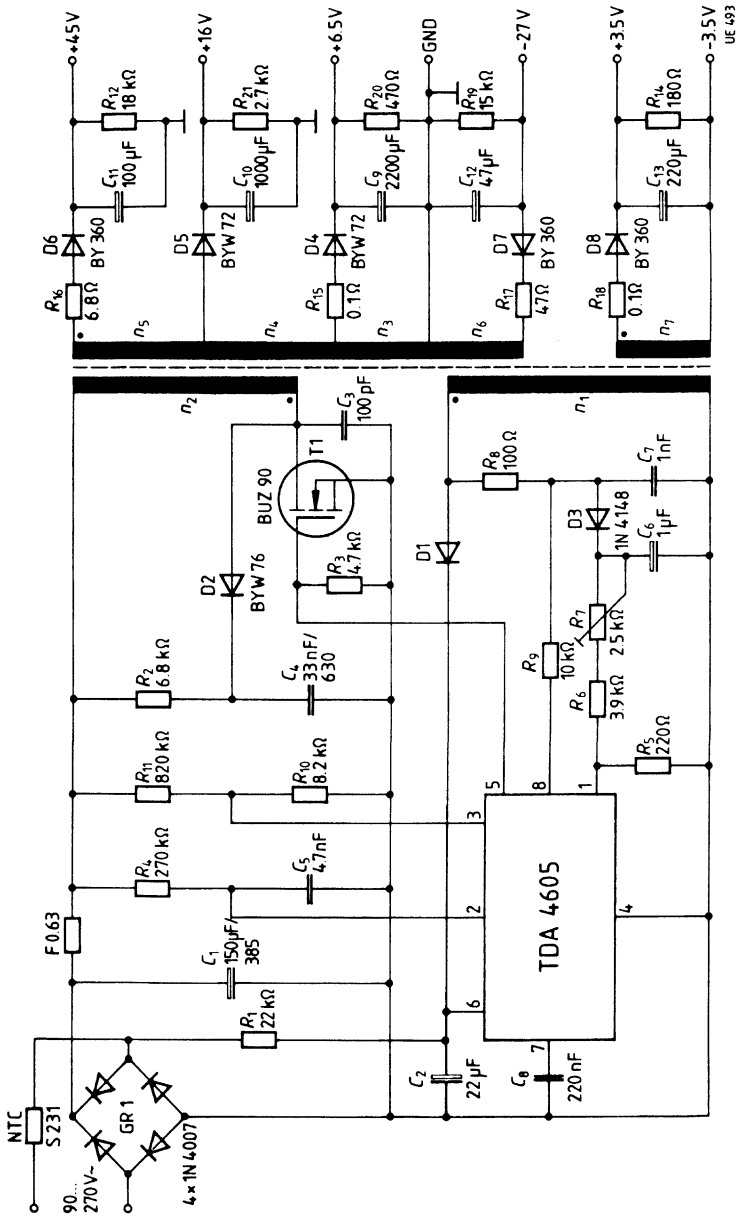
Test Circuit 1



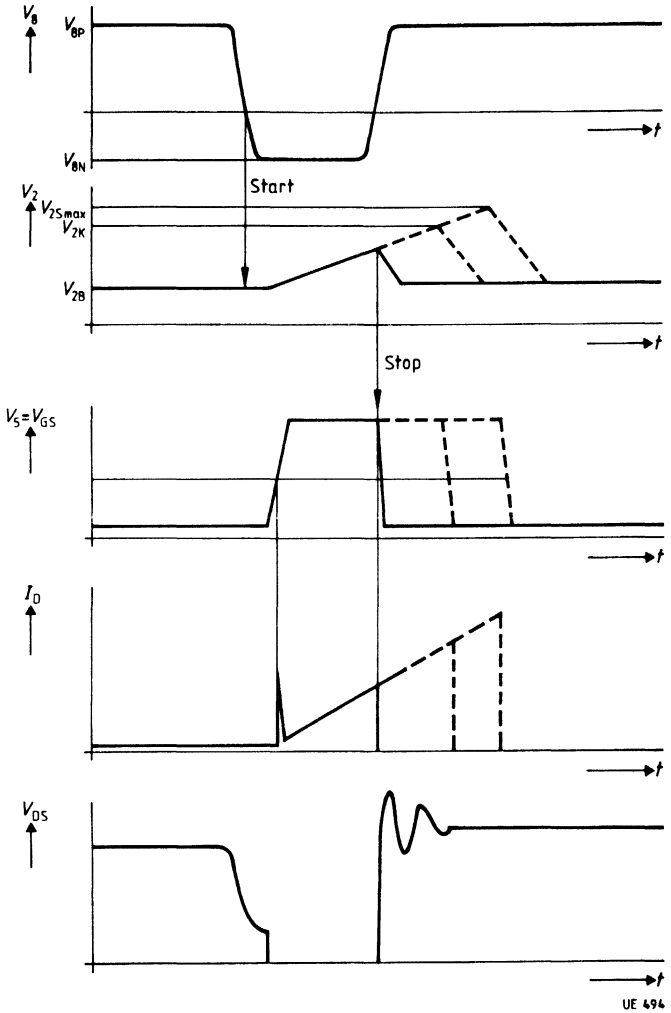
Test Circuit 2



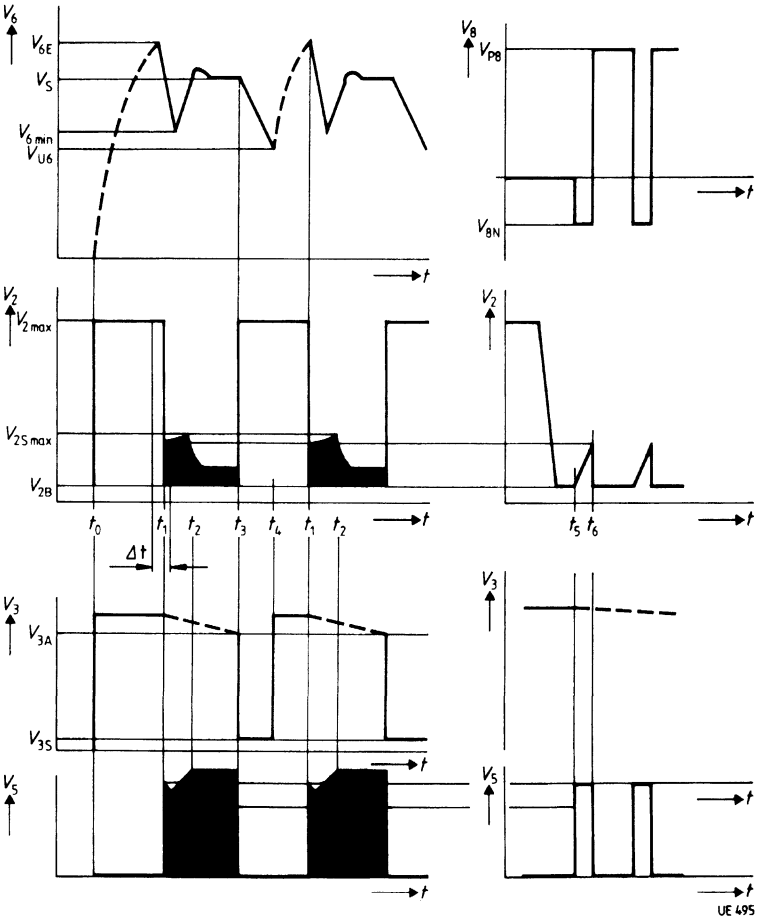
Application Circuit



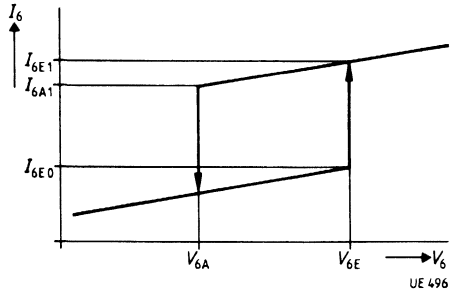
Diagrams


V_8
V_{8P}
V_{8N}
t
Start
V_2
V_{2Smax}
V_{2K}
V_{2B}
t
Stop
$V_S=V_{GS}$
t
I_D
t
V_{DS}
t
UE 494

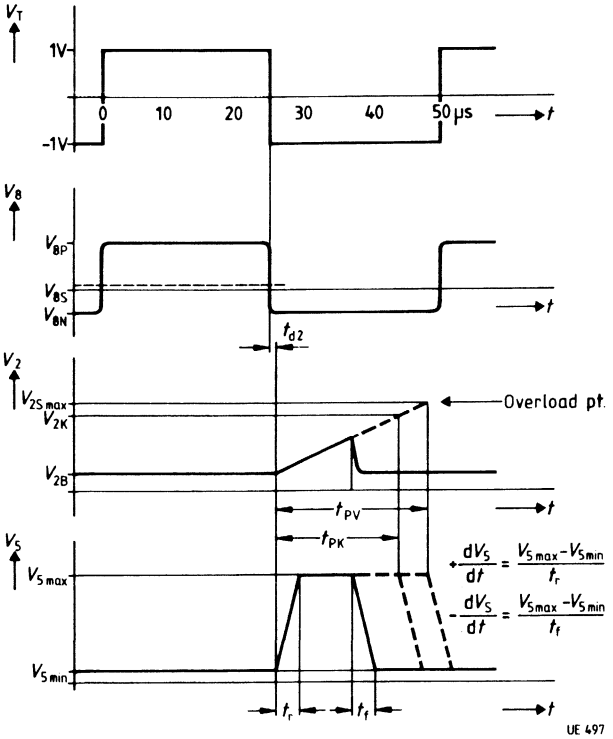
Diagrams


V6
V6E
VS
V6 min
VU6
t
V8
VP8
V8N
t
V2
V2 max
V2S max
V2B
t0
t1
t2
t3
t4
t1
t2
t
Δt
V2
t5
t6
t
V3
V3A
V3S
t
V5
t
V3
V5
t
UE 495

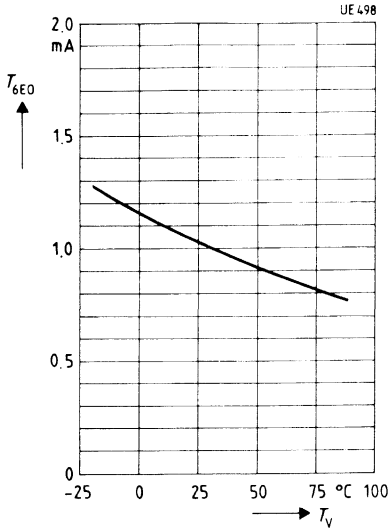
Start-Up Hysteresis



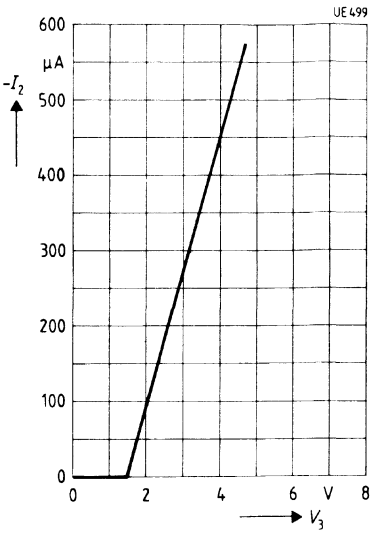
Operation in Test Circuit 2



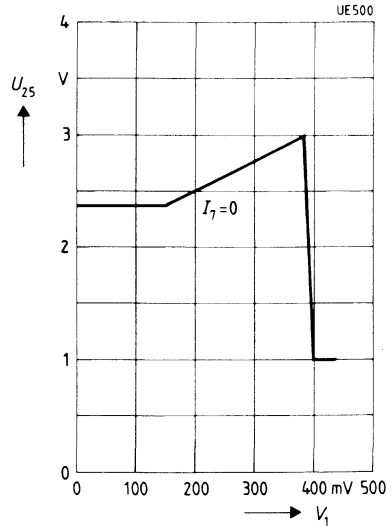
Start-up current as a function of the ambient temperature



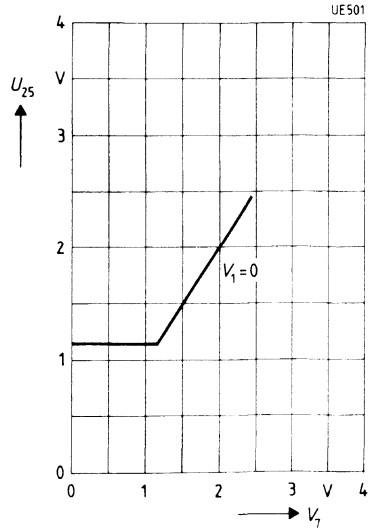
Overload point correction as a function of the voltage at pin 3



Peak value of the primary current reproduct. volt. as a function of the regulating voltage

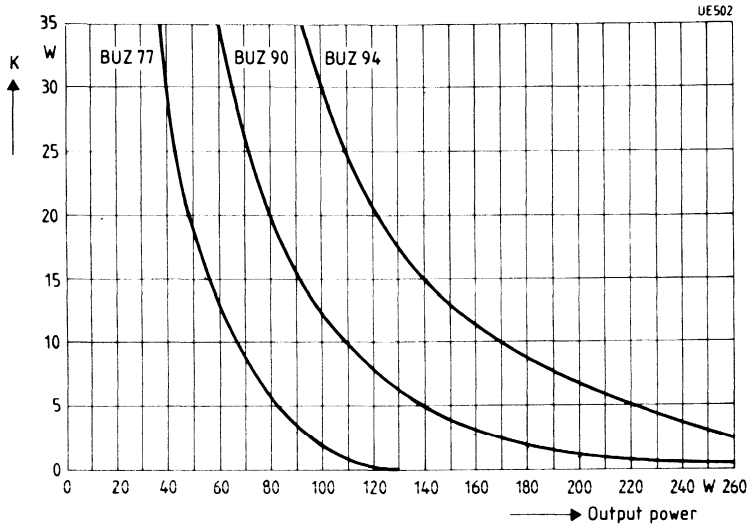


Peak value of the primay current reproduction voltage by loading pin 7

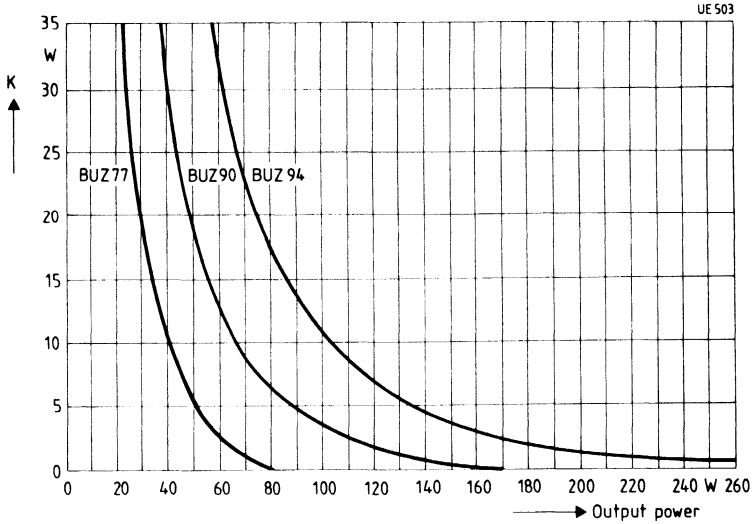


Recommended haet sink by 60 °C ambient temperature

SMALL RANGE 180V ... 270V~



WIDE RANGE 180V ... 270V~



Stereo/Bridge AF Amplifier 2 x 15 W/30 W

TDA 4935

Bipolar IC

Features

- Universal application as stereo amplifier or mono amplifier in bridge configuration
- Wide supply voltage range
- Minimum of external components

Type	Ordering Code	Package
TDA 4935	Q67000-A2538	P-SIP-9

The TDA 4935 can be applied as a class B stereo amplifier or mono amplifier in bridge configuration for AF signals. In addition, the component is provided with a protective circuitry against overtemperature and overload.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	32	V
Output peak current	I_1; I_9	2.8	A
Input voltage range	V_2; V_3; V_7	– 0.3 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 40 to 125	°C
Thermal resistance (system-case)	$R_{th\,JC}$	4	K/W

Operating Range

Supply voltage			
$R_L \geq 8\ \Omega$	V_S	8 to 30	V
$R_L = 4\ \Omega$	V_S	8 to 24	V
Case temperature (P_V=15W)	T_C	– 20 to 85	°C

Characteristics
V_S = 24 V; T_C = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Quiescent current V_I = 0	I_5		40	80	mA	1
Output voltage V = 0	$V_{Q\,1;9}$	11	12	13	V	1
Input resistance[1]	$R_{I\,3;7}$		20		kΩ	1
Output power f = 1 kHz – stereo operation						
THD = 1%	$P_{Q\,1;9}$	10	12		W	1
THD = 10%	$P_{Q\,1;9}$	13	15		W	1
– bridge operation						
THD = 1%	$P_{Q\,1;9}$	20	24		W	2
THD = 10%	$P_{Q\,1;9}$	26	30		W	2
Line hum suppression[2] f_R = 100 Hz; V_R = 0.5 V	a_{hum}	40	46		dB	1
Current consumption $P_9 = P_1$ = 15 W; f_I = 1 kHz	I_5		1.8		A	1
Efficiency $P_9 = P_1$ = 10 W; f_I = 1 kHz	η		70		%	1
Total harmonic distortion $P_{9/1}$ = 0.05 – 10 W f_I = 40 Hz to 15 kHz	THD		0.2	0.5	%	1
Cross-talk rejection f_I = 1 kHz; P_9 or P_1 = 15 W	a_{cr}		50		dB	1
Transmission range[3]	B	40 Hz to 60 kHz				1

Characteristics (cont'd)
V_S = 25 V; T_C = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Disturbance voltage (B = 30 Hz to 20 kHz) in acc. with DIN 45 405 referred to input[4]	V_d		5		µV	1
Noise voltage (CCIR filter) in acc. with DIN 45 405 referred to input[4]	V_n		15		µVs	1
Difference in transmission measure $P_9 = P_1$ = 10 W f_I = 40 Hz to 20 kHz	ΔG_V			1	dB	1
Voltage gain stereo bridge configuration	 G_V G_V		 30 36		 dB dB	 1 2

[1] S2a (b) open/closed
[2] S1a (b) and S3 in position 2
[3] $P_{9/1}$ = 6 W; –3 dB referred to 1 kHz
[4] S1a (b) in position 2

Circuit Description

The IC contains 2 complete amplifiers and can be used for a wide variety of applications with a minimum of external circuitry.

The TDA 4935 can be applied as stereo amplifier or amplifier in bridge configuration for operating voltages ranging between 8 V and 26 V.

The pre-stages are differential amplifiers with strong negative feedback. Internal frequency compensation in the driver amplifier limits the gain-bandwidth product to 4.5 MHz.

The power output stages are comprised of quasi PNP transistors (small saturation voltage).

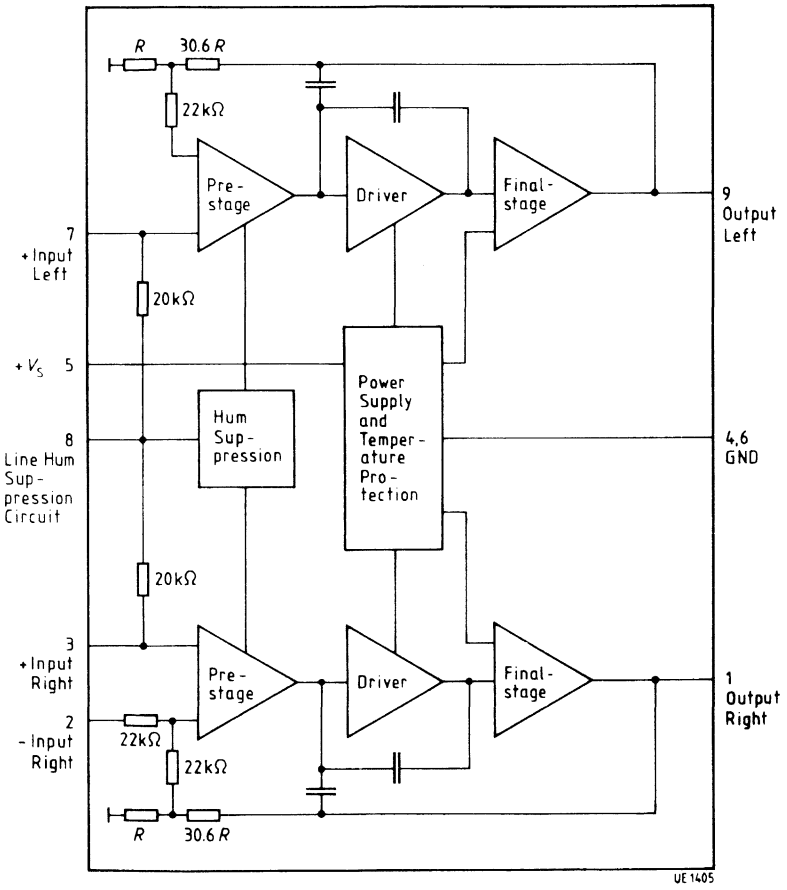
To avoid overheating, a temperature fuse affecting both amplifiers prevents current supply to the power output stages during inadmissibly high chip temperatures.

As a special economic feature, the negative feedback resistances for G_V = 30 dB and the input voltage reference divider have been integrated.

Pin Functions

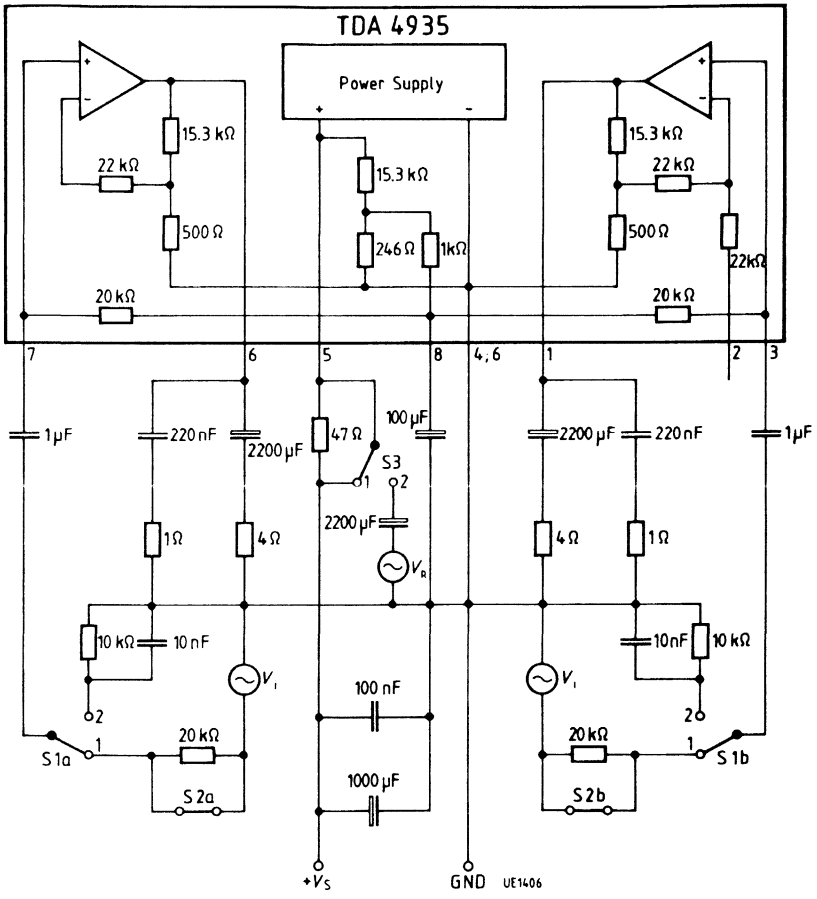
Pin No.	Function
1	Output right channel
2	Inverting input right channel (more than 22 kΩ)
3	Non-inverting input right channel
4	GND
5	$+V_S$
6	GND
7	Non-inverting input left channel
8	Line hum suppression right and left channel
9	Output left channel

Block Diagram



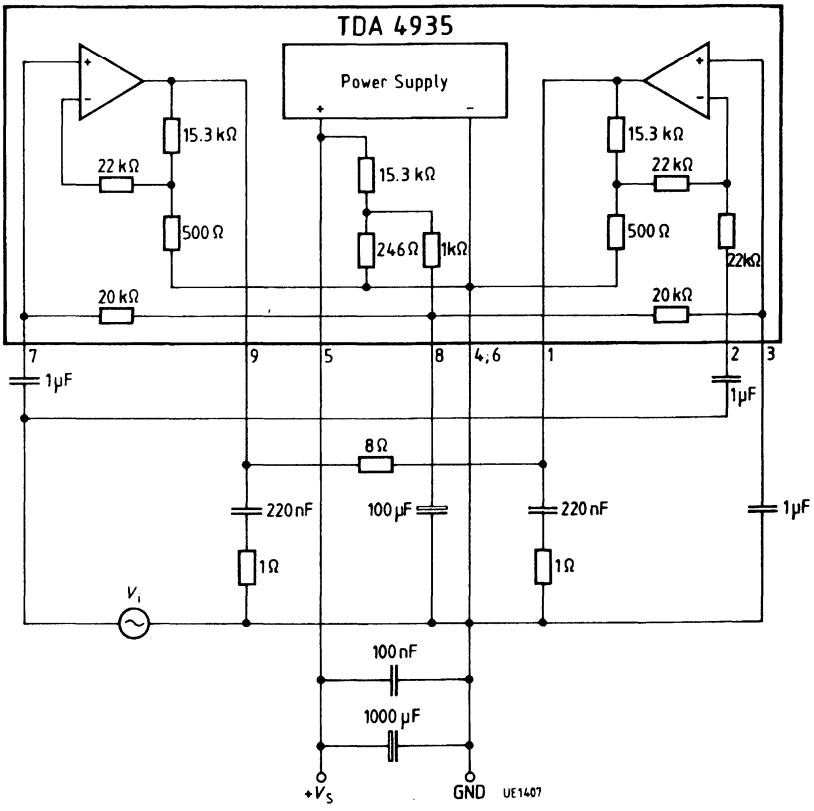
Test Circuit

1. Stereo Operation



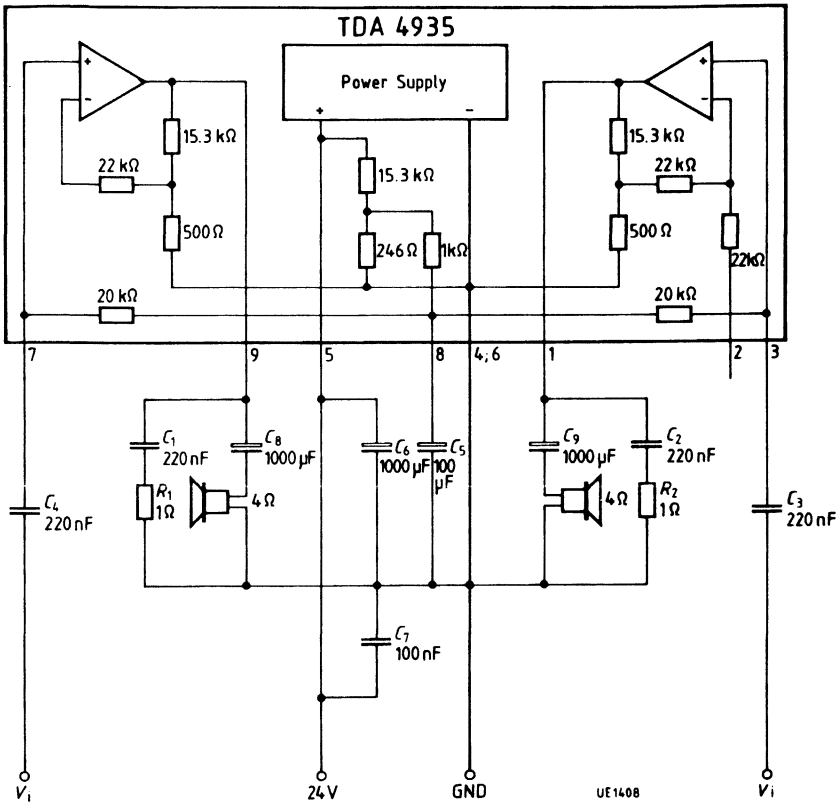
Test Circuit

2. Bridge Operation

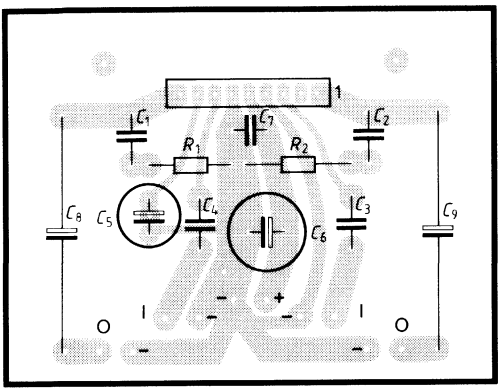


Application Circuit

1. Stereo Operation

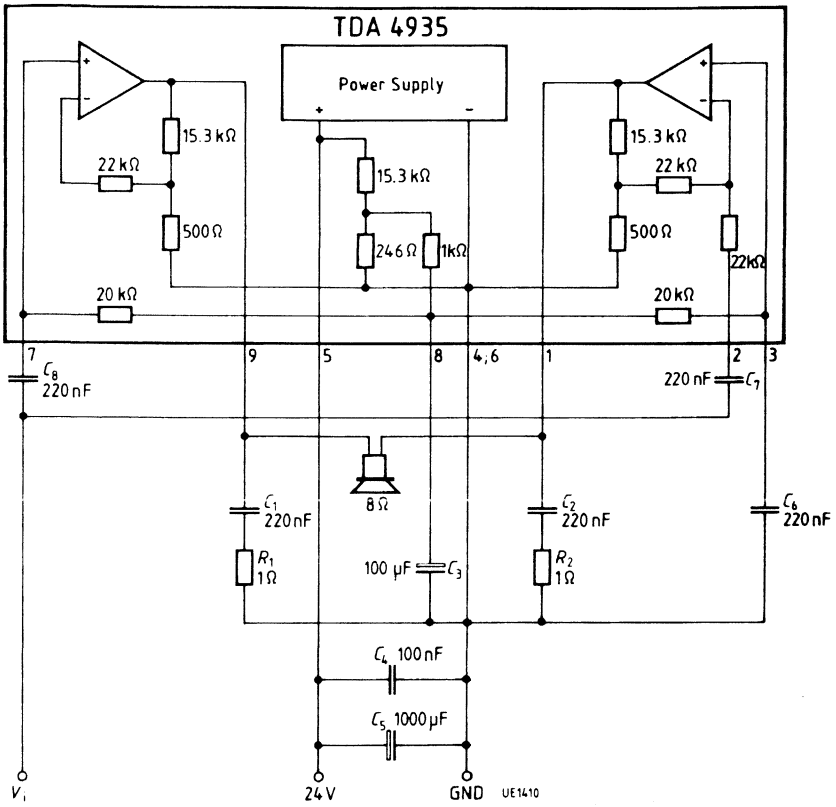


Layout / Plug-in Location Plan

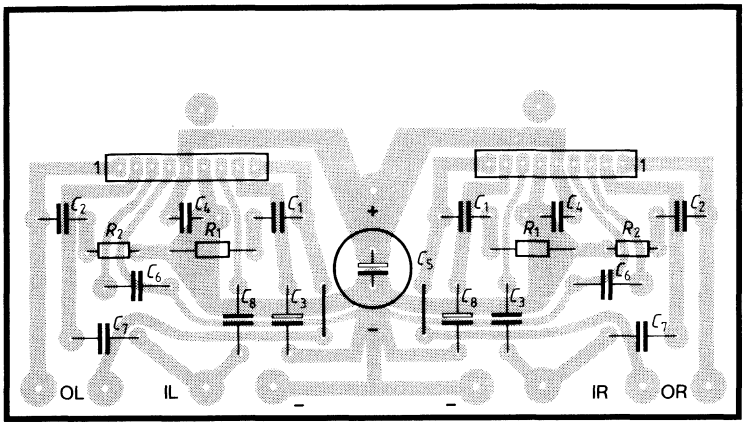


Application Circuit

2. Bridge Operation (one channel only)

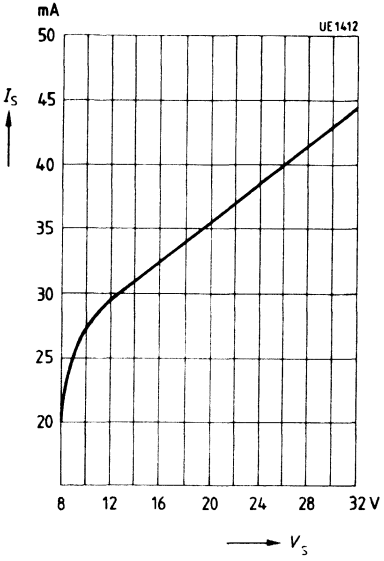


Layout / Plug-in Location Plan



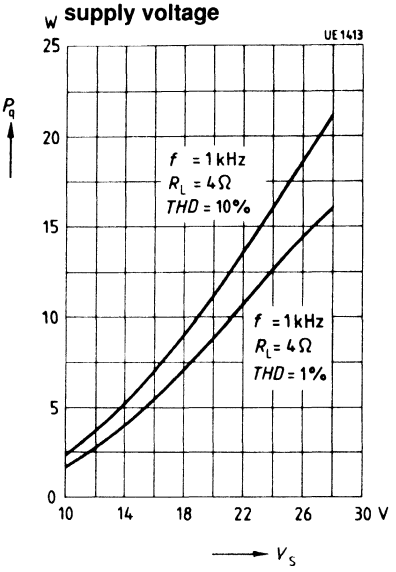
2 x 30W

Quiescent current versus supply voltage



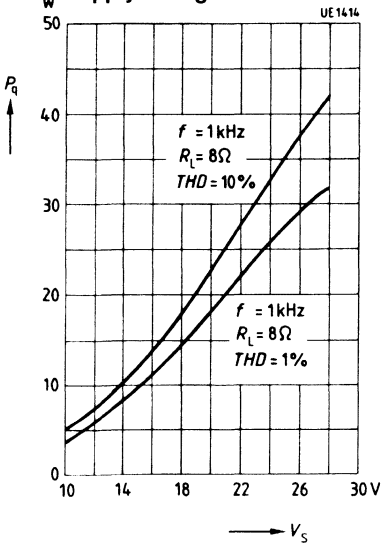
Stereo Operation

Output power versus supply voltage



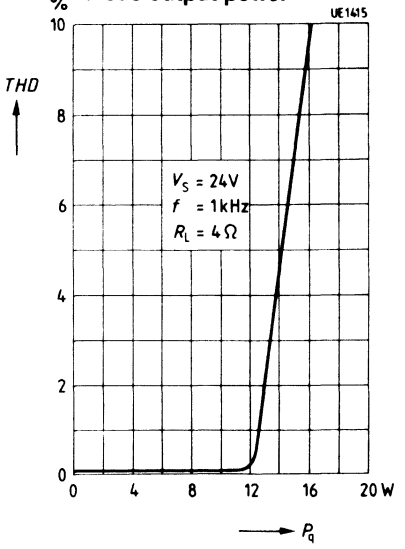
Bridge Operation

Output power versus supply voltage



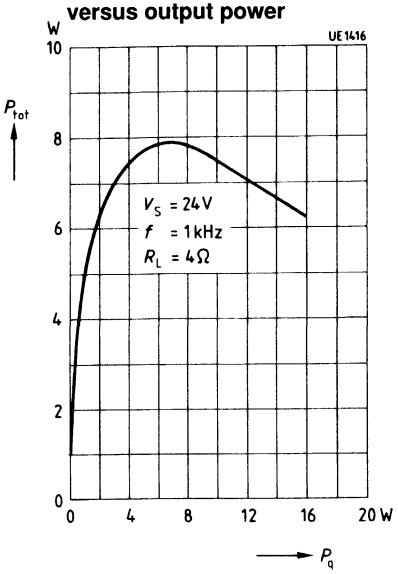
Stereo Operation

Total harmonic distortion versus output power



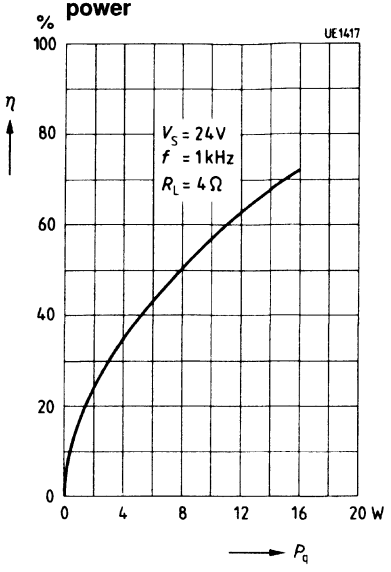
Stereo Operation

Power dissipation (each channel) versus output power



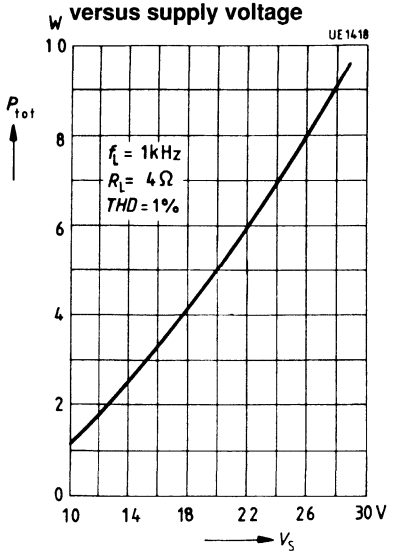
Stereo Operation

Efficiency versus output power



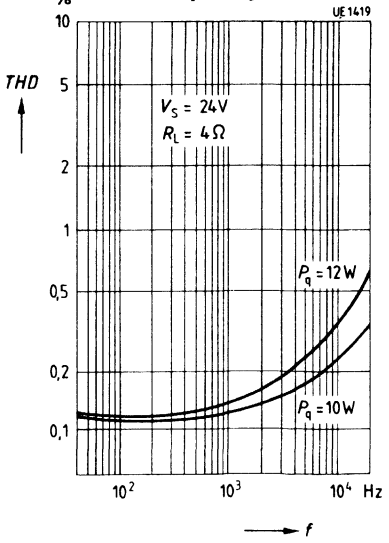
Stereo Operation

Power dissipation (each channel) versus supply voltage



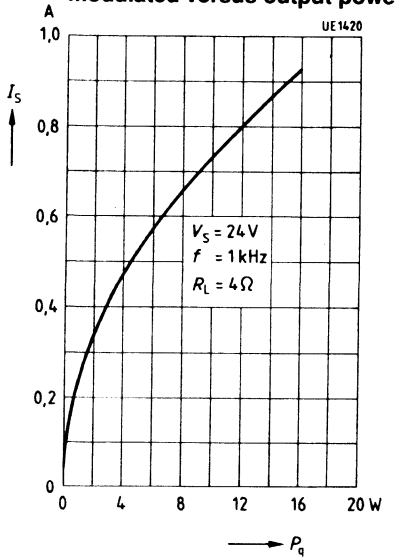
Stereo Operation

Total harmonic distortion versus frequency



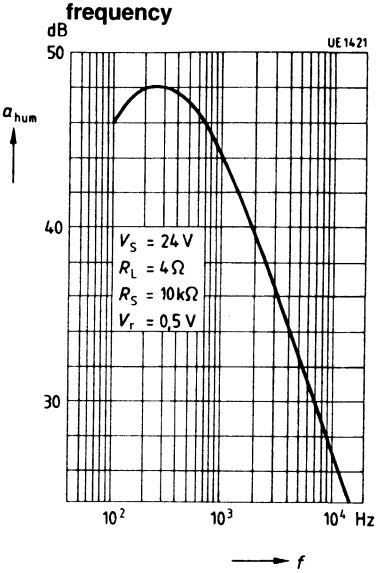
Stereo Operation

Supply current (one channel) modulated versus output power

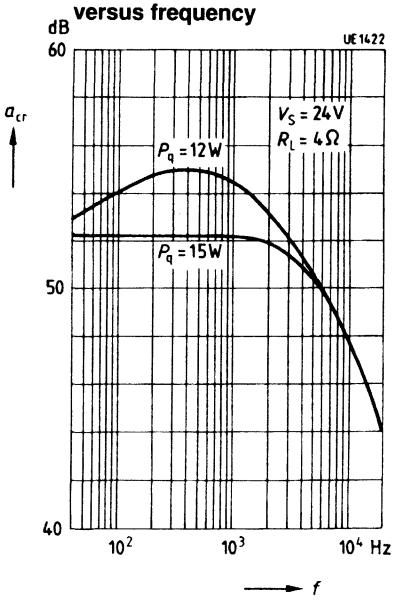


Stereo Operation

Line hum suppression versus frequency



Cross-talk rejection versus frequency



SIEMENS

5 V-Modulator

TDA 5664

Preliminary Data

Bipolar IC

Function

Monolitic integrated circuit for use as a modulator in the 30 to 860 MHz range.

Application

Video recorders, cable converters, cable TV head stations, remodulators, video generators, video security systems, and personal computers.

Features

- Sync level clamping of video input signal
- Clipping of peak white value
- Continuous adjustment of modulation depth for positive or negative values
- Balanced mixer output with separate ground connection
- Balanced RF oscillator with separate ground connection
- Low spurious radiation
- High stability of the RF oscillator frequency
- High stability of the FM sound oscillator
- Internal reference voltage
- 5 V supply voltage

Type	Ordering Code	Package
TDA 5664	Q67000-A8261	P-DIP-14
TDA 5664-X	Q67000-A8265	P-DSO-14

Circuit Description

Via pin 13 the sound signal is capacitively coupled to the AF input of the sound input amplifier. An external circuitry sets the preemphasis. At the output of the sound section the FM-modulated sound signal is added to the video signal and mixed with the oscillator signal in the RF mixer. A parallel resonant circuit is connected to the sound carrier oscillator at pins 1 and 14.

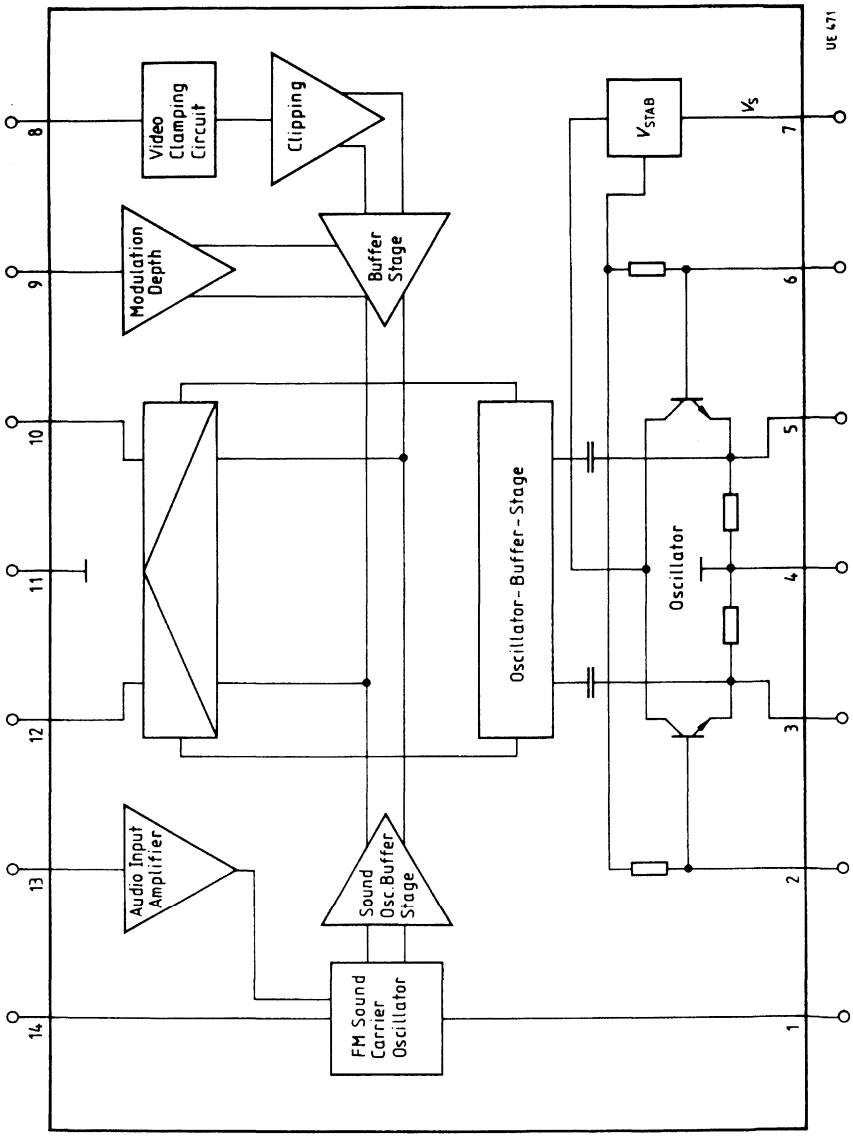
The video signal with a negative synchronous level is capacitively coupled to pin 8. An internal clamping circuit is referenced to the synchronizing level. When the video voltage V_{VSS} exceeds 1 V, the peak white value is clipped. The RF carrier switches from negative to positive video modulation, when pin 9 is connected to ground. By varying the value of resistance R at pin 9 between $\infty....0\,\Omega$ the modulation depth can be increased from 80 % to 100 % when the modulation is negative and decreased from 100 % to 80 % when the modulation is positive.

The amplifier of the RF oscillator is connected to pins 2 – 6. The oscillator operates as a symmetrical Colpitts circuit. The capacitive reactance for the resonance frequency should be $X_C = 70\,\Omega$ between pin 2 and 3 and 5 and 6 and $X_C = 26\,\Omega$ between pins 3,5. The oscillator chip ground, pin 4, should be connected to ground at the resonant circuit shielding point. An external oscillator signal can be injected inductively or capacitively via pins 2 and 6. The layout of the PCB should be such as to provide a optimum shielding attenuation between the oscillator pins 2 – 6 and modulator output pins 10 – 12 of approximately 80 dB.

For optimal residual carrier suppression, the symmetrical mixer outputs at pins 10 – 12 should be connected to a matched balanced-to-unbalanced broadband transformer, e.g. a Guanella transformer with good phase precision at 0 ° and 180 °. The transmission loss should be less than 3 dB. In addition a LC low pass filter combination is required at the output. The cut-off frequency of the LC low pass filter combination must exceed the maximum operating frequency.

If the application circuit 1 is used, the RF voltage at the signal output has to be multiplied by a factor of 1.5 in respect of changing from a balanced (300 Ω) to an unbalanced impedance (75 Ω). The loss of the output transformer is calculated for 0 dB.

Block Diagram



Pin Definitions and Functions

Pin No.	Function	Definition
1	5.5 MHz	Sound carrier oscillator; balanced inputs for tank circuit
2	OSC-Coupling 1	Balanced RF oscillator coupling point
3	OSC-Output 1	Balanced RF output
4	Ground OSC	Oscillator ground
5	OSC-Output 2	Balanced RF output
6	OSC-Coupling 2	Balanced RF oscillator coupling point
7	V_S	Supply voltage
8	Video	Video input with clamping
9	Modulation	Modulation type switch for pos. and neg. modulation and adjustment of modulation depth
10	Output 2	Balanced RF output
11	Ground	Signal and DC ground
12	Output 1	Balanced RF output with opposite phase to pin 10
13	Audio	AF input for FM modulation
14	5.5 MHz	Sound carrier oscillator; balanced inputs for tank circuit

Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.3	7.5	V	
Current at pin 13	V_1	1	4	V	
Current at pin 8	V_{8PP}		1.5	V	only via C_{max} = 1 µF
Current at pin 9	V_9	– 0.3	1.4	V	
Current at pin 10	V_{10}		6	V	
Current at pin 12	V_{12}		6	V	
According to the application circuit 1, only the provided circuitry can be connected to pins 1, 2, 3, 5, 6 and 14.					
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	– 40	125	°C	
Thermal resistance	$R_{Th\,SA}$		83	k/W	

Operating Range

Supply voltage	V_S	4.5	5.5	V	
Video input frequency	f_{Vid}	0	6	MHz	
Audio input frequency	f_{AF}	0	20	kHz	
Output frequency	f_O	30	860	MHz	depending on the oscillator circuitry at pins 2 – 6
Ambient temperature	T_A	0	70	°C	
Sound oscillator	f_{OSC}	4	7	MHz	

Characteristics
V_S = 5 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Current consumption	I_7	15	21	29	mA		
Current consumption	I_{10+12}	1.6	2.2	2.8	mA		1
Oscillator frequency range	f_{OSC}	30		860	MHz	external circuitry adjusted to frequency	1
Switch-on, warm-up drift of oscillator frequency	Δf_{OSC}	0 0	– 50 – 200	– 500 – 500	kHz kHz	Ch 30 Ch 40 TC value of capacitor in osc. circuit is 0; drift is referenced only to self-heating of the IC. t = 0.5–10 s; T_A = const.	1 1
Frequency drift as function of V_S	$-\Delta f_{OSC}$	– 120		120	kHz	V_S = 4.5 – 5.5V T_A = const. Ch 40	1
Video input voltage at pin 8	V_8	0	1	1.4	Vpp	at coupling capacitor $C \leq 1$ µF $I_{Leck} \leq \pm 0.3$ µA	2
Modulation depth	$m_{D/N}$ $m_{D/P}$	70 70	80 80	90 90	% %	neg. mod. pos.mod. Pin 9 at ground V_{Vid} = 1 Vpp	2
Output impedance	Z_{10}; Z_{12}	8			kΩ	static	3
RF output voltage	$V_{Q\,rms}$	2.5	4	5.5	mV	Ch 40; Pin 9 open	1
Output capacitance	$C_{10} = C_{12}$	0.5	1	2.0	pF		
RF output phase	$a_{10,12}$	140	180	220	deg.		
RF output voltage deviation	ΔV_Q	0		1.5	dB	f = 543.25 – 623.25 MHz Δf = 80 MHz Ch 30 ... Ch 40	1
RF output voltage deviation	ΔV_Q	0		1.5	dB	f = 100 – 300 MHz	4
RF output voltage deviation	ΔV_Q	0		1.5	dB	f = 48 – 100 MHz	4

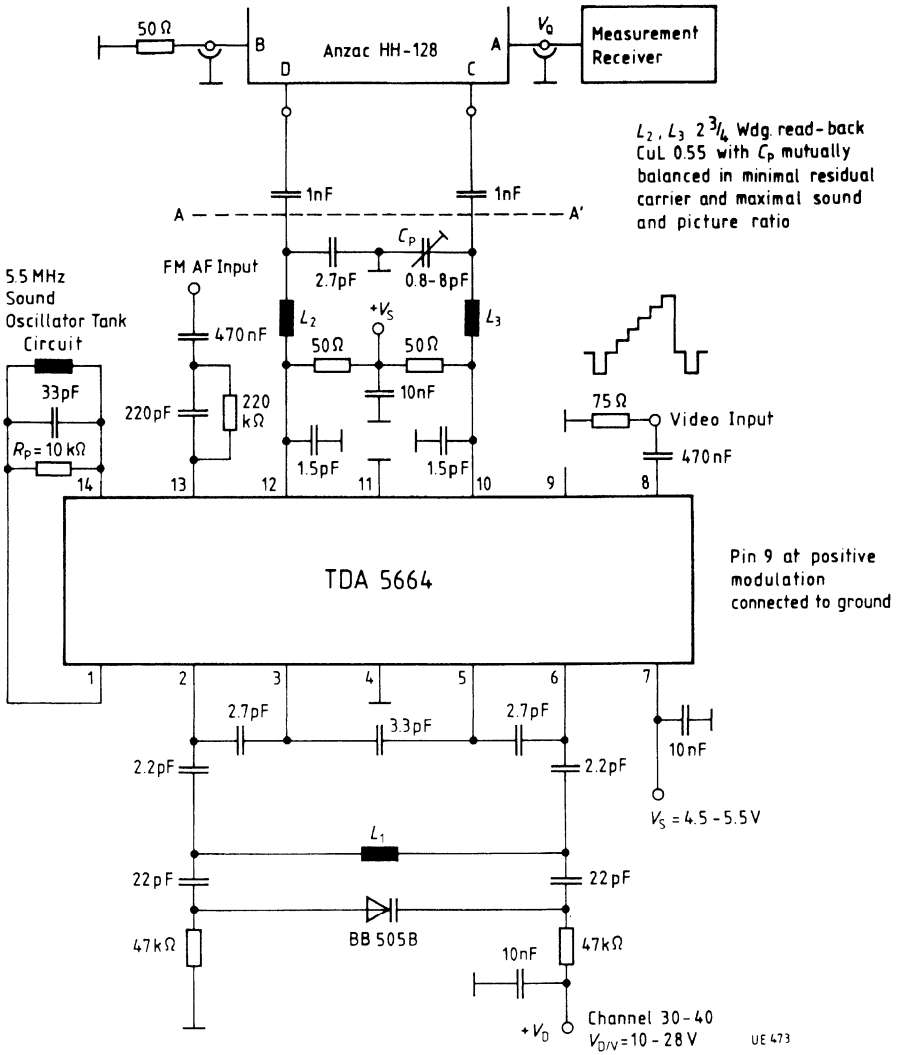
Characteristics
V_S = 5 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Intermodulation ratio	a_{IMA}	53	58		dB	f_P + 1.07 MHz	5
Harmonic wave ratio	a_O	40	46		dB	f_P + 8.8 MHz without vid.sig.	5
Harmonic wave ratio	a_O	35	58		dB	Unmodulated video and sound carrier, measured with the spectrum analyser as difference between video carrier signal level and sideband signal level, R_P = 10 kΩ	1; diagram 2
Harmonic wave ratio	a_O	42	60		dB		1; diagram 2
Sound carrier range	$a_{P/S}$	10	12.5	15	dB		1; diagram 2
All remaining harmonic waves	a_{VC}	15			dB	Multiple of fundamental wave of picture carrier, without video signal, measured with spectrum analyser; f_{VC} = 543.25–623.25 MHz	1
Amplitude response of video signal	a_V			1.5	dB	V_{Vid} = 1 V_{pp} with additional modulation f = 15 kHz–5 MHz sine wave signal between black and white	5
Residual carrier suppression	a_R	26			dB	Ch 30 ... Ch 40	9
Stability of modulation depth	Δm_T		± 3	± 10	%	staircase signal at Video input ΔV_{Vid} = 1 V_{pp}; Ch 30 ... Ch 40; V_S = 5V; T_A = const.	2
	Δm_T		± 1	± 3	%	V_S = 4.5–5.5 V; T_A = const. ΔV_{Vid} = 1 V_{pp}	2

Characteristics
V_S = 5 V; T_A = 25 °C

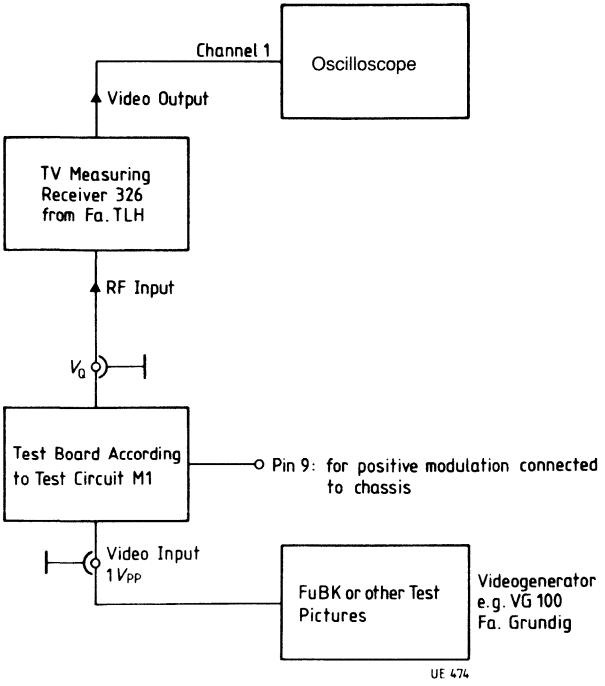
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Interference product ratio sound in video	$a_{S/P}$	48	88		dB	FM modulation of sound carrier; Ch 30 ... Ch 40	6
Signal-to-noise in video	$a_{N/P}$	48	90		dB	Unmodulated sound carrier; Ch 30 ... Ch 40	6
Unweighted FM noise level ratio in video sound	$a_{P/S}$	45	50		dB	FuBK – test picture as video signal; V_{Vid} = 1 Vpp Ch 30 ... Ch 40	7
Signal-to-noise in sound	$a_{N/S}$	48	52		dB	Unmodulated sound carrier	7
Differential gain Differential phase	 a_{dif} Φ_{dif}		 1 2	 10 15	 % deg.	Measured with test demodulator, video test signals and vector scope V_{Vid} = 1 Vpp V_{Vid} = 1 Vpp	 1 1
Sound oscillator frequency range	$f_{S/OSC}$	4		7	MHz	Unloaded Q factor of resonant circuit Q_u = 8 resonance frequency 5.5 MHz	1
Switch-on, warm-up drift of oscillator frequency	$\Delta f_{S/OSC}$		5	15	kHz	T_A = const.; TC value of capacitor in sound oscillator circuit is 0; the drift is only based on self-heating of the IC; $f_{S/OSC}$ = 5.5 MHz	1
Sound oscillator frequency deviation	$\Delta f_{S/OSC}$		5	15	kHz	V_S = 4.5–5.5 V; $f_{S/OSC}$ = 5.5 MHz; T_A = const.; Q_u = 8	1
FM modulation harmonic distortion	THD_{FM}		0.6	1.5	%	V_{1rms} 634 mV	8
Audio preamplifier input impedance (dynamic)	Z_{13}	15	22	29	kΩ		1
FM sound modulation (static)	$\Delta f_{S/OSC}$	±350	±450	±540	kHz	$\Delta V_{1/2} = V_1 - V_2 = \pm 1$ V; $f_{S/OSC}$ = 5.5 MHz; Q_u = 8	1
FM sound modulation (dynamic)	$\Delta fs/\Delta V_1$	0.7	0.93	1.1	kHz/mV		1

Test Circuit 1 for FM Sound Carrier and Negative Video Modulation



Test Circuit 2

Measuring of the Modulation Depth for Positive and Negative Modulation



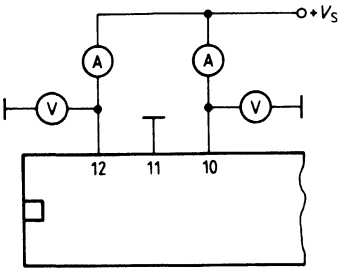
Calibration: A zero reference signal with the TV measuring receiver is given to the video signal. A video signal with V_{Vid} = 1 V_{pp} is connected to the video input.

Measurement: 1) Modulation depth $m_{D/N}$ for negative modulation: Pin 9 open, range peak white value – sync level in relation to range zero reference – sync level gives $m_{D/N}$.

2) Modulation depth $m_{D/P}$ for positive modulation. Pin 9 to ground, range peak white value – sync level in relation to range zero reference – peak white value gives $m_{D/P}$.

Test Circuit 3

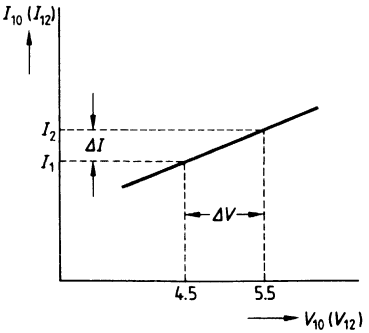
Measurement of the Static Output Frequency



UE 475

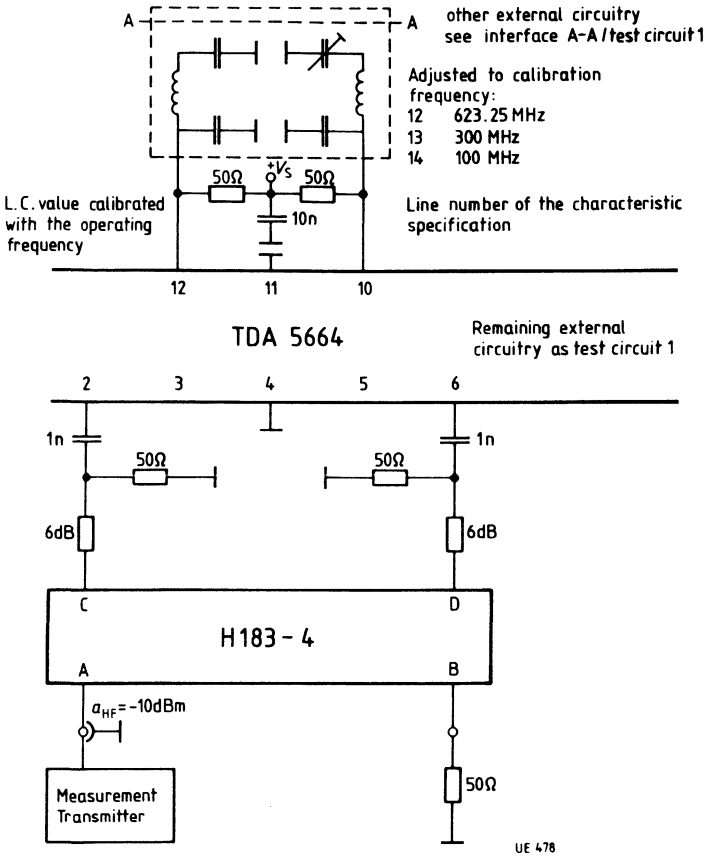
$$Z_{12} = \frac{\Delta V_{12}}{\Delta I_{12}}$$

$$Z_{10} = \frac{\Delta V_{10}}{\Delta I_{10}}$$



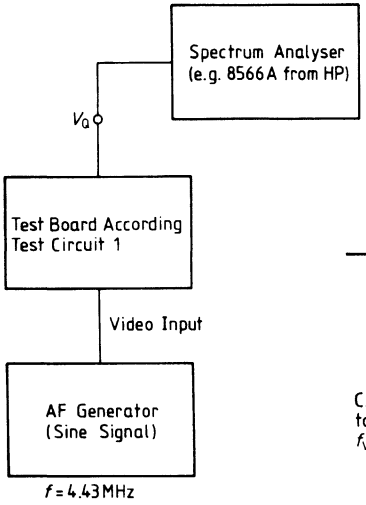
UE 476

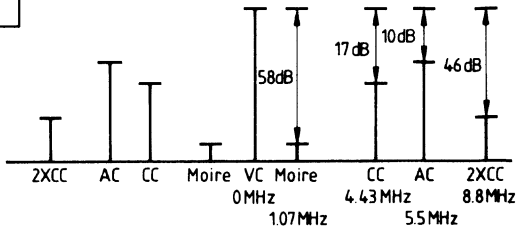
Test Circuit 4



Test Circuit 5

Measurement Configuration to Measure the 1.07 MHz Moires



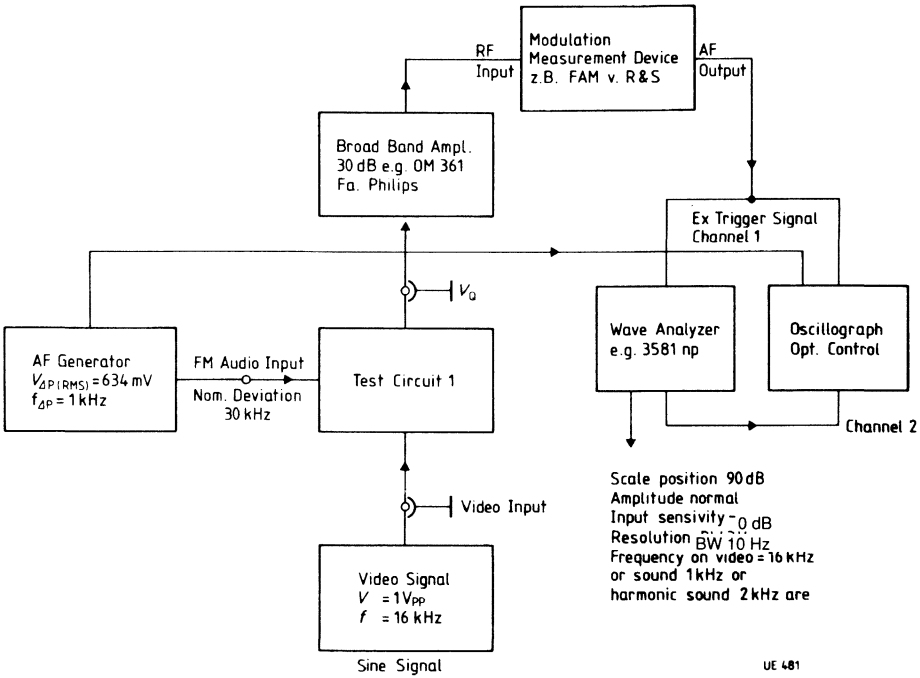


C.C. level lies below the activation point and has been set to provide a ratio of 17dB with respect to the video carrier.
f_{VC} = 623.25 MHz

UE 479

Test Circuit 6

Measurement Configuration to Measure the Audio and/or Noise in Video during FM Modulation of the Sound Carrier



Calibration: AF signals are switched off, video signal is present at video input, modulation measurement device set at AM is adjusted to video carrier; filter: 300 Hz ... 20 kHz; detector: (P + P)/2; wave analyzer at video signal level (16 kHz) adjusted and resultant level as reference a_V defined.

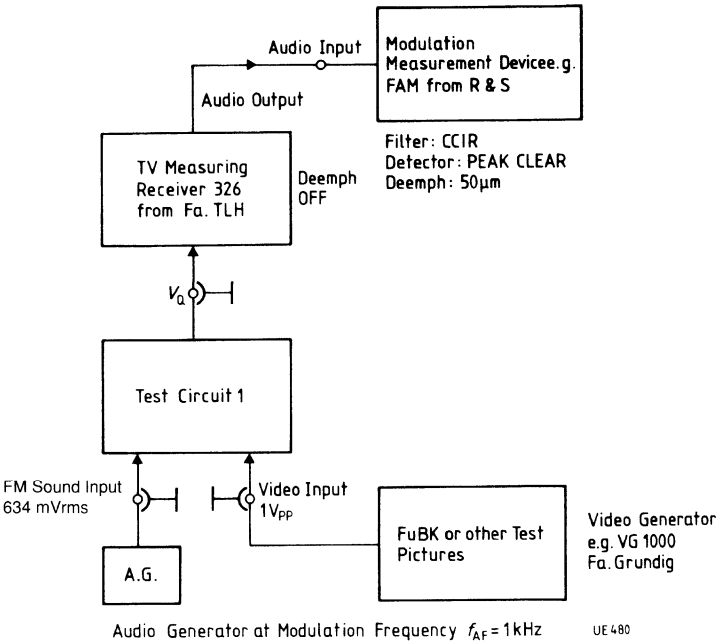
1) Measurement of audio interference product ratio in video during FM modulation of the sound carrier: AF signal is connected to FM audio input; modulation measurement device set at AM; filter: 300 Hz ... 20 kHz; detector: (P + P)/2; the automatic RF level position of the measurement device is switched off; wave analyzer at video signal level 1 kHz or 2 kHz or 3 kHz adjusted and resultant level is set to a_S. The audio noise ratio in video results from $a_{S/P} = a_S - a_V$ (dB).

2) Measurement of signal-to-noise ratio in video without AM/FM modulation of sound carrier: AF signals are switched off; video signal is switched off; modulation measurement device set at AM; filter: 300 Hz ... 3 kHz; detector: RMS·√2; read out in dB to reference level of calibration is $a_{N/P}$.

3) The noise limit of the measurement device is approx. 85 dB.

Test Circuit 7

Measurement Configuration to Measure the Video and/or Noise in Sound



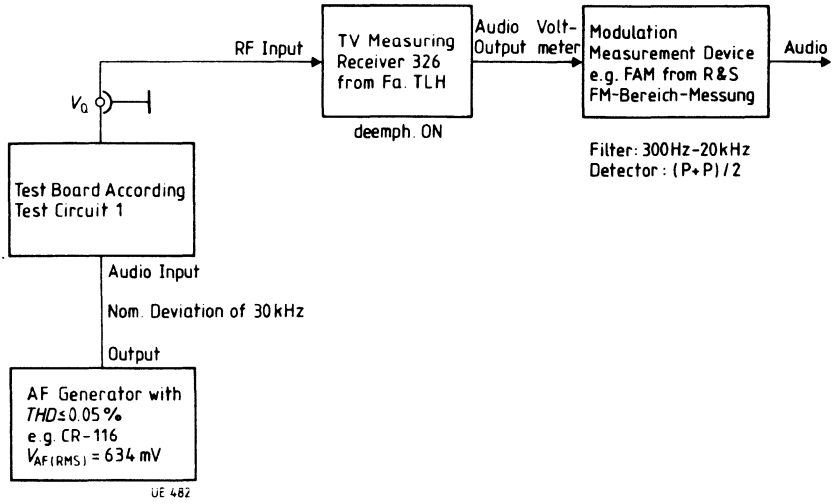
Calibration: A signal of V_{AM} = 634 mV $_{rms}$ and f = 1 kHz, corresponding to a nominal deviation of 30 kHz, is connected to the audio input, and the demodulated AF reference level at the audio measurement device is defined as 0 dB. No video signal is present.

Measurement: 1) The AF signal is switched off and the FuBK video signal is connected to the video input with V_{Vid} = 1 Vpp. The audio level in relation to the reference calibration level is measured as ratio $a_{P/S}$ = 20 log (V_{Video}) / ($V_{nom.}$).

2) AF and video signal are switched off. The noise ratio in relation to the AF reference calibration level is measured as signal-to-noise ratio $a_{S/N}$.

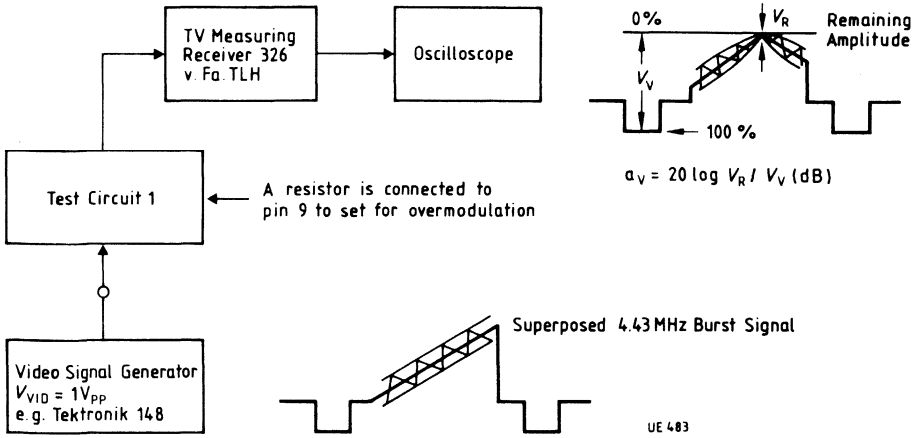
Test Circuit 8

Measurement Configuration to Measure the Harmonic Distortion Factor during FM Operation of the Sound Carrier

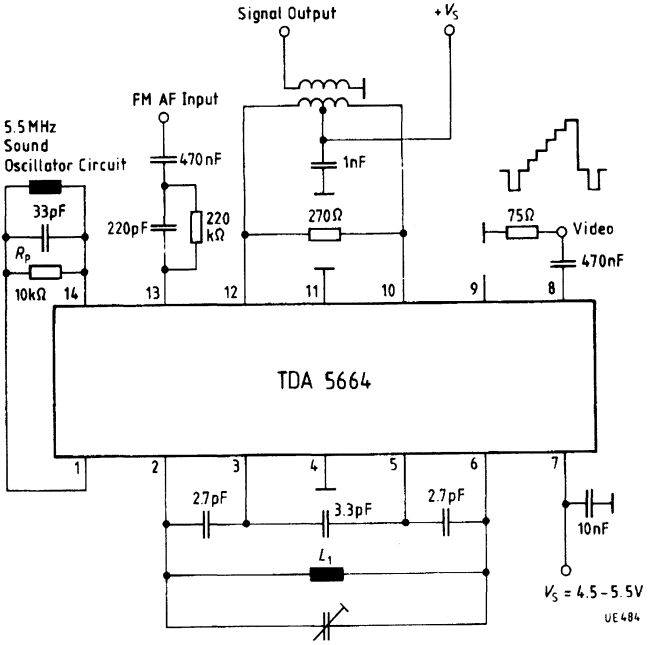


Test Circuit 9

Measurement Configuration to Measure the Residual Carrier Suppression

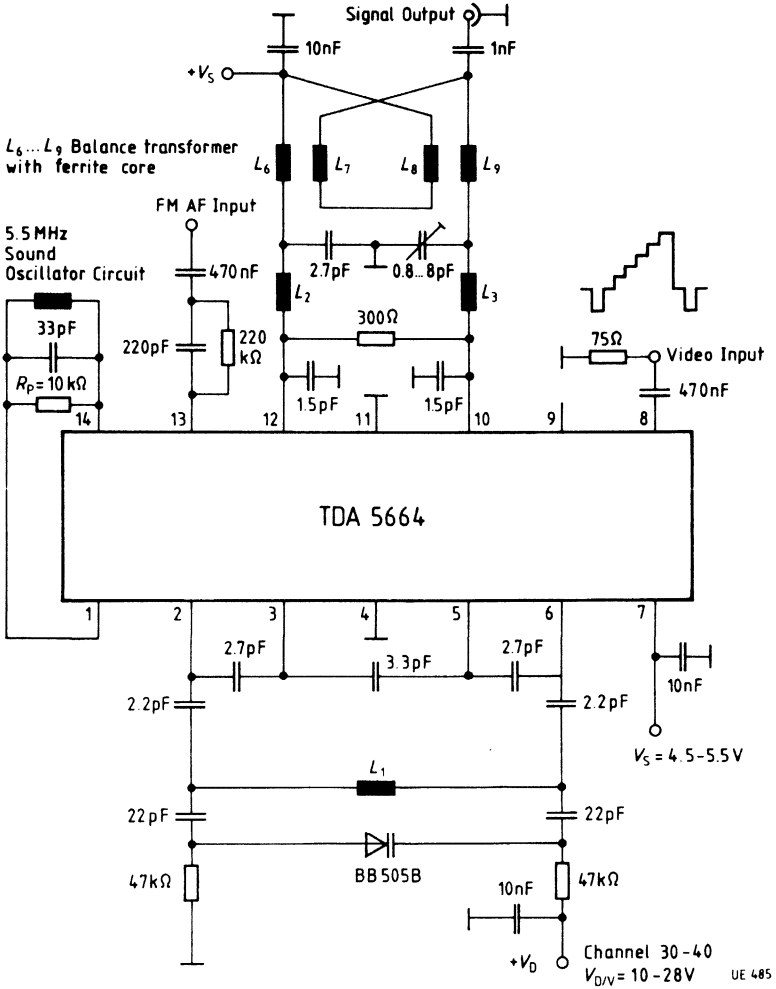


Application Circuit 1



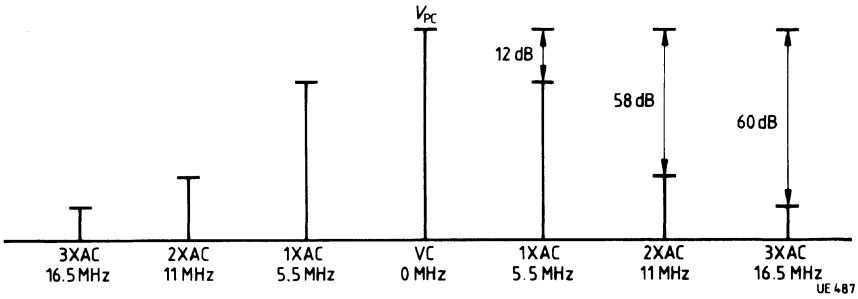
Application Circuit 2

Application with a Very Good Residual Carrier Suppression



Display of the Frequency Spectrum

- Measured at clamp V_{O} with spectrum analyser
- Video and audio unmodulated



SIEMENS

Video IF IC with VTR Connection and Quasi-Parallel Sound

TDA 5830-2

Bipolar IC

Video IF Section

Controlled AM broadband amplifier with synchronous demodulator, video amplifier, VTR input and output, and AGC voltage generation for the video IF amplifier and tuner.

Quasi-Parallel Sound Section

Controlled AM broadband amplifier with quadrature demodulator, sound carrier output, and internal AGC voltage generation.

The TDA 5830-2 is especially suitable for application with black and white or color television receivers and/or VTR systems with PNP/MOS tuners for TV standards with negative video modulation and FM sound.

Type	Ordering Code	Package
TDA 5830-2	Q67000-A2504	P-DIP-22

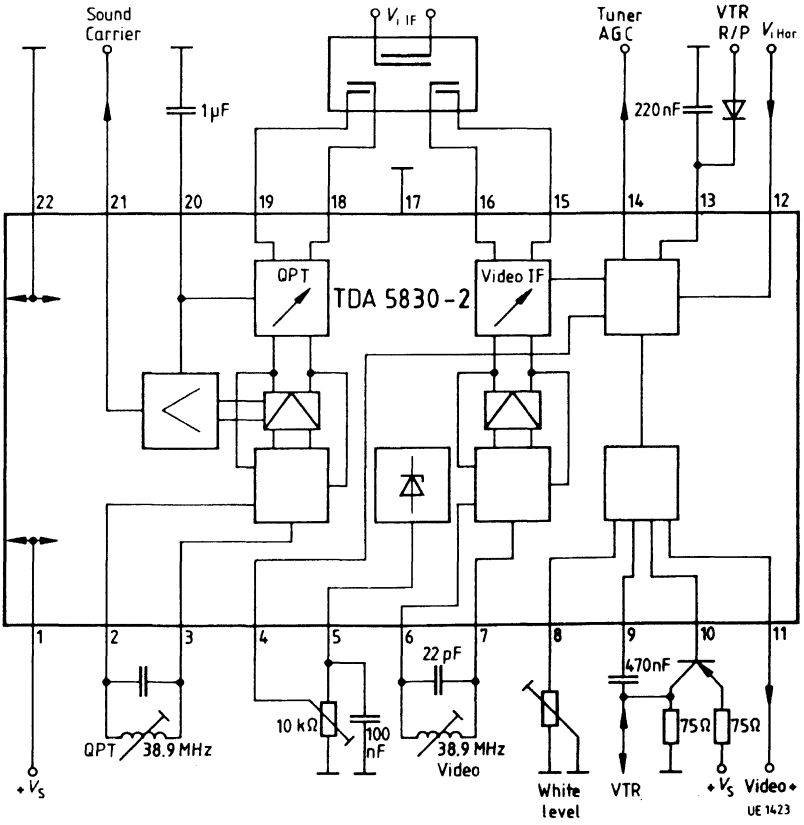
Circuit Description

The video IF section is comprised of a 4-stage controllable AM amplifier, a limiter, and a mixer for the synchronous demodulation of video signals as well as an amplifier for the positive video output signal.

The positive video signal is used for gated control. In addition, the IC includes a standard VTR connection via an external transistor. The delayed tuner AGC is generated by a threshold amplifier driven by the control voltage.

The quasi-parallel sound section also includes a 4-stage AM amplifier, a limiter, and a mixer for the quadrature demodulation of the 1st sound IF with subsequent sound carrier output for the 2nd sound IF. The control voltage is generated by a peak value rectifier from the 1st sound IF signal.

Block Diagram



Pin Functions

Pin No.	Function
1	Supply voltage
2	Demodulator tank circuit QPS
3	Demodulator tank circuit QPS
4	Tuner AGC threshold
5	Reference voltage
6	Demodulator tank circuit video IF
7	Demodulator tank circuit video IF
8	White level setting
9	VTR input
10	VTR output
11	Video output
12	Gating pulse input
13	AGC time constant video IF
14	Delayed tuner AGC
15	Video IF input
16	Video IF input
17	GND
18	QPS IF input
19	QPS IF input
20	AGC time constant QPS
21	Sound carrier output
22	GND

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_1		13	V
Max. DC voltage	$V_{2,3}$	V_5	V_1	V
Max. DC voltage	V_4	0	V_1	V
Max. DC current	I_5	– 2	2	mA
Max. DC voltage	$V_{6,7}$	V_5	V_1	V
Max. DC voltage	$V_{8,9}$	0	V_1	V
Max. DC current	I_{10}	– 1	3	mA
Max. DC current	$-I_{11}$	– 1	3	mA
Max. DC voltage	V_{12}	– 10	V_1	V
Max. DC voltage	$V_{13,14}$	0	V_1	V
Max. DC voltage	$V_{15,16}$	0	V_1	V
Max. DC voltage	$V_{18,19,20}$	0	V_1	V
Max. DC current	I_{21}	– 1	2	mA
Junction temperature	T_j		150	°C
Storage temperature range	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		55	K/W

Operating Range

Supply voltage	V_S	10.5	12.6	V
IF frequency	f_{IF}	15	75	MHz
Ambient temperature	T_A	0	70	°C

Characteristics

V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_1		95		mA	
Stab. reference voltage	$V_{5/22}$		6.7	7.0	V	
Video IF						
Control current for tuner	I_{14}		4.5		mA	
Tuner AGC threshold	$V_{4/22}$	0		4.0	V	
Gating pulse voltage	V_{12} V_{12}	4.0 – 10		V_1 – 4.0	V V	pos. gating pulse neg. gate pulse
Input voltage at Gmax	$V_{I\,15/16}$		30	60	µV	$V_{11\,pp}$ = 3 V
AGC range	ΔG		60		dB	
IF control voltage	$V_{13/22}$ $V_{13/22}$	0		 4.0	V V	Gmax Gmin
Video output voltage	$V_{Q\,11\,pp}$		3.0		V	$R_L = \infty$
Sync pulse level	$V_{11/22}$		2.0		V	
DC voltage V_{13} = 4 V; $V_{15/16}$ = 0 V	$V_{11/22}$		5.3		V	
Output current	$I_{Q\,11}$ $I_{Q\,11}$		– 5.0 2.0		mA mA	to ground via R to plus V_{11} = 7 V
VTR output voltage (neg.)	$V_{Q10\,pp}$		2.0		V	VTR record. $R_L = \infty$
Sync pulse level	$V_{10/22}$		V_1–1.6		V	VTR record. $R_L = \infty$
DC voltage $V_{13} \leq 5$ V; $V_{15/16}$ = 0 V	$V_{10/22}$		V_1–3.8		V	VTR recording
DC voltage V_{13} = 8 V	$V_{10/22}$		V_1–0.9		V	VTR playback
Output current	$I_{Q\,10}$ $I_{Q\,10}$		–5.0 1.0		mA mA	to ground via R to plus $V_{10} = V_1$
Video amplifier (VTR playback)	V_{video}		3.0			$V = V_{11}/V_9$; $V_{9\,pp}$ = 1 V
Quasi-Parallel Sound						
Sound carrier output voltage	V_{21}	10			mV	$V_{I\,VC}$ = 1 mV $V_{I\,SC}$ = 300 µV
Input voltage at Gmax	$V_{I\,18/19}$		50	100	µV	$V_{21} = V_{21}$ -3 dB
AGC range	ΔG		60		dB	$V_{21} = V_{21}$ ±3 dB
Signal-to-noise-ratio						IEC 468
White/staircase signal			61		dB	Peak weighting
Black picture			66		dB	

Characteristics (cont,d)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Test Conditions						
Video carrier/sound carrier			10		dB	
Modulation frequency			1		kHz	
Frequency deviation			50		kHz	
IF input voltage			20		mV	
Design-Related Characteristics						
Input impedance	$Z_{I\,15/16}$ $Z_{I\,18/19}$		1.8/2 1.8/2		kΩ/pF kΩ/pF	
Output impedance	$Z_{Q\,2/3}$ $Z_{Q\,6/7}$		6.6/2 6.6/2		kΩ/pF kΩ/pF	
Output resistance	R_{11}		150		Ω	
Residual IF (fundamental wave)	V_{11}		10		mV	
Video bandwidth (– 3 dB)	B_{video}		6.0		MHz	
Intermodulation ratio with reference to f_{CC}	α_{IM}		50		dB	sound color interference
Output resistance	$R_{Q\,21}$		200		Ω	
IF control voltage	$V_{20/22}$ $V_{20/22}$	0		 4	V V	G_{max} G_{min}

Alignment Procedures

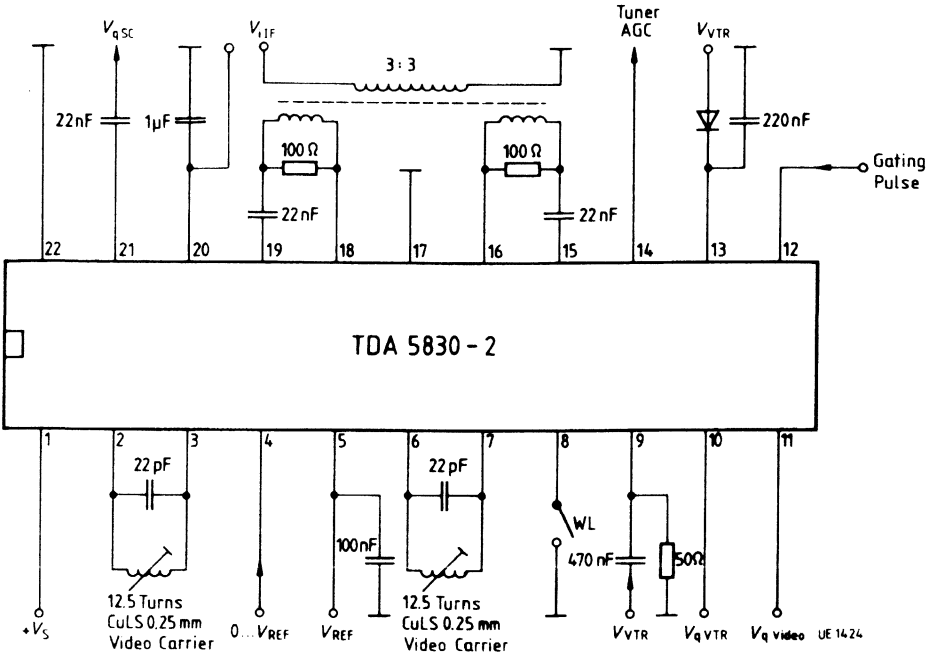
a) Video IF

At a video carrier input level of $V_{15/16\,rms}$ = 10 mV and a superimposed AGC voltage of V_{13} = 3 V, the demodulator tank circuit is preliminary aligned so that the demodulated video signal $V_{11\,pp}$ reaches its maximum output level at the positive video output. Any suitable video test signal can be used for modulation. Subsequently, the AGC voltage V_{13} is reduced until the video signal equals approx. 3 V (peak-to-peak). By fine-aligning the demodulator tank circuit, the maximum output level of the video signal is reached. The flat response characteristic of the demodulator ensures a non-critical alignment procedure.

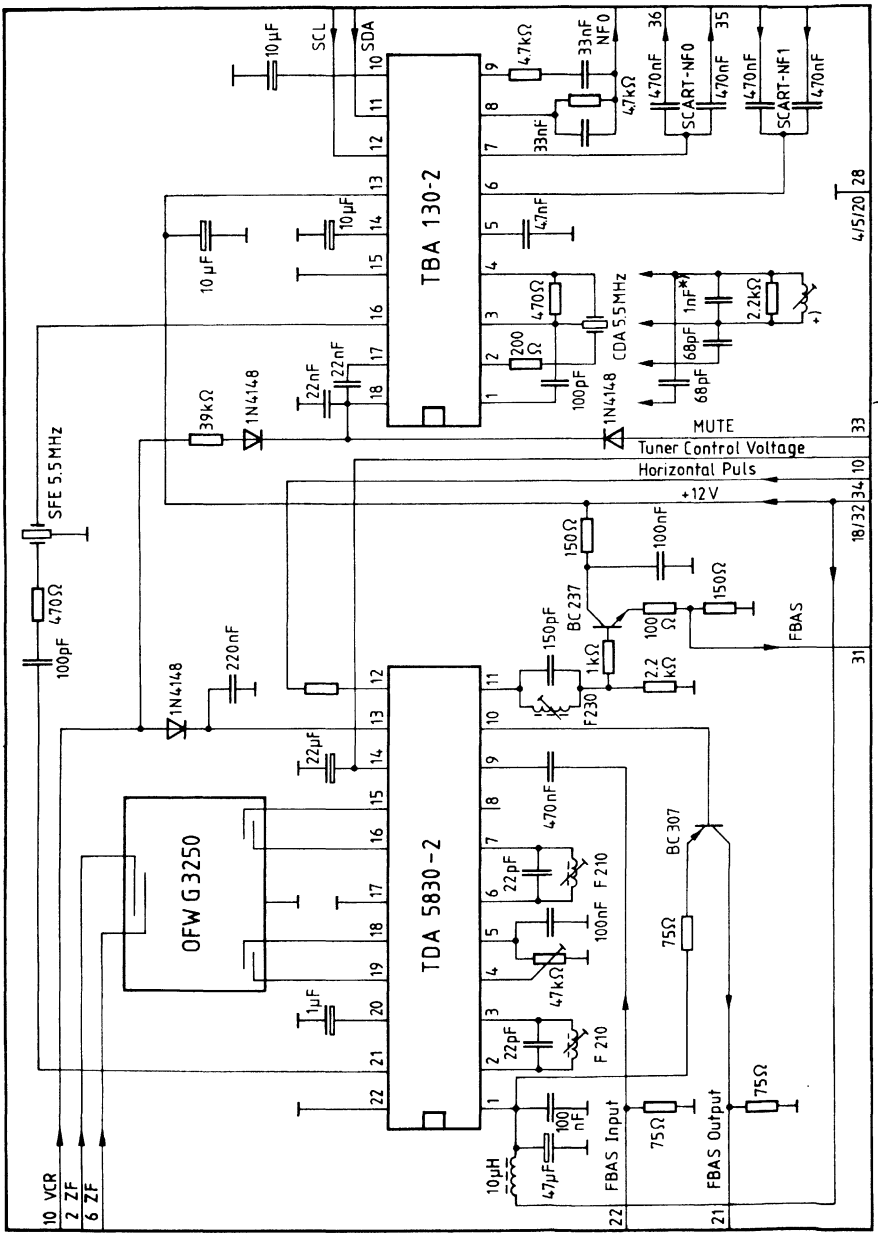
b) QPS

At an input signal of $V_{18/19\,rms}$ = 10 mV, the demodulator tank circuit is preliminarily aligned until a max. AM suppression of the demodulated video signal V_{21} is reached at the sound carrier output. A video signal critical for the sound-interference ratio should be used for modulation (white/staircase, FuBK). Subsequent fine-aligning is performed by measuring the sound-interference ratio at the output of a FM demodulator and fine-aligning the demodulator tank circuit for a max. interference ratio. If several sound carriers are used in a device, the sound carrier with the lowest level should be used for alignment purposes.

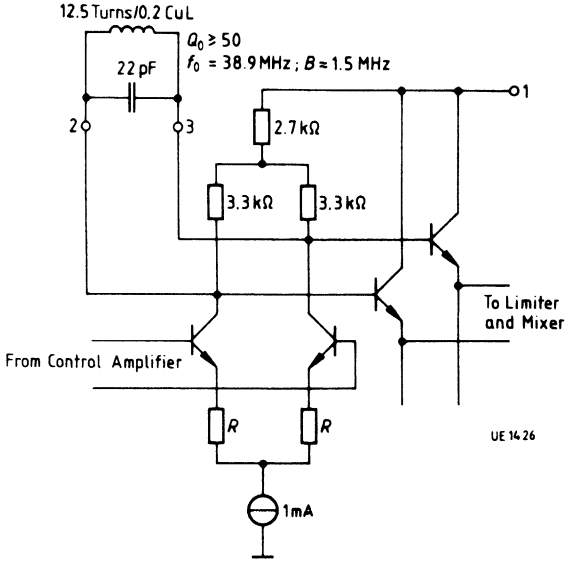
Measurement Circuit



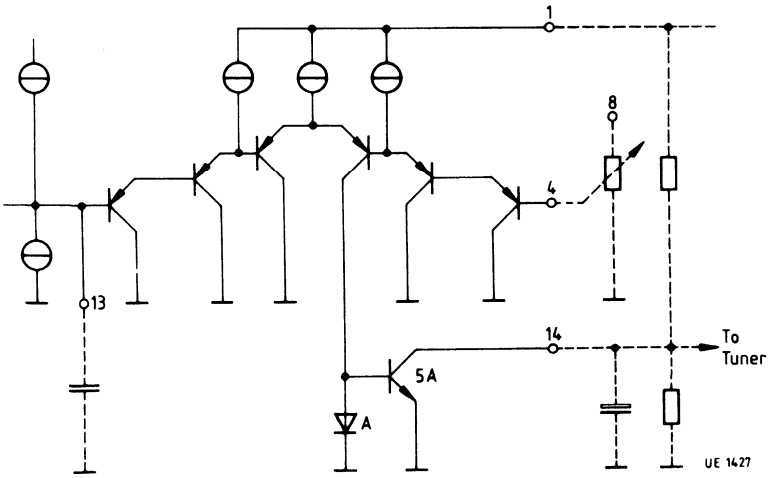
Application Circuit



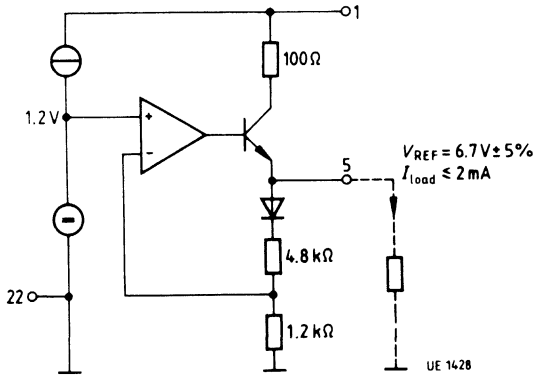
Demodulator Tank Circuit QPS



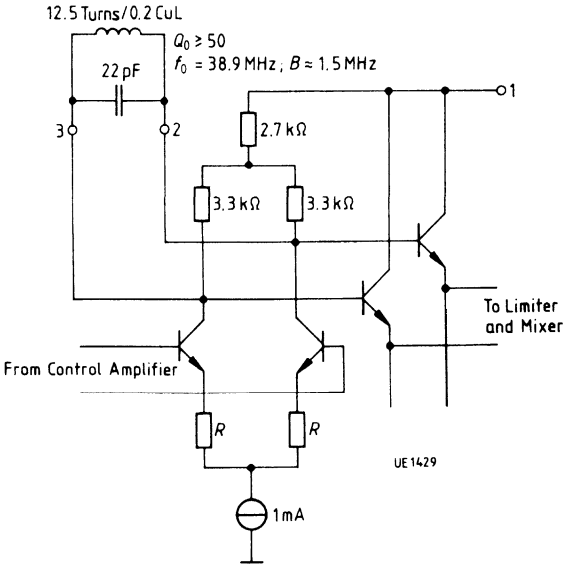
Tuner AGC Threshold and Output



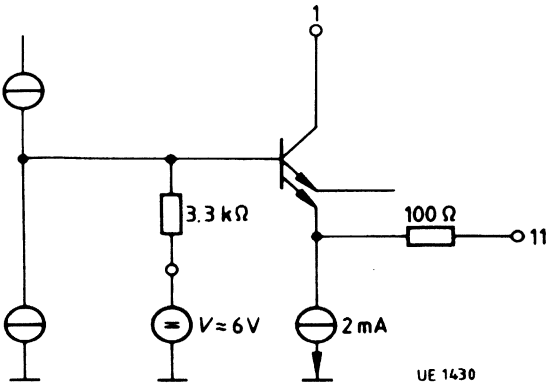
Reference Voltage



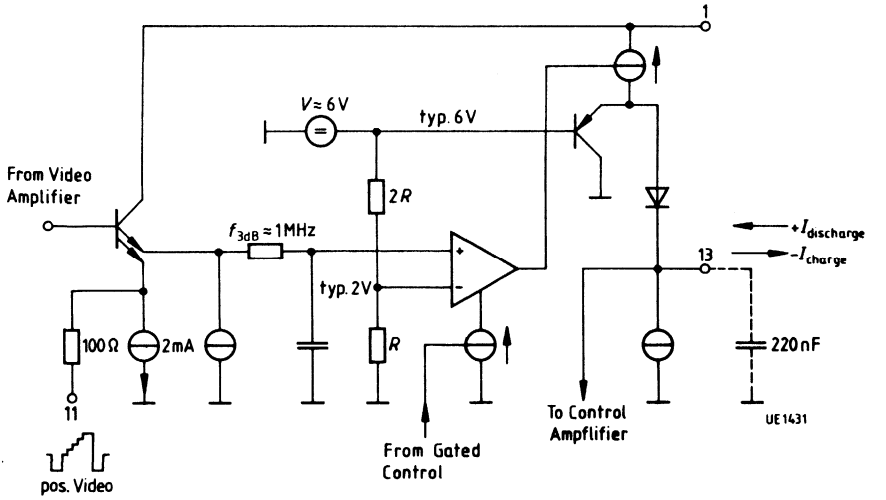
Demodulator Tank Circuit Video IF



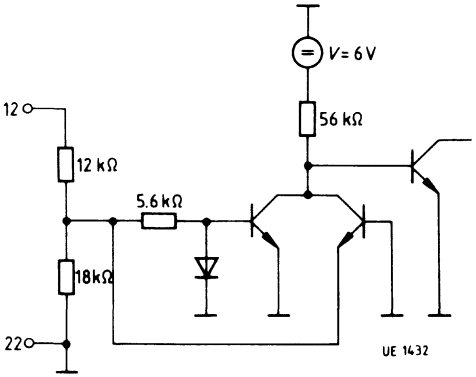
Positive Video Output



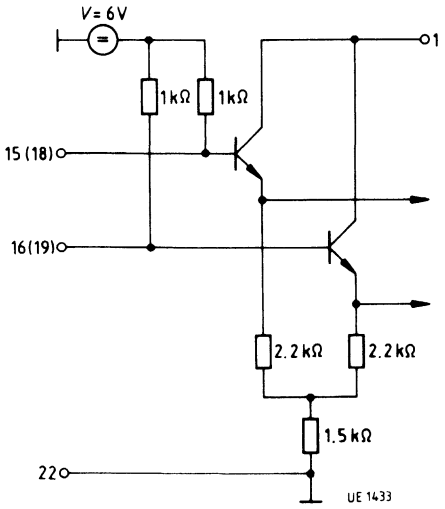
AGC Time Constant Video IF



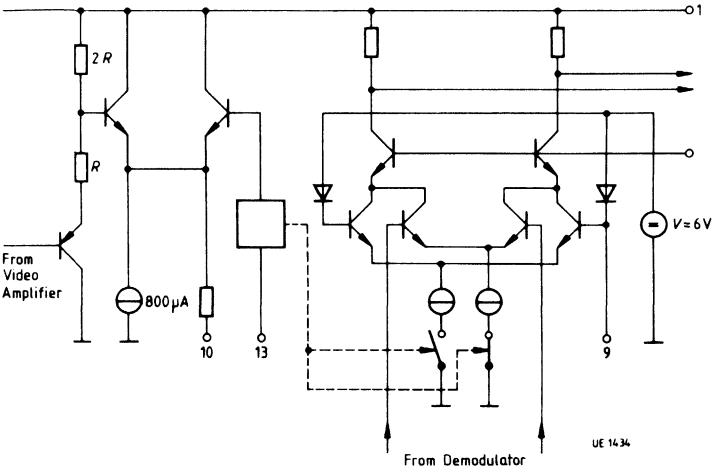
Gating Pulse Input



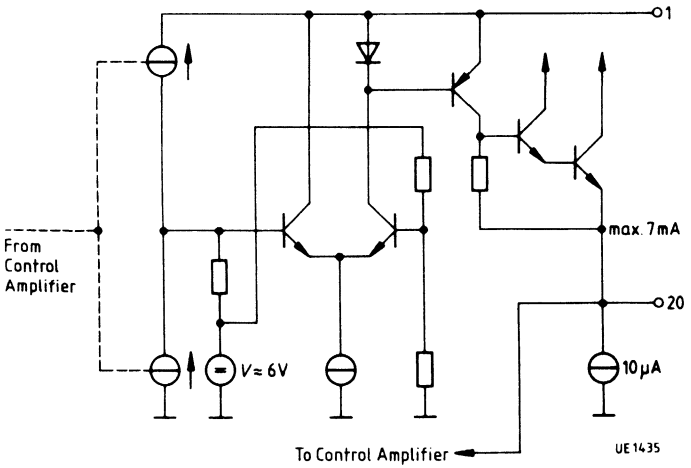
IF Input Video IF
IF Input QPS



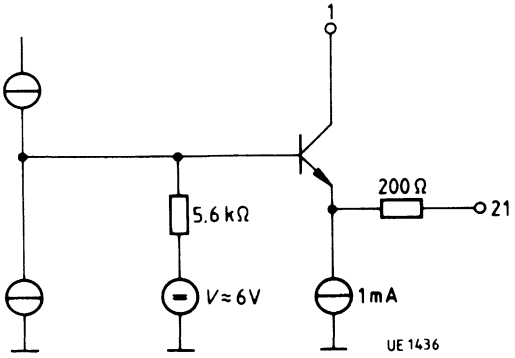
VTR Interface



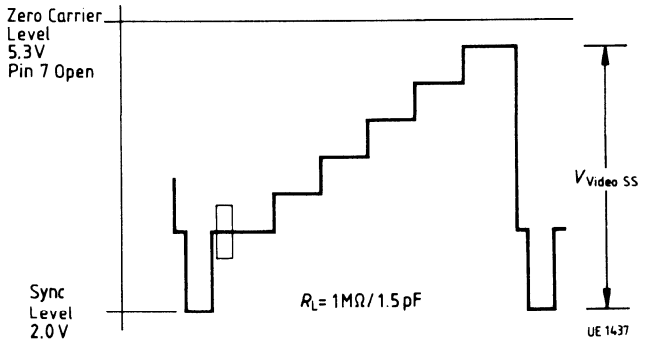
AGC Time Constant QPS



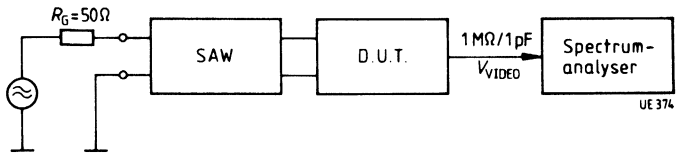
Sound Carrier Output QPS



AGC Time Constant QPS

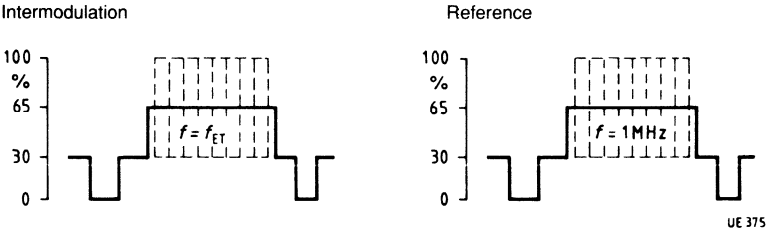


Measurement Configuration



(SAW 351 D)
(SAW 361 S)

Test signal: f_{VC} = 38.9 MHz with test signal modulated with 10% residual carrier; sound carrier – 13 dB (transmitter side)



Intermodulation ratio $a_{IM} = 20 \log \frac{V_{video\,(f\,=\,1\,MHz)}}{V_{video\,(f\,=\,f_{SC}-f_{CC})}}$

The 50% IRE signal with ± 50% IRE color carrier corresponds to Cyan with 75% color saturation.

Video IF IC with Quasi-Parallel Sound and AFC

TDA 5835

Bipolar IC

Video IF Section

Controlled AM broadband amplifier with synchronous demodulator, video amplifier, and AGC voltage generation for the video IF amplifier and tuner.

Quasi-Parallel Sound Section

Controlled AM broadband amplifier with quadrature demodulator, sound carrier output, internal AGC voltage generation, and an AFC section which can be disabled.

The TDA 5835 is especially suitable for application with black and white or color television receivers and/or VTR systems with PNP/MOS tuners for TV standards with negative video modulation and FM sound

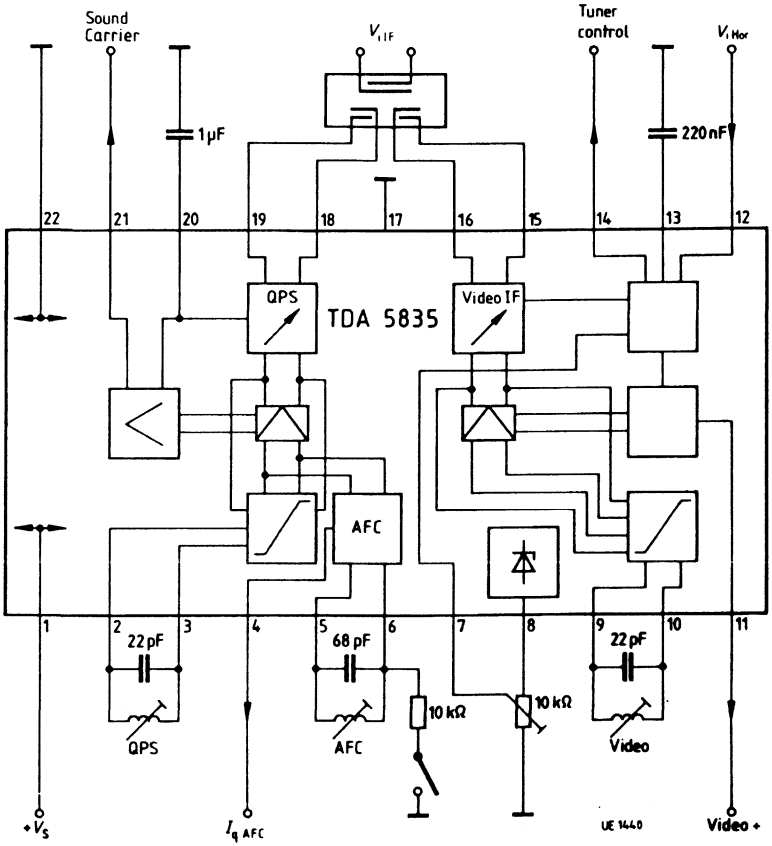
Type	Ordering Code	Package
TDA 5835	Q67000-A2507	P-DIP-22

Circuit Description

The video IF section is comprised of a 4-stage controllable AM amplifier, a limiter, and a mixer for the synchronous demodulation of video signals as well as an amplifier for the positive video output signal. The positive signal is used for gated control and a threshold amplifier to derive the delayed tuner AGC from the AGC voltage.

The quasi-parallel sound section also includes in 4-stage AM amplifier, a limiter, and a mixer for the quadrature demodulation of the 1st sound IF with subsequent sound carrier output for the 1st sound IF. The control voltage is generated by a peak value rectifier from

Block Diagram



Pin Functions

Pin No.	Function
1	Supply voltage
2	Demodulator tank circuit QPS
3	Demodulator tank circuit QPS
4	Push-pull current output AFC
5	Demodulator tank circuit AFC
6	Demodulator tank circuit AFC and switch-off
7	Tuner AGC threshold
8	Reference voltage
9	Demodulator tank circuit video IF
10	Demodulator tank circuit video IF
11	Video output
12	Gating pulse input
13	AGC time constant video IF
14	Delayed tuner AGC
15	Video IF input
16	Video IF input
17	GND
18	QPS IF input
19	QPS IF input
20	AGC time constant QPS
21	Sound carrier output
22	GND

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_1		13	V
Max. DC voltage	$V_{2,3}$	V_8	V_1	V
Max. DC voltage	V_4	0	V_1	V
Max. DC voltage	$V_{5,6}$	V_8	V_1	V
Max. DC voltage	V_7	0	V_1	V
Max. DC current	I_8	– 2	2	mA
Max. DC voltage	$V_{9,10}$	V_8	V_1	V
Max. DC current	$-I_{11}$	– 1	3	mA
Max. DC voltage	V_{12}	– 10	V_1	V
Max. DC voltage	$V_{13,14,15}$	0	V_1	V
Max. DC voltage	$V_{16,18}$	0	V_1	V
Max. DC voltage	$V_{19,20}$	0	V_1	V
Max. DC current	I_{21}	– 1	2	mA
Junction temperature	T_j		150	°C
Storage temperature range	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		55	K/W

Operating Range

Supply voltage	V_S	10.5	12.6	V
IF frequency	f_{IF}	15	75	MHz
Ambient temperature	T_A	0	70	°C

Characteristics

V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_1		102	134	mA	
Stab. reference voltage	$V_{8/22}$		6.7	7.0	V	

Video IF

Control current for tuner	I_{14}		4.5		mA	
Tuner AGC threshold	$V_{7/22}$	0		4.0	V	
Gating pulse voltage	V_{12} V_{12}	4.0 – 10		V_1 – 4.0	V V	pos. gating pulse neg. gating pulse
Input voltage at G_{max}	$V_{I\,15/16}$		30	60	µV	$V_{11\,pp}$ = 3 V
AGC range	ΔG		60		dB	
IF control voltage	$V_{13/22}$ $V_{13/22}$	0		 4.0	V V	G_{max} G_{min}
Video output voltage	$V_{Q\,11\,pp}$		3.0		V	$R_L = \infty$
Sync pulse leve	$V_{11/22}$		2.0		V	
DC voltage V_{13} = 4 V; $V_{15/16}$ = 0 V	 $V_{Q\,11\,pp}$		 5.3		 V	
Output current	$I_{Q\,11}$ $I_{Q\,11}$		– 5.0 + 2.0		mA mA	to ground via R to plus V_{11} = 7 V
AFC output current	$I_{Q\,4}$		± 1		mA	di/df < 0
AFC OFF ON	$V_{5/22}$ $V_{5/22}$	0	 6.0	4.0	V V	$V_5 = V_6$; R = 10 kΩ

Quasi-Parallel Sound

Sound carrier output voltage	$V_{Q\,21}$	10			mV	$V_{I\,PC}$ = 1 mV $V_{I\,SC}$ = 300 µV
Input voltage at G_{max}	$V_{I\,18/19}$		50	100	µV	$V_{21} = V_{21}$ -3 dB
AGC range	ΔG		60		dB	$V_{21} = V_{21} \pm 3$ dB
Signal-to-noise-ratio						IEC 468
White/staircase signal			61		dB	peak weighting
Black picture			66		dB	

Characteristics

V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Test Conditions						
Video carrier/sound carrier			10		dB	
Modulation frequency			1		kHz	
Frequency deviation			50		kHz	
IF input voltage			20		mV	
Design-Related Characteristics						
Input impedance	$Z_{I\,15/16}$ $Z_{I\,18/19}$		1.8/2 1.8/2		kΩ/pF kΩ/pF	
Output impedance	$Z_{Q\,2/3}$ $Z_{Q\,9/10}$ $Z_{Q\,5/6}$		6.6/2 6.6/2 20		kΩ/pF kΩ/pF kΩ	
Output resistance	$R_{Q\,11}$		150		Ω	
Residual IF (fundamental wave)	V_{11}		10		mV	
Video bandwidth (-3 dB)	B_{video}		6.0		MHz	
Intermodulation ratio with reference to f_{cc}	α_{IM}		50		dB	sound color interference
Output resistance	$R_{Q\,21}$		200		Ω	
IF control voltage	$V_{20/22}$ $V_{20/22}$	0		4	V V	G_{max} G_{min}

Alignment Procedures

a) Video IF

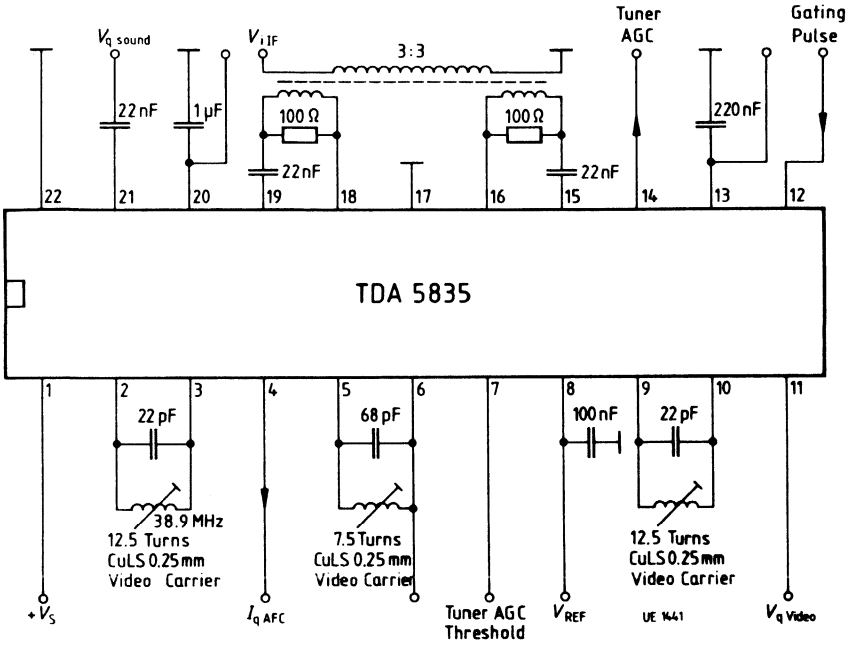
At a video carrier input level of $V_{15/16\ rms}$ = 10 mV and a superimposed AGC voltage of V_{13} = 3 V, the demodulator tank circuit is preliminarily aligned so that the demodulated video signal $V_{11\ pp}$ reaches its maximum output level at the positive video output. Any suitable video test signal can be used for modulation. Subsequently, the AGC voltage V_{13} is reduced until the video signal equals approx. 3 V (peak-to-peak). By fine-aligning the demodulator tank circuit, the maximum output level of the video signal is reached.

The flat response characteristic of the demodulator ensures a non-critical alignment procedure.

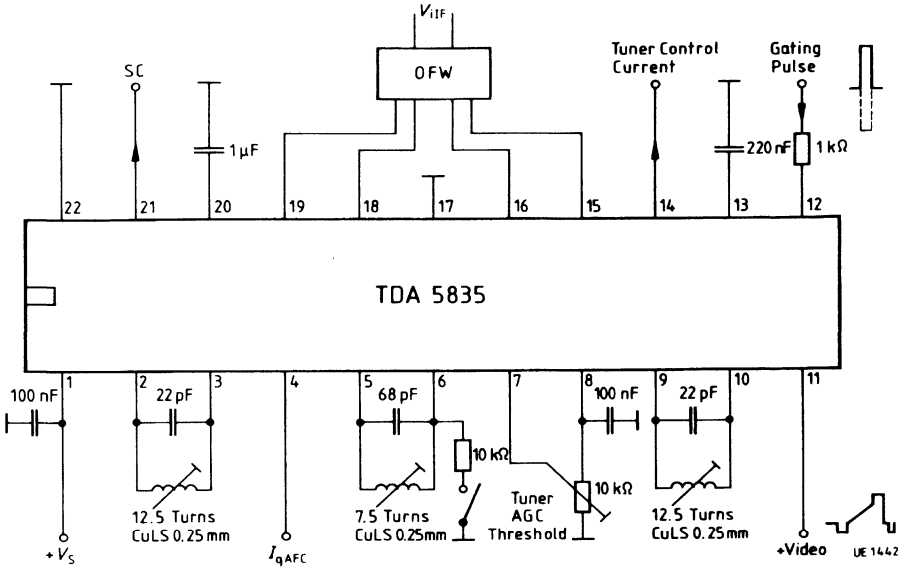
b) QPS

At an input signal of $V_{18/19\ rms}$ = 10 mV the demodulator tank circuit is preliminarily aligned until a max. AM suppression of the demodulated video signal V_{21} is reached at the sound carrier output. A video signal critical for the sound-interference ratio should be used for modulation (white/staircase, FuBK). Subsequent fine-aligning is performed by measuring the sound-interference ratio at the output of a FM demodulator and fine-aligning the demodulator tank circuit for a max. interference ratio. If several sound carriers are used in a device, the sound carrier with the lowest level should be used for alignment purposes.

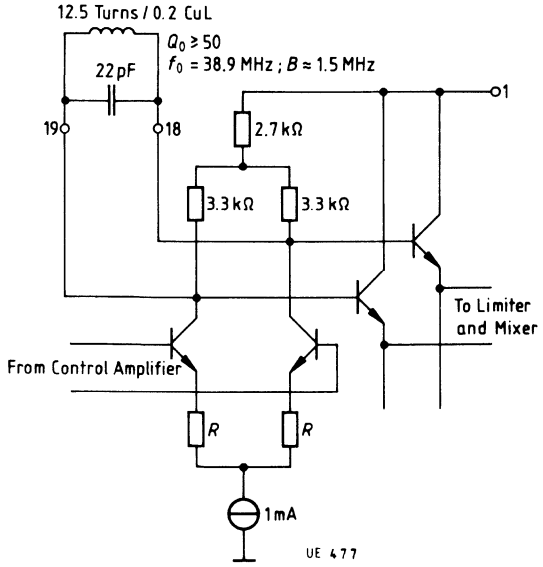
Measurement Circuit



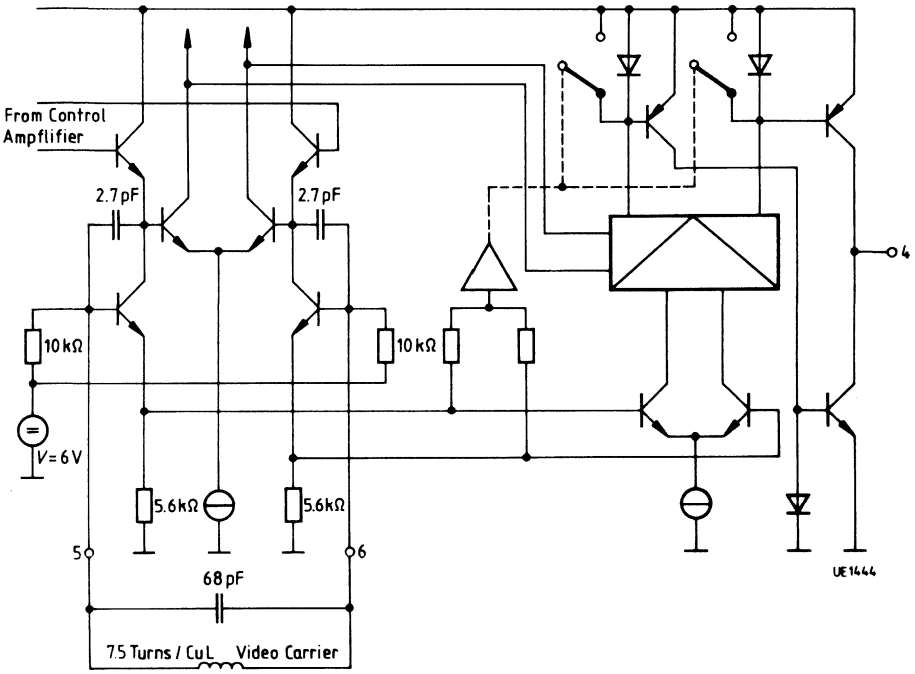
Application Circuit



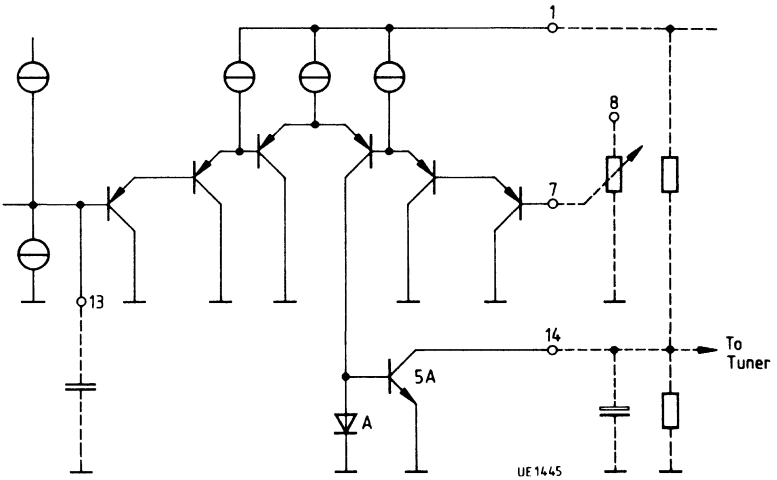
Demodulator Tank Circuit of QPS Unit



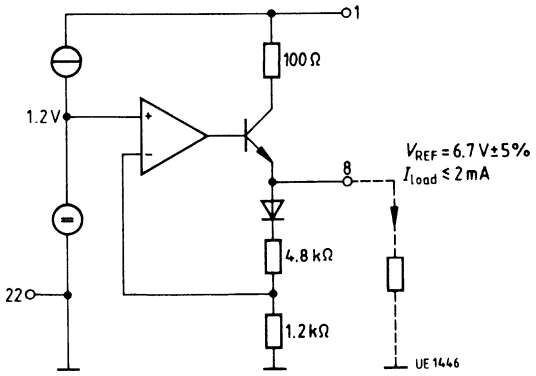
Demodulator Tank Circuit of AFC Unit



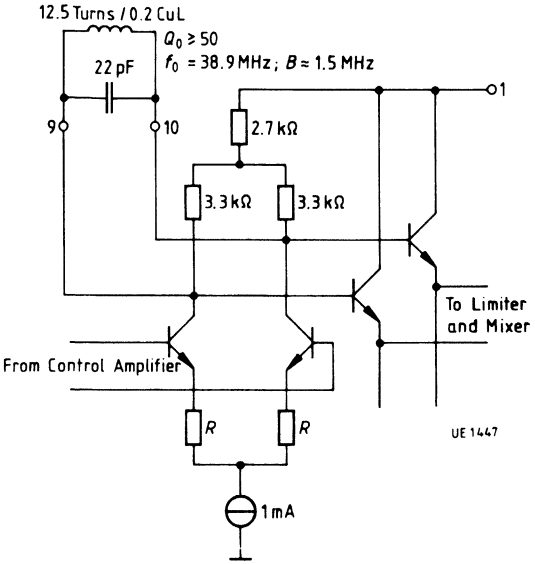
Tuner AGC Threshold and Output



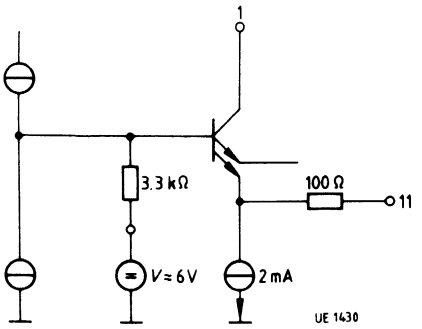
Reference Voltage



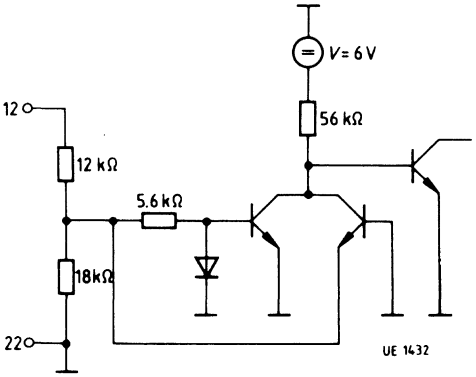
Demodulator Tank Circuit of Video IF Unit



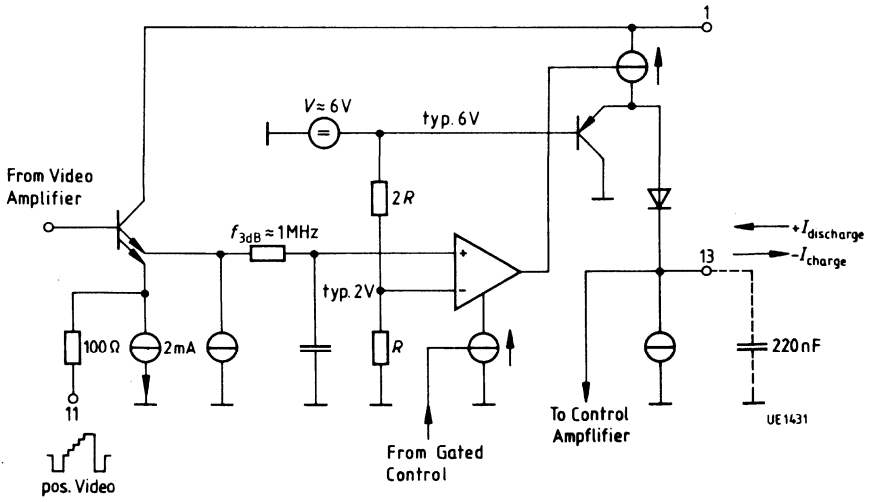
Positive Video Output



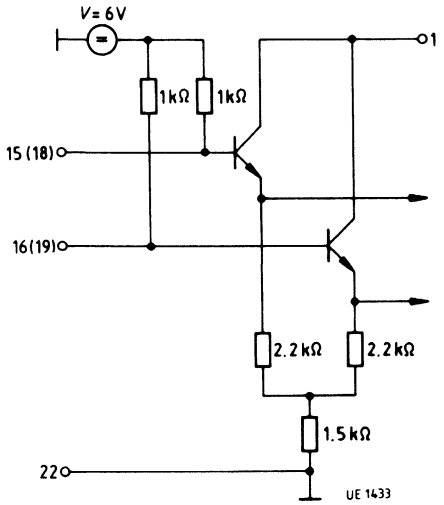
Gating Pulse Input



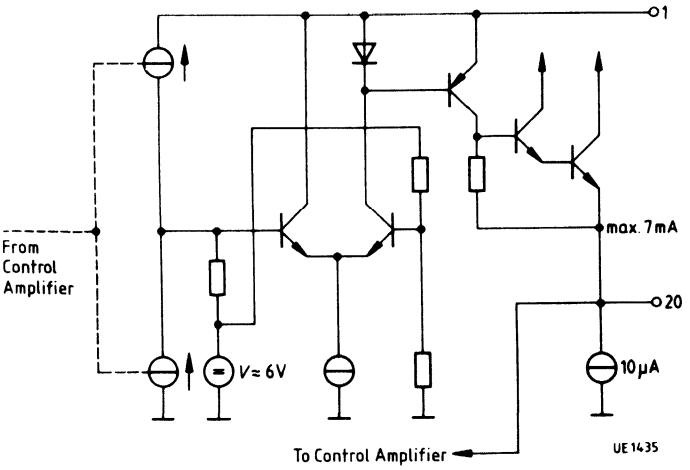
AGC Time Constant of Video IF Unit



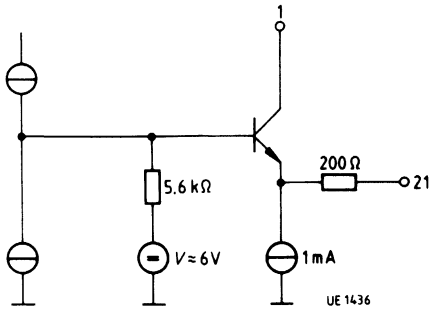
IF Input of Video IF
IF Input of QPS



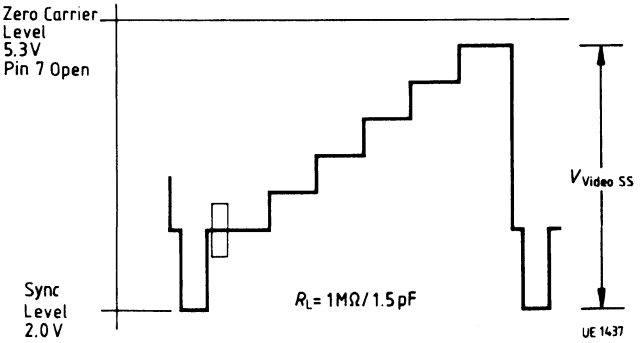
AGC Time Constant of QPS Unit



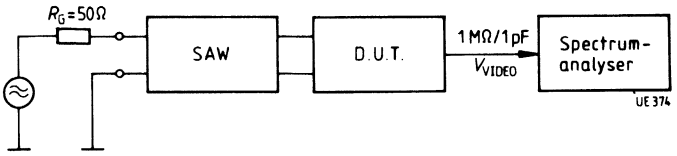
Sound Carrier Output of QPS Unit



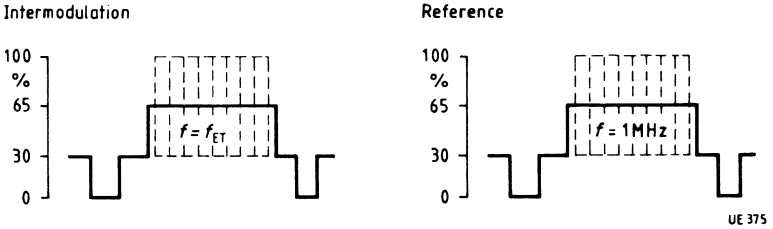
Pos. Video Output



Measurement Configuration



Test signal: f_{VC} = 38.9 MHz with test signal modulated with 10% residual carrier; sound carrier –13 dB (transmitter side)



Intermodulation ratio: $a_{IM} = 20 \log \frac{V_{video\ (f = MHz)}}{V_{video\ (f = f_{SC} - f_{CC})}}$

The 50% IRE signal with ± 50% IRE color carrier corresponds to Cyan with 75% color saturation.

SIEMENS

Video Switch

TDA 5850

Bipolar IC

Features

- Standard connection for VTR (CCIR) and Peri TV sets
- Input clamping
- Positive and negative video outputs

The TDA 5850 is a switchable video amplifier with connections for the French and IEC VTR standards.

Type	Ordering Code	Package
TDA 5850	Q67000-A1775	P-DIP-8

Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

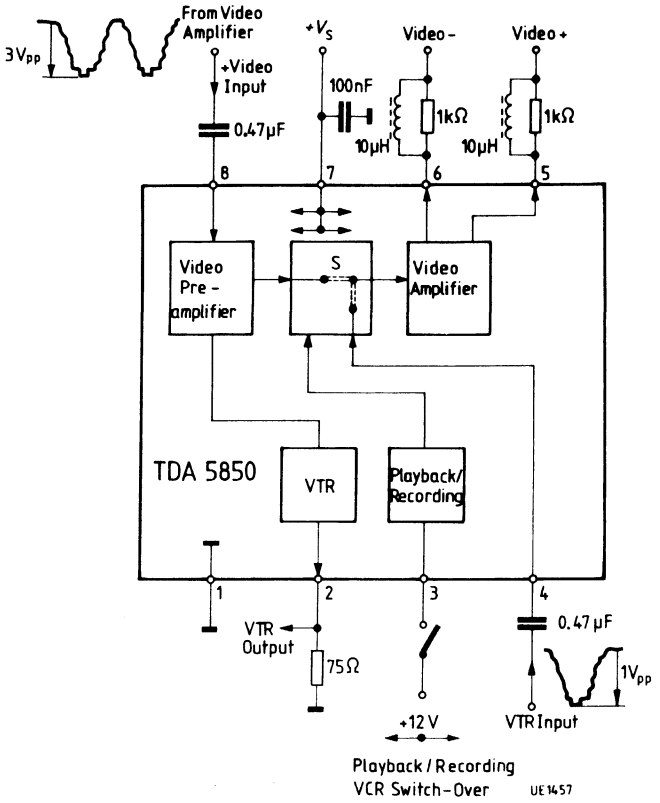
Operating Range

Supply voltage	V_S	10 to 15.8	V
Video bandwidth	B_{video}	6	MHz
Ambient temperature	T_A	0 to 70	°C

Characteristics
V_S = 13 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption (pin 2 open)	I_7		23.0		mA
Switch input VTR recording	$V_{3/1}$	0		1.2	Vdc
Switch input VTR playback	$V_{3/1}$	3.0		V_7	Vdc
Switch input $V_{3/1}$ = 15 V	I_3			1.0	mA
Video output voltage pos. V_3 = 1.2 V; $V_{8\,pp}$ = 3 V	$V_{Q\,5\,pp}$		3.0		V
Video output voltage pos. $V_3 \geq 3$ V; $V_{4\,pp}$ = 1 V	$V_{Q\,5\,pp}$		3.0		V
Sync pulse level	$V_{5/1}$		2.0		V
Output current (to ground)	$I_{Q\,5}$		– 5.0		mA
Output current (to +)	$I_{Q\,5}$		2.0		mA
Output resistance	$R_{Q\,5}$		150		Ω
Video output voltage neg. V_3 = 1.2 V; $V_{8\,pp}$ = 3 V	$V_{Q\,6}$		3.0		V
Video output voltage neg. $V_3 \geq 3$ V; $V_{4\,pp}$ = 1 V	$V_{Q\,6\,pp}$		3.0		V
Sync pulse level	$V_{6/1}$		V_7 -2		V
Output current (to ground)	$I_{Q\,6}$		– 5.0		mA
Output current (to +)	$I_{Q\,6}$		1.0		mA
Output resistance	$R_{Q\,6}$		150		Ω
Video output voltage pos. $V_{8\,pp}$ = 3 V; $R_{2/1}$ = 75 Ω	$V_{Q\,2\,pp}$		1.0		V
Sync pulse level $R_{2/1}$ = 75 Ω	$V_{2/1}$		1.0		V
Output current (to ground)	$I_{Q\,2}$		– 30.0		mA
Output current (to +)	$I_{Q\,2}$		2.0		mA
Output resistance	$R_{Q\,2}$		75		Ω
Video input current ($V_{8\,pp}$ = 3 V)	$I_{I\,8}$			40	µA
Video input current ($V_{4\,pp}$ = 1 V)	$I_{I\,4}$			20	µA
Video gain ($V_{8\,pp}$ = 3 V; $R_{2/1}$ = 75 Ω)	$G_{2/8}$		1/3		
Video gain ($V_{8\,pp}$ = 3 V; V_3 = 1.2 V)	$G_{5/8}$		1		
Video gain ($V_{8\,pp}$ = 3 V; V_3 = 1.2 V)	$G_{6/8}$		– 1		
Video gain ($V_{4\,pp}$ = 1 V; $V_3 \geq 3$ V)	$G_{5/4}$		3		
Video gain ($V_{4\,pp}$ = 1 V; $V_3 \geq 3$ V)	$G_{6/4}$		– 3		
Video bandwidth (– 3 dB)	B_{video}	6.0			MHz
Cross-talk rejection referred to $V_{5\,pp}$ = 3 V f = 50 Hz...6.0 MHz; V_3 = 1.2 V; $V_{4\,pp}$ = 1 V	a		50		dB

Block Diagram, Measurement Circuit and Application Circuit



SIEMENS

Stereo-IF

TDA 5910

Preliminary Data

Bipolar IC

Features

- Quasi-parallel sound, AM sound
- Average or peak AGC control
- Active carrier recovery with F PLL concept
- Picture/sound stages are fully SCART compatible
- I^2C bus for μP controllable switching functions

Type	Ordering Code	Package
TDA 5910	Q67000-A8167	P-DIP-40

Euro-standard video IF for positive and negative modulation. The video section has a full SCART interface. A separate video output after the demodulator permits the installation of one or more sound traps at the input of the SCART switch. Carrier recovery is accomplished by an FPLL. An AFC signal is derived from the VCO tuning voltage. The tuner AGC threshold is set by means of a potentiometer.

Euro sound IF for AM and FM sound transmissions using a multistandard FM IF converter.

Dual FM sound IF with coincidence demodulator. The AM-FM changeover switch is located at sound IF output 1.

To permit RF muting a coincidence detector for identifying TV signals is built in. During the SCART playback mode it is recommended to use this function.

I^2C bus for controlling the changeover functions and the three ports as well as for reading out the identification and AFC "up" / "down" data.
Use in multi-standard TV sets for mono and stereo applications with full SCART, meeting PTT requirements.

Circuit Description

The video IF section incorporates a four-stage, capacitively coupled, symmetrical and controlled amplifier, a FPLL carrier recovery stage, a mixer for synchronous demodulation of positively and negatively modulated IF signals followed by a video output amplifier and noise suppression circuitry. The video output is used for generating the AGC voltage. The control circuit for both types of modulation is designed on the integralaction AGC principle, employing noise-free peak value detectors for both types and an averaging detector for the positive modulation only. For SCART applications, a video switch with two inputs (for signals from demodulator or SCART socket) and two outputs (SCART and TV output) is connected to the video output. The video output (pin 28) and the SCART switch input (pin 26) are connected by means of a sound trap with a pass-band attenuation of 3.5 dB (factor 2/3) for both DC and AC. A delayed tuner AGC voltage with positive control direction (increase in tuner AGC voltage → increase in gain) is derived from the AGC voltage via a threshold amplifier that is set by means of an external potentiometer. The demodulator output delivers a video level that is 3.5 dB higher than is normally required for the TV set or the SCART socket. This makes it possible to install one or more sound traps between the video output and the SCART switch input. This trap has to be designed to reduce the AC or DC signal level by 3 dB to prevent overdriving in the switch. The TV standard selection and SCART recording/playback switching operations are controlled via the I^2C bus.
The FPLLs VCO tuning voltage is likewise fed to an OTA. At the output of the OTA the residual video signal is filtered out by means of a low-pass filter. The external reference voltage is connected to the OTA output via a resistor. The resistor connecting the reference output (pin 27) and the OTA output (pin 32) is used to vary the steepness of the S-curve. The S-waveform signal is fed to a window comparator to provide the I^2C bus with the necessary "up" / "down" data.

The Euro-Standard sound IF section incorporates a four-stage, capacitively coupled AGC amplifier followed by a quasi-synchronous demodulator for producing the average AGC control voltage and the audio voltage in the AM mode. The AM - AF signal is fed to the AM/FM changeover switch at sound IF 1 output (pin 32). In parallel with the AM demodulator, the AGC controlled sound IF signal is fed to a second mixer and superimposed with the picture carrier recovered in the FPLL. The resulting sound IF (for FM transmission) is fed into the multistandard sound converter. Here the sound IF signal is mixed with an oscillator signal. In this way only one sound IF filter is required to extract FM sound IF 1. For the standard sound IF, the oscillator and the mixer are taken out of operation.

The sound IF section incorporates two identical channels (sound IF 1 and sound IF 2). The AM/FM changeover switch is located at the output of the sound IF 1 demodulator. Both outputs can be muted. The switching functions are controlled via the I^2C bus.

For coincidence detection, the video signal is evaluated. The evaluation results are read out via the I^2C bus. AF 1 and AF 2 can be muted by means of software.

The I^2C bus is used for controlling the switching functions in the components and ports as well as for reading out the AFC windows ("up" / "down") and the coincidence information.

Software TDA 5910

The following data format is used:

1) Chip address (90H, 91H)

MSB							LSB	
1	0	0	1	0	0	0	X	Ack

MSB is transmitted first
X = 0 IC in the receive mode (90_H)

2) Data Bytes

MSB							LSB
V7	V6	V5	V4	V3	V2	V1	V0

V7 = MSB
V0 = LSB

1	0	X	X	X	X	X	X

Data Byte by "Receive Mode" (Chip Address = 90 H):

MSB							LSB
P2	P1	P0	VCR	AM	FM	TV STAN-DARD	5.5 MHz
P2	=0:	PORT	P2	is	tristate;	POWER	ON
P2	=1:	PORT	P2	is	open collector LOW;		
P1	=0:	PORT	P1	is	tristate;	POWER	ON
P1	=1:	PORT	P1	is	open collector LOW;		
P0	=0:	PORT	P0	is	tristate;	POWER	ON
P0	=1:	PORT	P0	is	open collector LOW;		
VCR	=0:	REPRODUCTION					
VCR	=1:	RF OPERATION;			POWER	ON	
AM	=0:	AM-ON					
AM	=1:	AM-OFF			(=MUTE);	POWER	ON
FM	=0:	FM-ON					
FM	=1:	FM-OFF			(=MUTE);	POWER	ON
TV STAN-DARD	=0:	L-STANDARD (pos. modulat.)					
TV STAN-DARD	=1:	G-,M-,I-STANDARD (neg. modulat.)				POWER	ON
5.5 MHz	=0:	MULTISOUND			FM-IF		
5.5 MHz	=1:	5.5 MHz			FM-IF;	POWER	ON

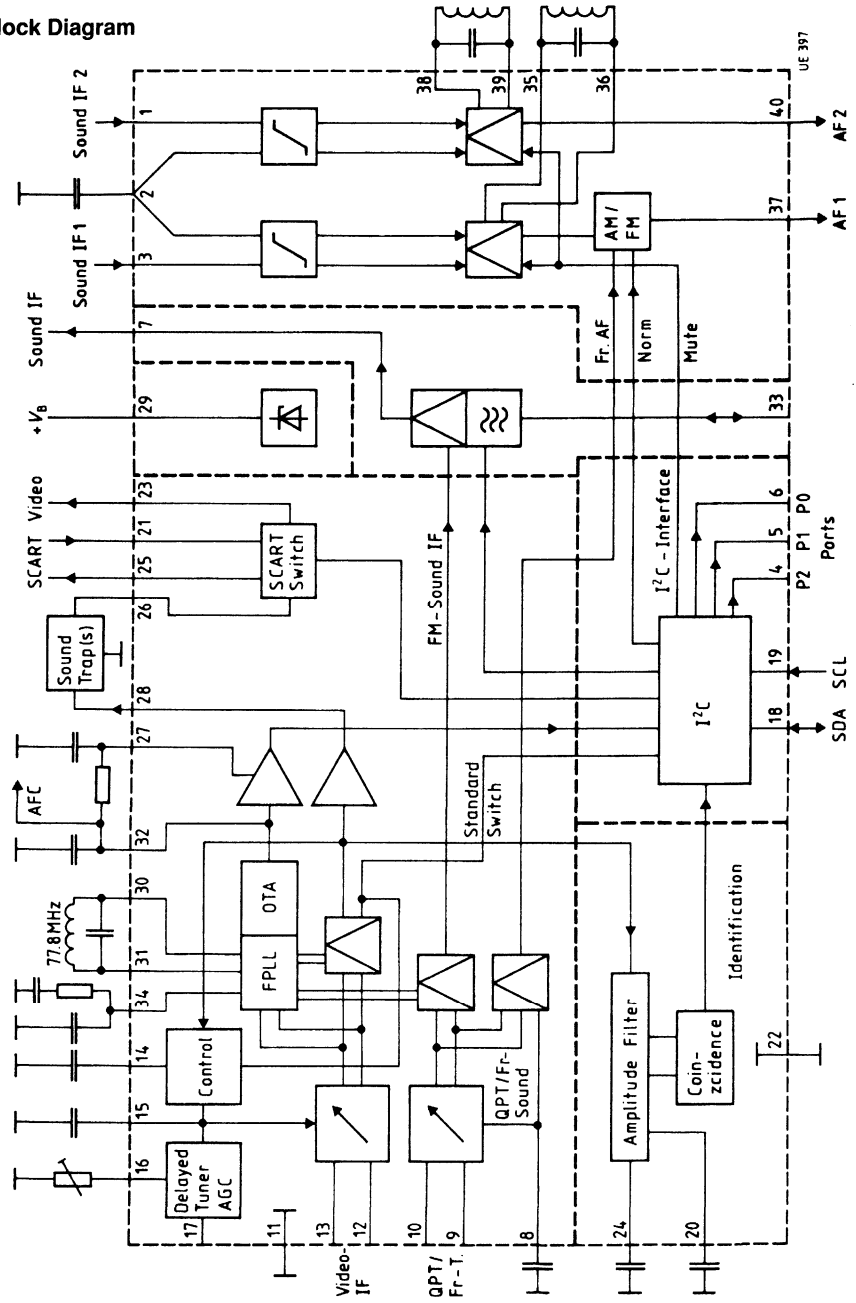
Data Byte by "Transmit Mode" (Chip Address = 91 H):

MSB LSB

P0-IN TVID DOWN UP

P0-IN	=0:	P0 INPUT = HIGH
P0-IN	=1:	P0 INPUT= LOW
TVID	=0:	Coincidence recognized
TVID	=1:	Coincidence not recognized
DOWN	=0:	AFC to HIGH
UP	=1:	AFC to HIGH
DOWN	=1:	AFC to LOW
UP	=0:	AFC to LOW
DOWN	=0:	AFC MIDDLE
UP	=0:	AFC MIDDLE
DOWN	=1:	is suppressed
UP	=1:	is suppressed

Block Diagram

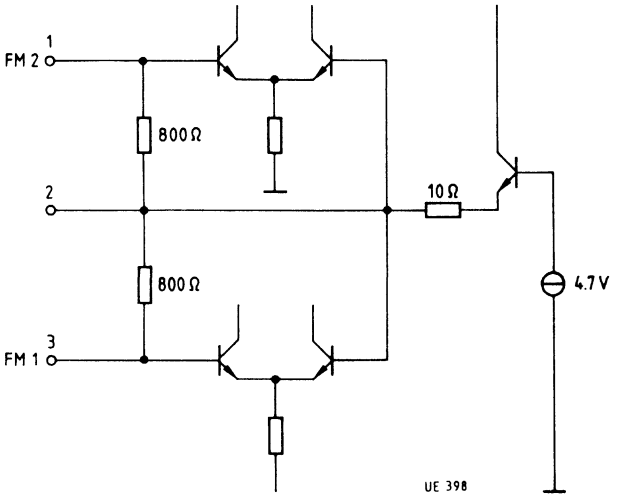


Pin Functions

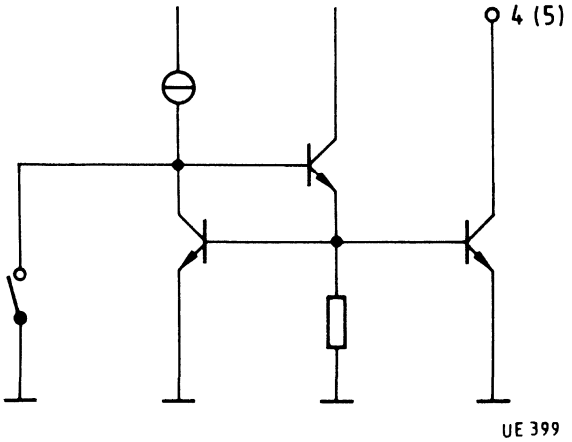
Pin No.	Function
1	Sound IF input 2
2	Sound reference
3	Sound IF input 1
4	Port 2
5	Port 1
6	Port 0
7	FM Sound IF output (TT1; TT2; NICAM)
8	AGC time constant (Euro-Standard sound IF)
9	Euro-Standard sound IF input
10	Euro-Standard sound IF input
11	Ground
12	Video IF input
13	Video IF input
14	Mean value AGC time constant
15	Main AGC time constant
16	Delayed tuner AGC threshold
17	Delayed tuner AGC output
18	I^2C bus (SDA)
19	I^2C bus (SCL)
20	Vertical amplitude filter time constant
21	Video SCART input
22	Ground
23	Video output
24	Horizontal amplitude filter time constant
25	Video SCART output
26	Video input at sound trap output
27	Voltage reference for AFC
28	Video output at demodulator output
29	+ V_S supply
30	FPLL-VCO (2 × video carier)
31	FPLL-VCO (2 × video carier)
32	AFC filter
33	Multi-standard oscillator
34	FPLL Loop filter
35	Sound IF 1 demodulator
36	Sound IF 1 demodulator
37	AF 1 output
38	Sound IF 2 demodulator
39	Sound IF 2 demodulator
40	AF 2 output

Pin Functions

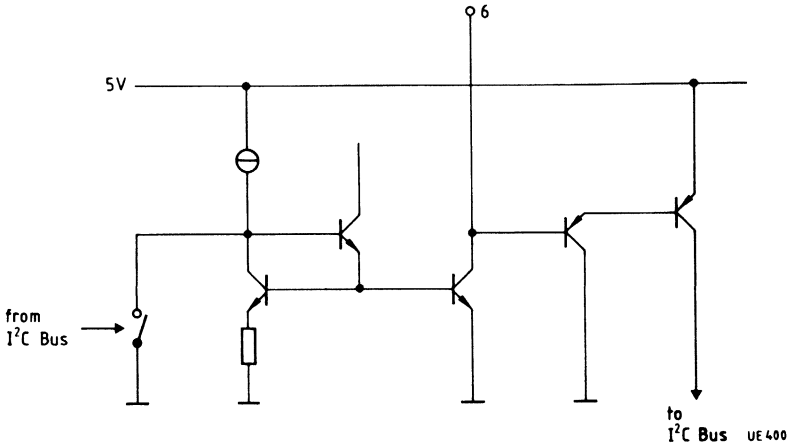
FM Limiter Amplifier Output (Pin 1, 2, 3)



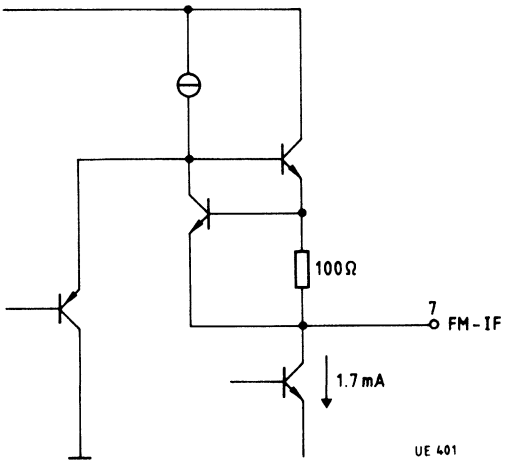
Port P1, P2 (Pin 4, 5)



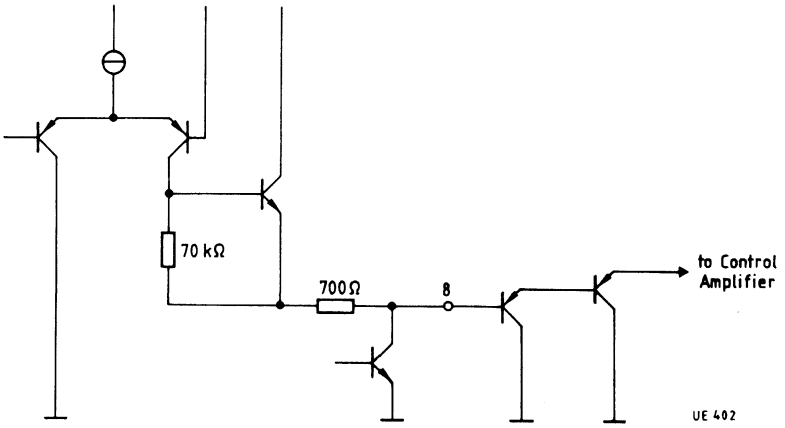
Port 0 (Pin 6)



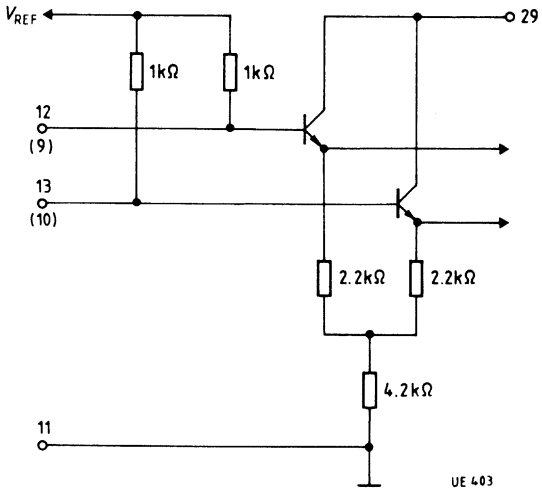
Multi Sound IF Output (Pin 7)



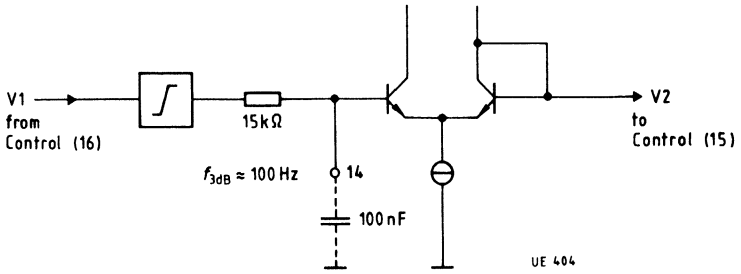
QPT Control (Pin 8)



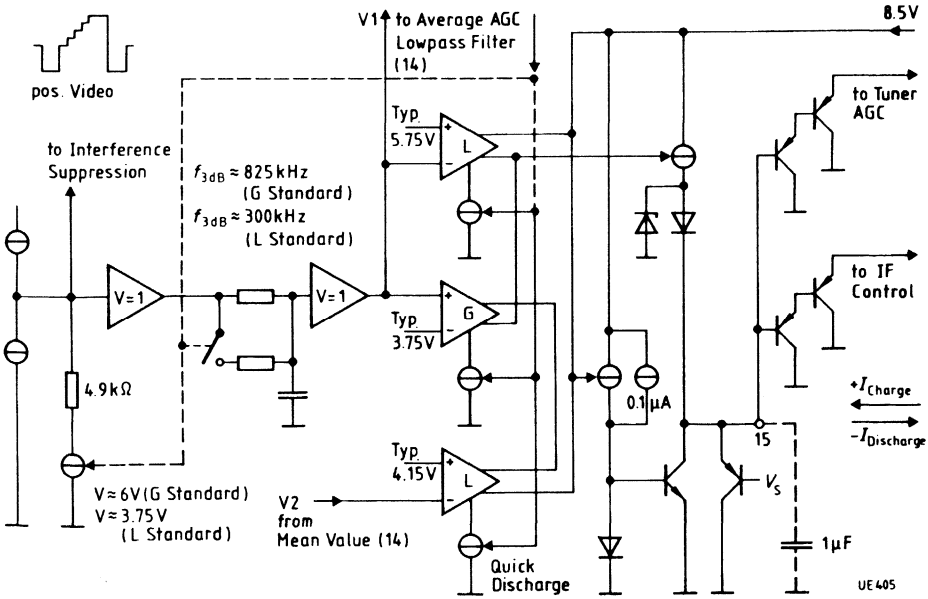
IF Inputs (9/10) (Pin 12, 13)



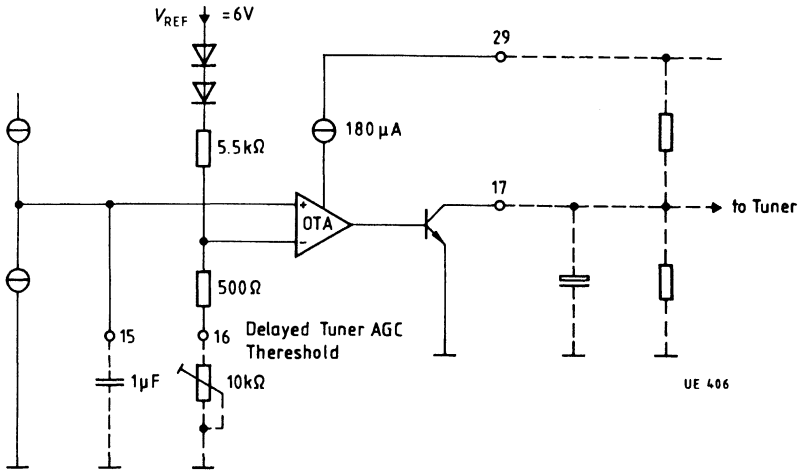
Average AGC Low Pass Filter (Pin 14)



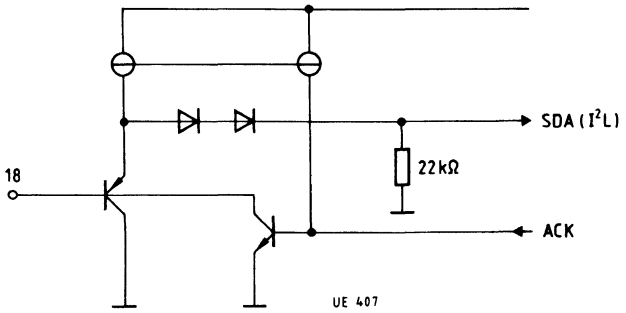
Time Constant AGC (Pin 15)



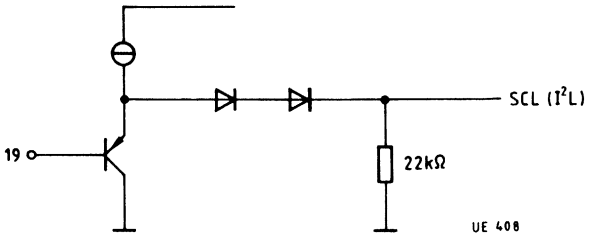
Tuner AGC Threshold and Output (Pin 16, 17)



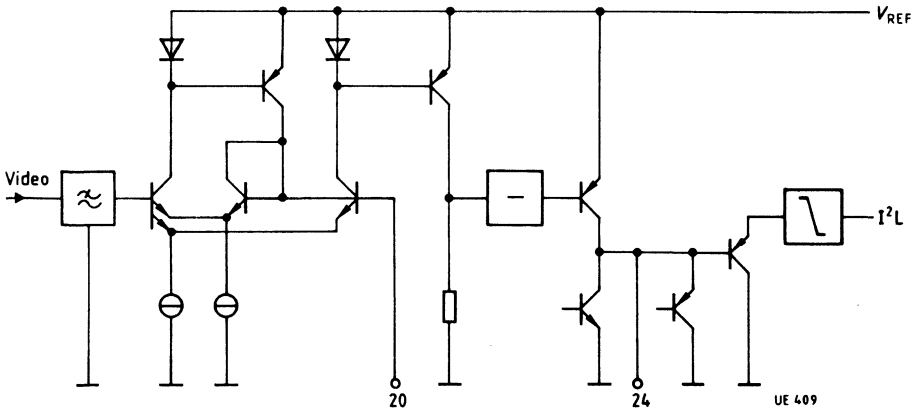
I²L Bus SDA (Pin 18)



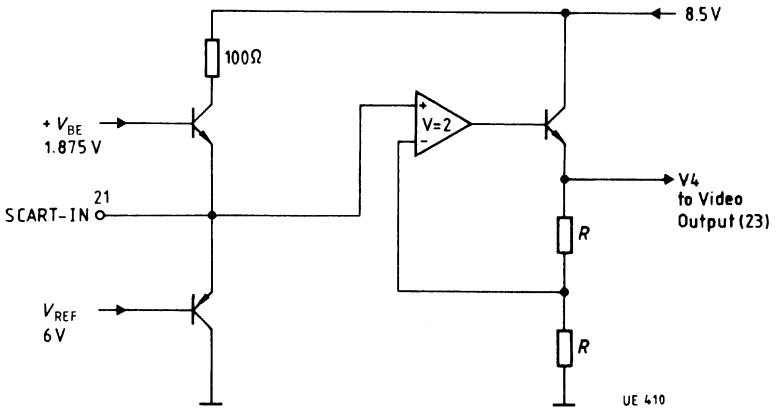
I^2L Bus SCL (Pin 19)



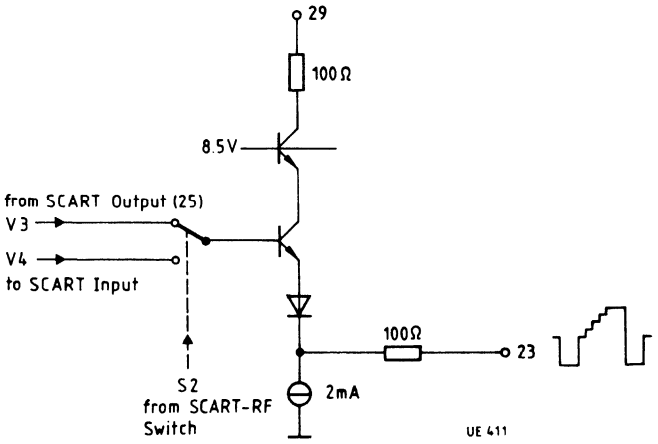
TV Identification (Pin 20, 24)



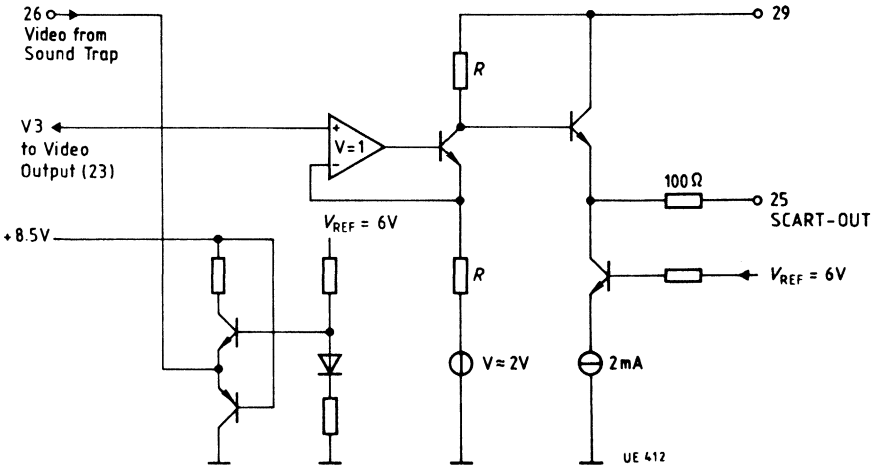
SCART Input (Pin 21)



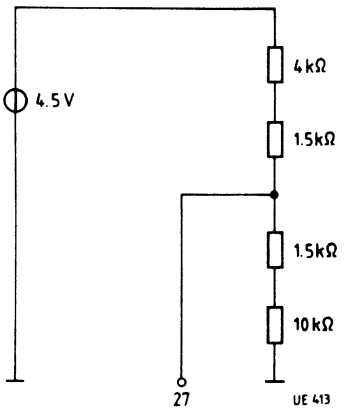
Video Output and Video Switch (Pin 23)



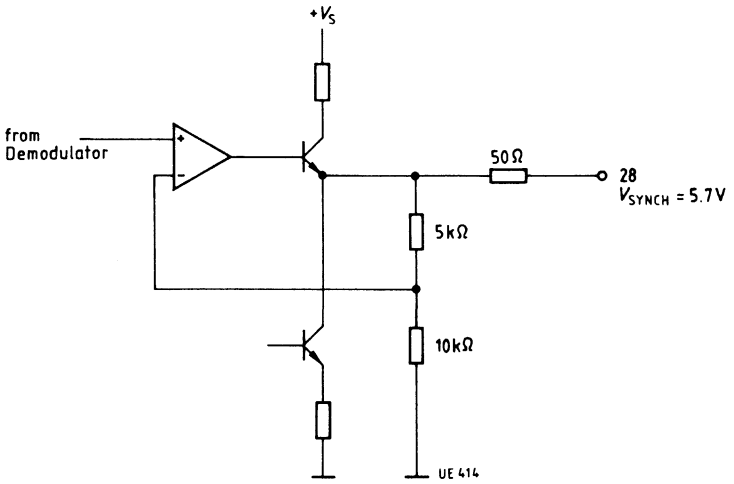
Sound Trap Input and SCART Output (Pin 25, 26)



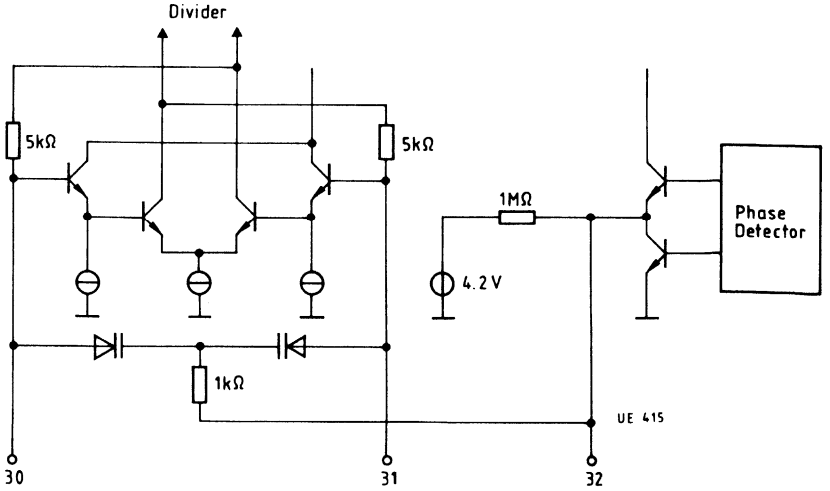
AFC Reference (Pin 27)



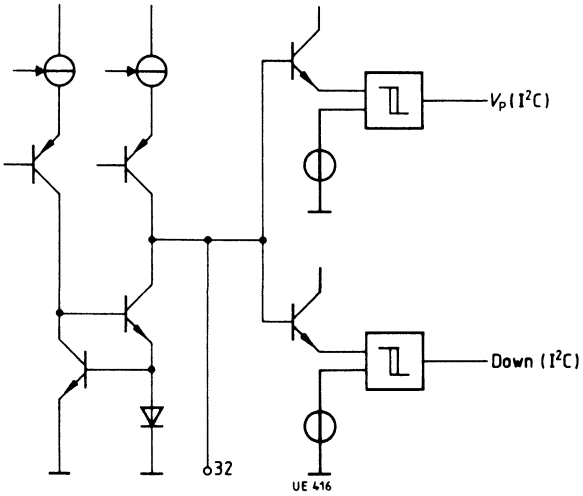
Demodulator Output (Pin 28)



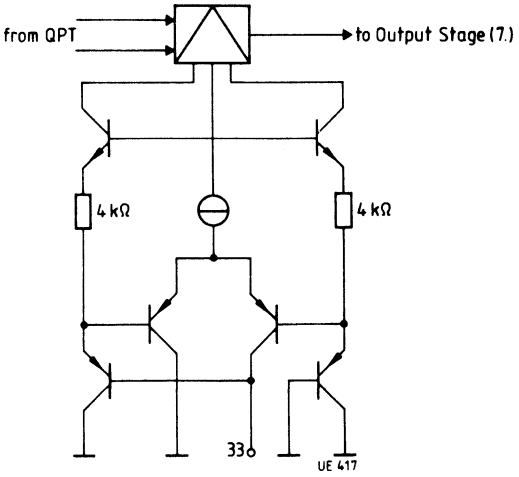
Demodulator Tank Circuit and Loop Filter Output (Pin 30, 31, 34)



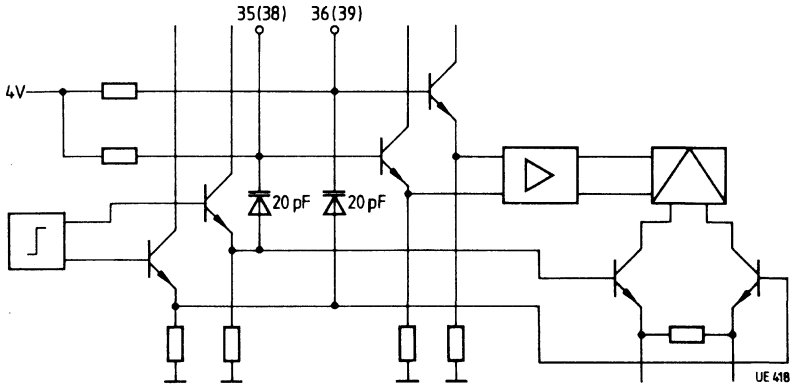
AFC Output/Window Comparator Input (Pin 32)



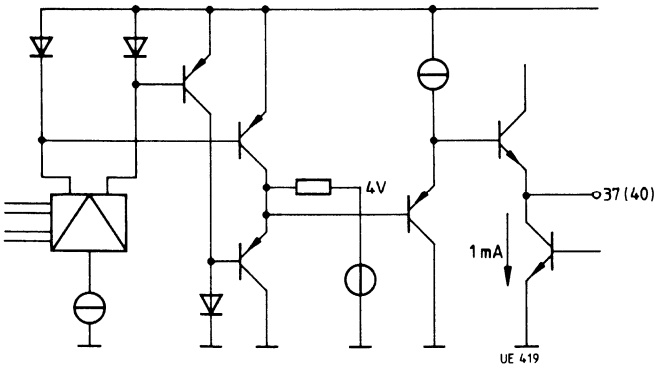
FM Converter Oscillator (Pin 33)



FM Demodulator Tank Circuit (Pin 35, 36, 38, 39)



AF Output (Pin 37, 40)



Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	0	13.2	V
Reference voltage to ground	$V_{27/22}$	0	6	V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\ SA}$		51	°K/W

Operating Range

Supply voltage	V_{29}	10.8	13.2	V
Supply voltage delayed tuner AGC	V_{17}	1	10	V
Ambient temperature during operation	T_A	0	70	°C
Input frequency range – 3 dB	f_{IF}	10	100	MHz
Input frequency range – 0.3 dB	f_{IF}	30	75	MHz
Function range of the sound-conversion oscillator	$f_{Sound\ OSC}$	1	15	MHz

All voltage values are referenced to ground pin 3, 15, if not stated otherwise. The current isidentified according to the source/sink principle.
If the IC is considered a sink (the current flows the respective pin to ground), it is identified by a negative algebraic sign.
However, if the IC is the source (the current flows from V_8 via the respective pin) it is identified by a positive algebraic sign.

Characteristics

V_S = 12 V ± 10 %; the input levels are given as rms values to synchronous peak
f_{PC} = 38.9 MHz ; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Total current consumption	$-I_{29}$		tbf		mA	$V_{12/13}$ = 10 mV rms
Video IF Part						
AGC voltage						
Min. AGC	V_{15}	0	0.1	0.5	V	$V_{12/13}$ = 45 µV rms
Max. AGC	V_{15}	2.6	2.85	6.0	V	$V_{12/13}$ = 175 mV rms
AGC Time Constant with Neg. Modulation						
Charge current (I_{max}:2)	I_{15}	0.55	0.70	0.95	mA	V_{15} = 2V; V_{23} < 2.2 V
Discharge current	$-I_{15}$	13	17	23	µA	V_{15} = 2V; V_{23} > 2.8 V
Charge-/discharge ratio	V_{15}	55	82	140		
AGC Time Constant with Pos. Modulation						
Charge current (I_{max}:2)	I_{15}	0.60	0.75	0.90	mA	V_{15} = 2 V; $V_{23} \geq$ 4.6 V
Discharge current	$-I_{15}$	0.1	0.2	0.3	µA	V_{15} = 2 V; 3.1 V < V_{23} < 4.1 V
Discharge current	$-I_{15}$	65	80	95	µA	V_{15} = 2 V; V_{23} < 2.6 V
Charge-/discharge ratio	V_{15}	4500	6500	8500		
Mean Value Generation with Pos. Modulation						
White level	V_{14}	3.9	4.3	4.7	V	$V_{12/13}$ = 10 mV rms
Zero carrier level	V_{14}	3.3	3.7	4.1	V	$V_{12/13}$ = 0 V; V_{15} = 3 V
Tuner AGC threshold	V_{16}	4.2	4.5	4.8	V	R_{16} = ∞
$I_S = I_{max}$:2	I_{16}	650	850	1050	µA	V_{16} = 0 V
"	V_{15}	2.8	3.1	3.4	V	R_{16} = 10 k
"	V_{15}	0.33	0.38	0.43	V	R_{16} = 10 Ω
Tuner AGC current	$-I_{17}$	30	50		mA	V_{17} = 0.5 V_S $V_{12/13}$ = 100 mV rms V_{16} = 0.75 V
	$-I_{17}$	0		10	µA	V_{17} = 0.5 V_S $V_{12/13}$ = 10 mV rms V_{16} = 4.0 V
IF input	V_{12}, V_{13}	5.7	6.0	6.3	V	
Oscillator tank circuit	V_{30}, V_{31}	2.8	3.2	3.6	V	

Characteristics (cont'd)
V_S = 12 V ± 10 %; the input levels are given as rms values to synchronous peak
f_{PC} = 38.9 MHz; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Video Output (Demodulator)						
Output current	$-I_{28}$	2.0	2.5	3.0	mA	V_{28} = 9 V
Output current	I_{28}	4			mA	to ground
Sync pulse level	V_{28}	5.2	5.6	6.2	V	$V_{12/13}$ = 10 mV rms
Sound Trap Iinput						
Sync pulse level	V_{26}	3.3	3.7		V	signal splitting V_{28}/ V_{26} = 3/2
White level	V_{26}					signal splitting V_{28}/ V_{26} = 3/2
			5.7	6.5	V	$V_{12/13}$ = 0 V; V_{15} = 3 V
Pos. Video Output (fig. 8) RF Operation						
Output current	$-I_{23}$	1.5	2.0	2.5	mA	V_{23} = 6 V
	I_{23}	4			mA	to ground via R = 500Ω
Pos. Modulation (L Standard) V_{28} / V_{26} = 3/2						
White level	V_{23}	3.7	4.2	4.9	V	$V_{12/13}$ = 10 mV rms
Zero carrier (Sync)	V_{23}	1.9	2.2	2.7	V	$V_{12/13}$ = 0 V; V_{15} = 3 V
Neg. Modulation (BG Standard)						
Sync pulse level	V_{23}	1.9	2.2	2.7	V	$V_{12/13}$ = 10 mV rms
Zero carrier	V_{23}	3.9	4.4	5.1	V	$V_{12/13}$ = 0 V; V_{15} = 3 V
Neg. SCART Output (fig. 9) $R_L = \infty$; V_{28} / V_{26} = 3 / 2						
Output current	$-I_{25}$	1.5	2.0	2.5	mA	$V_{25} = V_{29}$
	I_{25}	4			mA	to ground via R = 500 Ω

Characteristics (cont'd)
T_A = 25 °C; V_S = 12 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Pos. Modulation (L Standard)						
White level	V_{25}	V_{12}-5.3	V_{12}-5.0	V_{12}-4.3	V	$V_{12/13}$ = 10 mVrms
Zero carrier (Sync)	V_{25}	V_{12}-3.2	V_{12}-2.9	V_{12}-2.5	V	$V_{12/13}$ = 0 V; V_{15} = 3 V
Neg. Modulation (BG Standard)						
Sync pulse level	V_{25}	V_{12}-3.2	V_{12}-2.9	V_{12}-2.5	V	$V_{12/13}$ = 10mVrms
Zero carrier	V_{25}	V_{12}-5.5	V_{12}-5.2	V_{12}-4.6	V	$V_{12/13}$ = 0V; V_{15} = 3 V
Pos. SCART Input						
Clamping level	V_{21}	1.8	1.9	2	V	via R = 270 kΩ to ground
Output current	I_{21}	3			mA	V_{21} = 1.2 V
AFC-reference	V_{27}	2.5	3.0	3.5	V	$R_{27/32} = \infty$
AFC current deviation	$\pm I_{32}$	± 24	± 30	± 36	µA	$R_{27/32}$ = 15 kΩ
AFC window comparator width	$\pm V_{F32}$	± 350	± 400	± 450	mV	$R_{27/32}$ = 15 kΩ
Hysteresis	ΔV_{H32}		50		mV	$R_{27/32}$ = 15 kΩ

Dynamic Characteristics

min. IF input voltage (min. gain) BR rms	$V_{12/13}$		45	60	µV	V_{23} – 1dB
max. IF input voltage (max. gain) BT rms	$V_{12/13}$	105	140		mV	V_{23} + 1dB
IF control range	ΔV	65	70		dB	
AFC control response	$\Delta I_{32} / \Delta f$		45		nA/kHz	

Characteristics (cont'd)
T_A = 25 °C; V_S = 12 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Video output voltage (peak-peak) PC = 10 mV_{rms} with neg. mod. and residual carrier = 10 %; with pos. mod. and residual carrier < 6 %						
Pos. video output	V_{23}	1.8	2.0	2.2	V_{pp}	RF operation
Changes with norm switch	ΔV_{23}		1	5	%	
Changes via operating voltage	$\Delta V_{23}/\Delta V_{29}$		1.5	3	%	10.8 V < V_{29} < 13.2 V
Neg. SCART output	V_{25}	1.9	2.1	2.3	V_{pp}	$R_L = \infty$
Video output voltage change by means of a control range of 55 dB						
	ΔV_{23}		0.2	0.5	dB	
Video gain	V_{23}/V_{21}		1.9	2.0	2.1	R_G < 500 Ω; SCART reproduction V_{21} = 1 V_{pp}(2 MHz)
Video band width	$B_{23/21}$ −3dB	8	10		MHz	SCART reproduc.; V_{21} = 1 V_{pp} Sine
Cross talk attenuation	a	40	50		dB	RF operation$_{2/13}$ = 0 V; V_{15} = 3 V; V_{21} = 1V_{pp} Sine 50 Hz . . . 10 MHz

Characteristics (cont'd)
T_A = 25 °C; V_S = 12 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Design Notes (no 100% final test)						
Input resistance (symmetrical)	$R_{12/13}$	1.5	2	2.5	kΩ	
Input capacitance (symmetrical)	$C_{12/13}$		2	5	pF	
Low pass cut-off	$f_{-3dB(14)}$	70	100	130	Hz	$C_{14/22;11}$ = 100 nF ± 10%
Pos. video output white level	V_{23}	3.9	4.2	4.9	V	(SCART operation) V_{21} = 1Vpp standard video signal
Sync pulse level	V_{23}	1.9	2.2	2.7	V	V_{21} = 1Vpp standard video signal
Video input voltage by R_G < 500 Ω	V_{21}		1		Vpp ± 3 dB	
Dyn. output resistance						
pos. video output	R_{23}	80	115	150	Ω	
neg. video output	R_{25}	100	150	200	Ω	
Demodulator output	R_{28}	70	100	130	Ω	
Noise figure $V_{12/13}$ = – 57 dBm = + 50 dBμV R_{GEN} = 800 IΩ	F		5	7	dB	
Video noise voltage ratio with PC = 10 mV_{rms}						
0 dB = 700 mV_{pp} BA unweighted	S/N	50	55	–	dB	
weighted according to CCIR Rec. 567-1	S/N	55	60	–	dB	

Characteristics (cont'd)
T_A = 25 °C; V_S = 12 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Video frequency reponse – 3 dB – 12 dB	 B_{-3dB} B_{-12dB}	 8 15	 10 17	 13 20	 MHz MHz	
Residual carrier voltage at video output PC = 10 mV$_{rms}$ Fundamental wave f = 38.9 MHz 1. harmonic wave f = 77.8 MHz	 V_{23} V_{23}		 3.0 0.3	 6.0 0.6	 mV mV	
Differential gain with PC = 10 mV$_{rms}$(staircase) Peak-to-peak accor. to CCIR Rec. 567-1 staircase signal Changes via AGC Changes via detuning f_{PC} = 38.9 MHz; Δf = ± 400 kHz	 DG $\Delta DG/\Delta v$ $\Delta DG/\Delta f$		 4	 6 1 1	 % % %	
Differential phase with PC = 10 mV$_{rms}$(staircase) Peak-to-Peak accor. to CCIR Rec. 567-1 staircase signal Changes via AGC Changes via detuning f_{PC} = 38.9 MHz; Δf = ± 400 kHz	 DP $\Delta DP/\Delta v$ $\Delta DP/\Delta f$		 1.5	 2.5 1 2	 degree degree degree	
Intermodulation ratio with f_{IM} = 1.07 MHz = f_{TT}-f_{FT} with PC = 10 mV$_{rms}$ sound porch – 13 dB sound porch – 20 dB sound porch – 17 dB	 a_{IM} a_{IM} a_{IM}	 32 54 51	 38 60 57	 	 dB dB dB	 SAW G 3950 SAW 361D SAW G 1956
Oscillator tank circuit voltage f_{OSC} = 2 × f_{PC}	 $V_{30/31}$		 700		 mV$_{pp}$	
Sync pulse compresion	$\Delta V_{Sync}/V_{23}$			5	%	

Alignment Instructions

At a video carrier input level of $V_{28/29}$ = 4 mV rms, f_{BT} = 38.9 MHz and a superimposed AGC voltage of V_{15} = 1.5 V the demodulator circuit is aligned until the demodulated video signal at the positive video output is $V_{23\,pp}$ = maximum. Any suitable video test signal may be used for modulation. The AGC voltage V_{15} is then reduced until the video signal is approx. 2 Vpp. By fine alignment with the demodulator coil, the video signal is subsequently brought to a maximum.

Because of the wide maximum, the alignment is not critical.
Fine alignment regarding intercarrier S/N ratio, differential phase or 2 T pulse response is possible too.

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Euro Sound IF						
Static Characteristics						
AGC voltage min. AGC max. AGC	 V_8 V_8	 0 2.6	 0.1 2.85	 0.5 6	 V V	 $V_{9/10}$ = 45 µV$_{rms}$ $V_{9/10}$ = 175 mV$_{rms}$
AGC time contant (pin 8) charge current with quick charge charge current discharge current	 I_8 I_8 I_8	 	 tbf tbf tbf	 	 µA µA µA	 IF level change > 20 dB integral control operation integral control operation
IF input	$V_{9/10}$	5.7	6	6.3	V	
FM sound IF output	V_7		tbf		V	
Sound osc. current	I_{33}		200		µA	
Dynamic Characteristics						
Min. sound IF Input voltage (min. control) TT$_{rms}$	$V_{9\text{-}10}$		45		µV	$V_{7\text{-}3\,dB}$
Max. sound IF Input voltage (max. control) TT$_{rms}$	$V_{9\text{-}10}$		140		mV	$V_{7+3\,dB}$
AGC control range	Δv		70		dB	
FM sound IF output voltage	V_{7rms}		100		mV	$V_{9/10}$ = 10 mV
AF output voltage in AM operation	V_{37}		500		mV	$V_{9/10}$ = 10 mV m = 80%
Noise figure in AM operation	V_{37}		0.3 1		% %	$V_{9/10}$ = 1 mV m = 30% m = 80 %

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Design Notes for FM Operation						
Sound oscillator tank circuit voltage	V_{33rms}	400			mV	$Q_0 > 40$
Input resistance symmetrical	$R_{9/10}$	1.5	2	2.5	kΩ	
Input capacitance symmetrical	$C_{9/10}$	1.5	2	5	pF	
Intercarrier signal to noise ratio (weighted accor. to CCIR 468) f_{SC1} = 5.5 MHz with transmitting sound carrier SC1 – 13 dB (FM-demodulator is SC1 sound IF1)						
	S/N		tbf		dB	$V_{9/10}$ = 10 mV FuBk
	S/N		tbf		dB	$V_{9/10}$ = 10 mV 2.753 MHz-mod.
FuBk-test picture	$\Delta S/N$		tbf		dB	with detuning Δf = – 400 kHz
FuBk-test picture	$\Delta S/N$		tbf		dB	with detuning Δf = + 400 kHz
Intercarrier signal to noise ratio (weighted accor. to CCIR 468) f_{SC1} = 5.74 MHz with transmitting sound carrier SC2 – 20 dB (FM-demodulator is SC2 sound IF2)						
	S/N		tbf		dB	$V_{9/10}$ = 10 mV FuBk
	S/N		tbf		dB	$V_{9/10}$ = 10 mV 2.753 MHz-mod.
	S/N		tbf		dB	$V_{9/10}$ = 10 mV 250 kHz-mod.
FuBk-test picture	$\Delta S/N$		tbf		dB	with detuning Δf = – 400 kHz
FuBk-test picture	$\Delta S/N$		tbf		dB	with detuning Δf = + 400 kHz
Dynm. output resistance SC output	R_7			150	Ω	
Noise figure	F			5	dB	$V_{9/10}$ = 50 dB µV R_G = 800 Ω

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
FM Part						
Static and Dynamic Data						
Input frequency range range	$f_3; f_1$	3		10	MHz	
Input voltage for limiting start (V_{qAF} - 3dB AF)	$V_{3/1}$		20	50	µV	$f_{I3;1}$ = 5.5 MHz; Δf = 30 kHz; f_{mod} = 1 kHz
AF Output voltage	$V_{37/40}$	500	600		mV	$f_{I3;1}$ = 5.5 MHz; Δf = 30 kHz; $V_{I3;1}$ = 10 mV; f_{mod} = 1 kHz
Total distorsion harmonic factor	$THD_{37/40}$			0.2	%	$f_{I3;1}$ = 5.5 MHz; Δf = 30 kHz; $V_{I3;1}$ = 10 mV; f_{mod} = 1 kHz
Total distorsion harmonic factor	$THD_{37/40}$			1	%	$f_{I3;1}$ = 5.46 . . . 5.54 MHz;
AM-Suppression	a_{AM}	55	65		dB	$V_{I3;1}$ = 1 mV . . . 100 mV m = 30%
AM-Suppression	a_{AM}	45	55		dB	$V_{I3;1}$ = 500 µV . . . 1 mV m = 30%
MUTE-bass	a_{MUTE}	70			dB	Δf = 30 kHz; $V_{I3;1}$ = 10 mV; f_{mod} = 1 kHz
Cross talk attenuation AM→FM	$a_{AM/FM}$	70			dB	Δf = 30 kHz; $V_{I3;1}$ = 10 mV; f_{mod} = 1 kHz

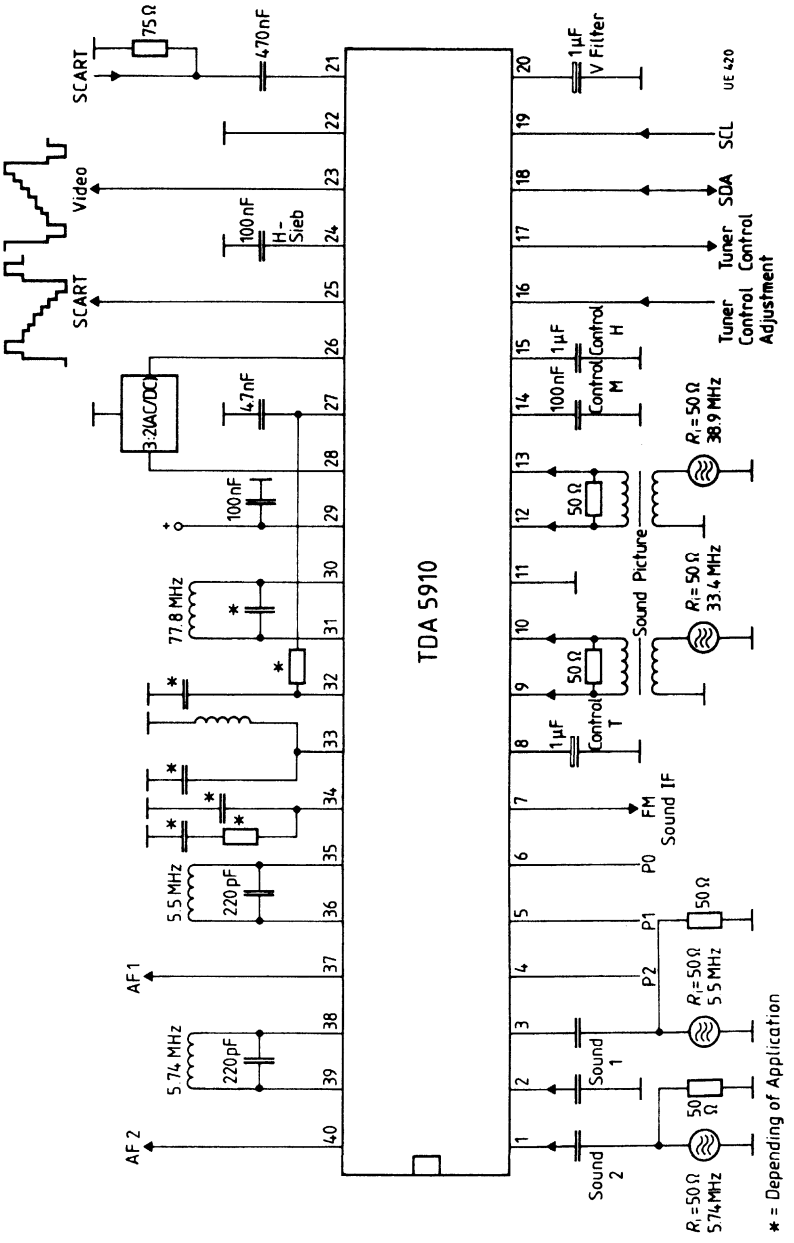
Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Design Notes						
Sound IFinput resist.	$R_{3;1}$		800		Ω	
Demodulator attenuation resist.	$R_{35/36;38/39}$		20		kΩ	
AF output resistance	$R_{37;40}$			200	Ω	
IF residual voltage	V_{IF}		10		mV	without deemphasis
Hum suppression	a_{hum}		tbf			$\Delta V_{37;40}/\Delta V_{29}$; without deemphasis
Coincidence Detector						
Static Data						
Voltage at V-amplitude filter	V_{20}		2.2		V	
Dynamic Data						
Recognition threshold of the coincidence video signal	$V_{28\,pp}$	tbf		tbf	V	V_{15} = 2 V
Design Notes						
Recognition threshold of the video signal signal-to-noise ratio	$S/N\ V_{28}$		tbf		V	V_{28N} = 3 Vpp

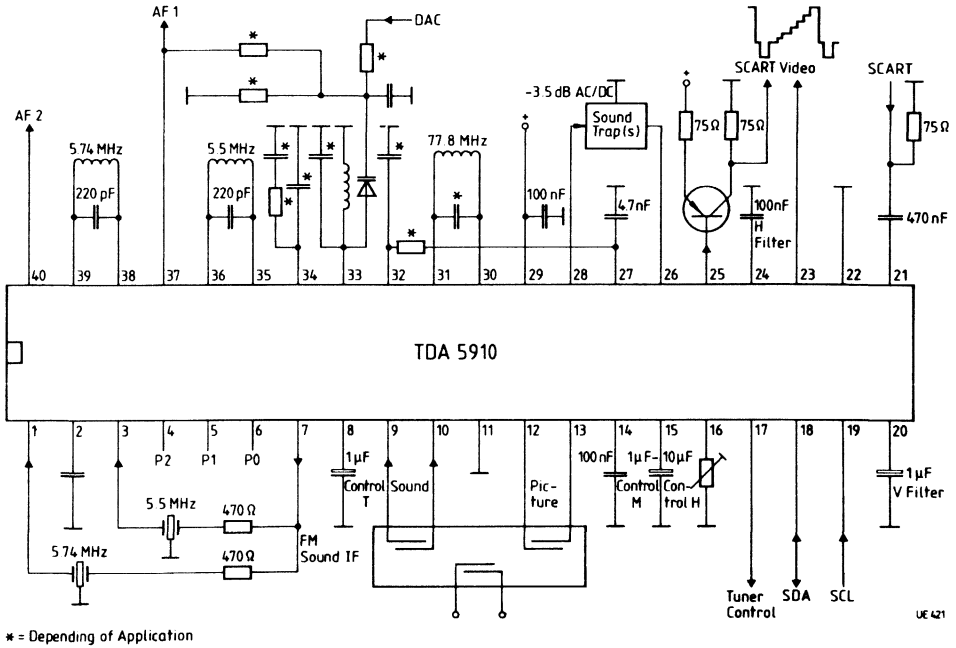
Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
I²C Bus (SCL, SDA)					
SCL, SDA edges					
Rise time	t_R			1	µs
Fall time	t_F			300	ns
Shift register clock pulse SCL					
Frequency	f_{SCL}	0		100	kHz
H-pulse width	t_{HIGH}	4			µs
L-pulse width	t_{LOW}	4			µs
Start					
Set-up time	t_{SUSTA}	4			µs
Bus free time	t_{HDSTA}	4			µs
Stop					
Set-up time	t_{SUSTO}	4			µs
Bus free time	t_{BUF}	4			µs
Data transfer					
Set-up time	t_{SUDAT}	1			µs
Hold time	t_{HDDAT}	1			µs
Inputs SCL, SDA					
Input voltage	V_{QH}	2.4		5.5	V
	V_{QL}	0.3		1	V
Input current	I_{QH}			50	µA
	I_{QL}			100	µA
Output SDA (open collector)					
Output voltage					
R_L = 2.5 kΩ	V_{QH}	4.5		5.5	V
I_{QL} = 3 mA	V_{QL}			0.4	V

Test Circuit



Application Circuit



* = Depending of Application

SIEMENS

Video-IF Amplifier and Demodulator

TDA 5930

Bipolar IC

Features

- Multistandard video IF
- Interference suppression circuitry
- Mean/peak value control
- Area of application: multistandard TV / VCR, mono, stereo
  cable converter, mono, stereo

Type	Ordering Code	Package
TDA 5930	Q67000-A8169	P-DIP-16

Circuit Description

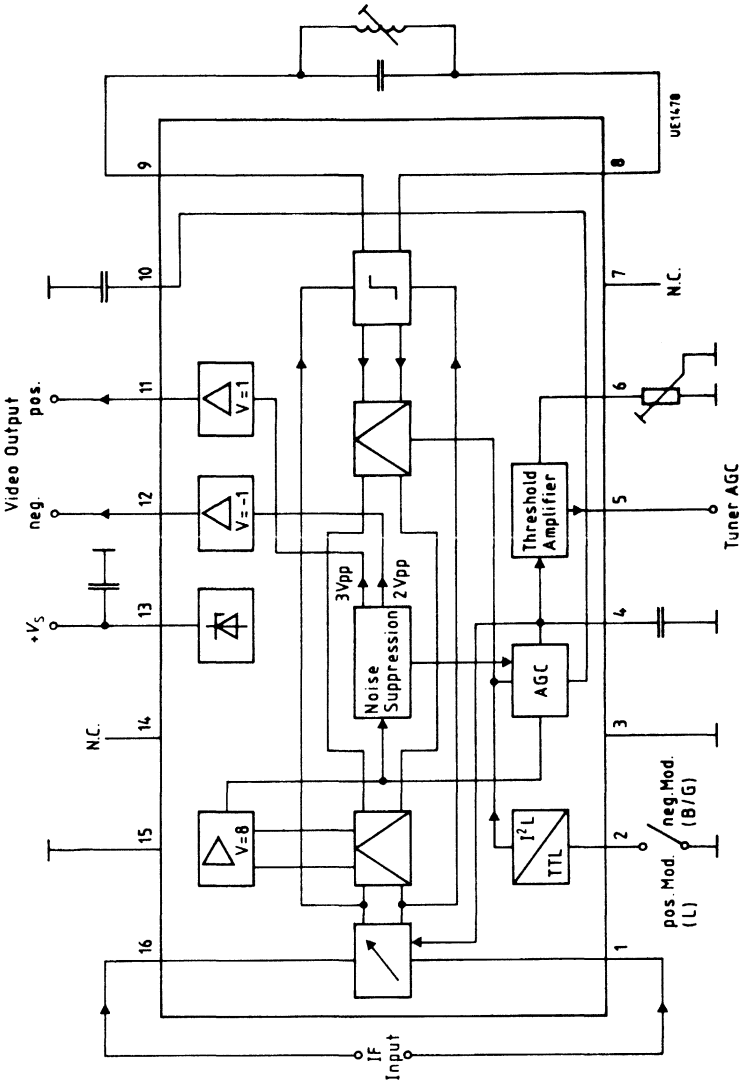
Video IF for all European standards. The analog setting function (delayed tuner AGC threshold) is controlled via a potentiometer.

The IC is suitable for use in Euro- or multi-standard TV sets for mono and stereo application.

The component includes a four-stage, capacitatively coupled, symmetrically designed and controlled amplifier, a limiter with selection, and a mixer for quasi-synchronous demodulation of positive and negative modulated IF signals. In addition a video output amplifier and noise suppression circuitry are included. This output is used for generating the AGC voltage. The AGC for both modulation types has been realized as integral AGC with noise-free peak and mean value detector (only for positive modulation). A delayed tuner AGC with positive AGC direction (increase in tuner AGC voltage $\rightarrow$ increased gain) is derived from the AGC voltage via a threshold amplifier set by means of an external potentiometer.

A positive video output with 3 V_{pp} and a negative video output with 2 V_{pp} are available.

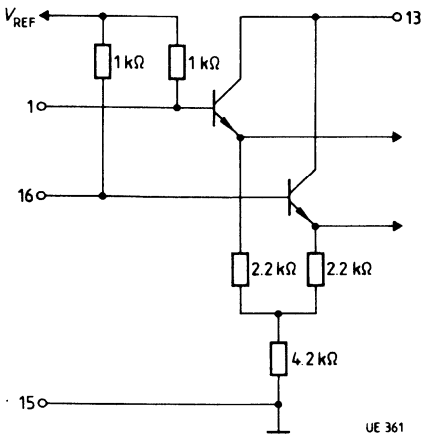
Block Diagram



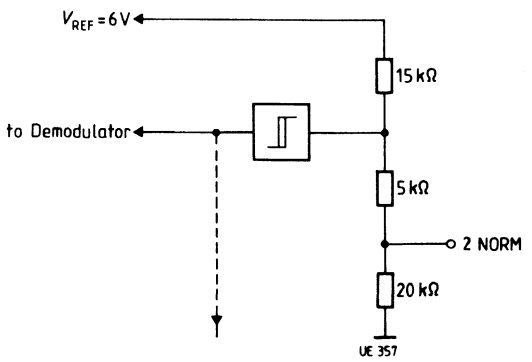
Pin Functions

Pin No.	Function
1	Video IF input
2	Standard switch over B/G-L
3	Ground
4	AGC time constant
5	Tuner AGC output
6	Tuner AGC threshold
7	n.c.
8	Demodulator tank circuit
9	Demodulator tank circuit
10	Low pass (mean value generation)
11	Positive video output
12	Negative video output
13	Supply voltage
14	n.c.
15	Ground
16	Video IF input

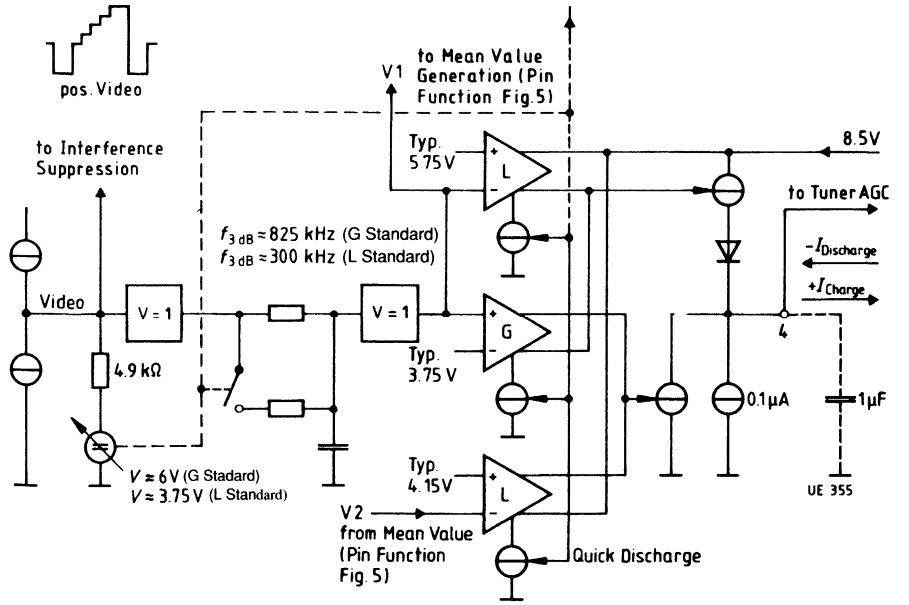
IF Input (Pin 1, 16)



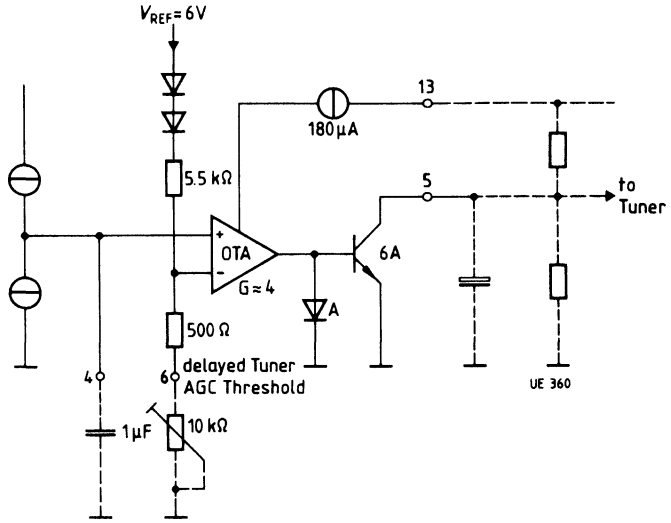
Standard-Switch over B/G-L (Pin 2)



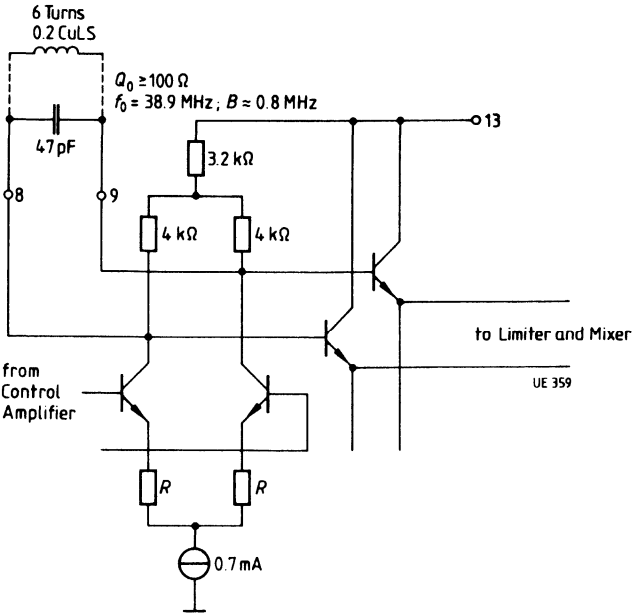
Time Constant AGC (Pin 4)



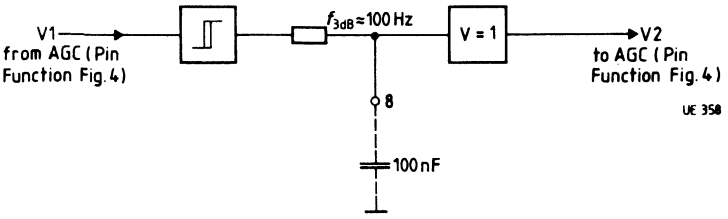
Tuner AGC Threshold and Output (Pin 5, 6)



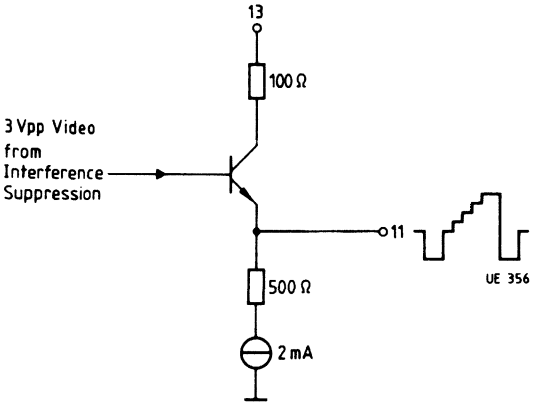
Demodulator Tank Circuit (Pin 8, 9)



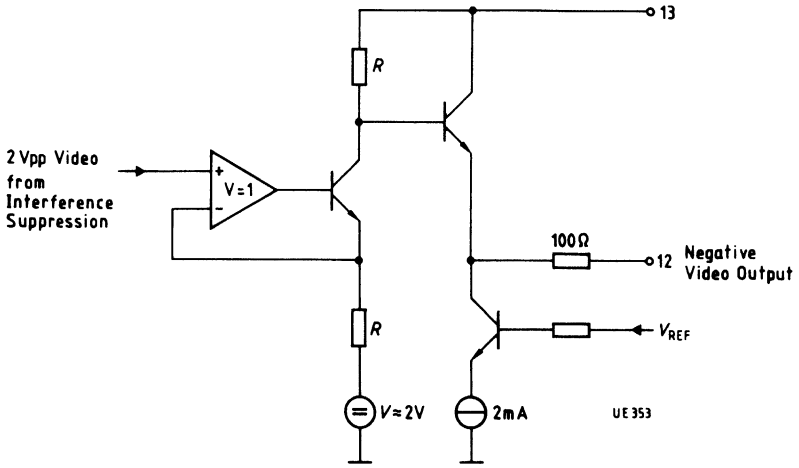
Mean Value Generation (Pin 10)



Video Output (Pin 11)



Negative Video Output (Pin 12)



Absolute Maximum Ratings

T_A = 25 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{13}	0	13.5	V
Pos. video output	I_{11}	– 3	5	mA
Pos. video output	V_{11}	0	10	V
Demodulator tank circuit	V_8/V_9	0	$+V_{13}$	V
Neg. video output	I_{12}	– 3	5	mA
Neg. video output	V_{12}	0	$+V_{13}$	V
Tuner AGC threshold	V_6	0	6	V
Tuner AGC output	V_5	0	$+V_{13}$	V
IF input	V_1/V_{16}	0	6	V
IF control	V_4	0	8.5	V
Standard switch-over	V_2	0	6	V
Auxiliary control	V_{10}	0	6	V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\ SA}$		70	K/W

Operating Range

Supply voltage	V_{13}	10.5	13.5	V
Supply voltage, delayed tuner AGC	V_5	1	13.5	V
Ambient temperature during operation	T_A	0	70	°C
Input frequency range -3dB Input frequency range -0.3dB	f_{IF} f_{IF}	10 30	100 75	MHz MHz

All voltage values are referenced to ground pin 3, 15, if not stated otherwise. The currents are identified according to the source/sink principle.

If the IC is considered a sink (the current flows from the respective pin to ground), it is identified by a negative algebraic sign.
However, if the IC is the source (the current flows form V_8 via the respective pin), it is identified by a positive algebraic sign.

Characteristics

$V_S = V_{13/15} = 12\ V \pm 10\%$; $T_A = 25\ °C$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
DC Characteristics						
Tot. current consumption		37	53	69	mA	$V_{1/16} = 10mV_{rms}$
AGC Voltage (figure 1)						
Min. AGC	V_4	0	0.1	0.5	V	$V_{1/16} = 45\mu V_{rms}$
Max. AGC	V_4	2.6	2.85	4.5	V	$V_{1/16} = 175mV_{rms}$
AGC Time Constant (figure 6) with Neg. Modulation						
Charge current (I_{max}:2)	I_4	0.7	0.9	1.1	mA	$V_4 = 2V$; $V_{11}<5.2V$
Discharge current	$-I_4$	12	17	23	µA	$V_4 = 2V$; $V_{11}>6.3V$
Charge/discharge ratio	V_4	75	105	150		
AGC Time Constant (figure 7) with Pos. Modulation						
Charge current	I_4	5.5	7	8.0	mA	$V_4 = 2V; V_{11}\geq 9V$
Discharge current	$-I_4$	0.1	0.2	0.3	µA	$V_4 = 2V; 4.5V<V_{11}<8.2V$
Discharge current	$-I_4$	270	330	420	µA	$V_4 = 2V; V_{11}<6V$
Charge/discharge ratio	V_4	20000	35000	75000		
Mean Value Generation with Pos. Modulation						
White level	V_{10}	3.9	4.3	4.7	V	$V_{1/16} = 10mV_{rms}$
Zero carrier level	V_{10}	3.3	3.7	4.1	V	$V_{1/16} = 0V; V_4 = 3V$
Tuner AGC threshold	V_6	3.9	4.3	4.7	V	$R_{615} = \infty$
(figure 2)	I_6	550	750	950	µA	$V_6 = 0V$
$I_5 = I_{max}$:2	V_4	2.8	3.1	3.4	V	$R_{6/15} = 10k\Omega$
	V_4	0.35	0.4	0.45	V	
Tuner AGC current	$-I_5$	3.0	4.0	5.0	mA	$V_5 = 0.5V_{13}$
(figure 3,4)						$V_{1/16} = 100mV_{rms}$
						$V_6 = 0.75V$
	$-I_5$	0	-	10	µA	$V_5 = 0.5V_{13}$
						$V_{1/16} = 10mV_{rms}$
						$V_6 = 4.0V$
IF input	V_1, V_{16}	5.7	6.0	6.3	V	
Demodulator tank circuit	V_8, V_9	V_{13}–3.5	V_{13}–3.8	V_{13}–4.1	V	

The characteristics data apply to the supply voltage range V_S stated or in case of alignment to the alignment instructions (see page 622). All static voltages are referenced to ground if not stated otherwise.

The input levels are given as rms values referenced to synchronous peak $f_{PC} = 38.9$ MHz.

Characteristics (cont 'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Pos. Video Output (figure 8)						
Output current	$-I_{11}$	1.7	2.2	2.7	mA	V_{11} = 9V
	I_{11}	4			mA	to ground via R = 1kΩ
Pos. Modulation (L norm)						
White level	V_{11}	5.9	6.6	7.3	V	$V_{1/16}$ = 10mV rms
Zero carrier (sync.)	V_{11}	3.3	3.6	4.0	V	$V_{1/16}$ = 0V; V_4 = 3V
Neg. Modulation (BG norm)						
Sync.pulse level	V_{11}	3.3	3.6	4.0	V	$V_{1/16}$ = 10mV rms
Zero carrier	V_{11}	6.2	6.9	7.6	V	$V_{1/16}$ = 0V; V_4 = 3V
Neg. Video Output (figure 9)						
Output current	$-I_{12}$	1.7	2.2	2.7	mA	$R_L = \infty$
	I_{12}	4			mA	$V_{12} = V_{13}$
Pos. Modulation (L norm)						
White level	V_{12}	V_{13}–5.7	V_{13}–4.95	V_{13}–4.2	V	$V_{1/16}$ = 10mV rms
Zero carrier (sync.)	V_{12}	V_{13}–3.3	V_{13}–2.8	V_{13}–2.4	V	$V_{1/16}$ = 0V; V_4 = 3V
Neg. Modulation (BG norm)						
Synchr. pulse level	V_{12}	V_{13}–3.3	V_{13}–2.8	V_{13}–2.4	V	$V_{1/16}$ = 10mV rms
Zero carrier	V_{12}	V_{13}–5.9	V_{13}–5.2	V_{13}–4.4	V	$V_{1/16}$ = 0V; V_4 = 3V
Switching Voltage (figure 12)						
L = L/E standard	V_2	0		1.8	V	
H = B/G stand. or open	V_2	2.6		6	V	
Dynamic Characteristics						
Min. IF Input Voltage (figure 1)						
(min. gain) PC rms $V_{1/16}$			45	60	µV	V_{11PP} – 1dB
Max. IF Input Voltage (figure 1)						
(max. gain) PC rms		105	140		mV	$V_{1/16}$ V_{11PP} + 1dB
IF control range (**figure 1**)	ΔV	65	70		dB	

Video output voltages (peak-to-peak) PC = 10 mV rms
with neg. modulation = 10%; with pos. modulation and residual carrier<6%

Characteristics (cont 'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Pos. video output (**figure 8**)	V_{11}	2.7	3.0	3.3	Vpp	$R_L \geq 1.5k\Omega$
Change ΔV_{11} by standard switch-over	ΔV_{11}		1	5	%	0V<V_2<2V = B/G Operat. 2.6V<V_2<6V = L Operat.
Changes via operating voltage	$\Delta V_{11}/\Delta V_{13}$		1.5	3	%	10.8V<V_{13}<13.2V
Neg. video output (**figure 9**)	V_{12}	1.95	2.15	2.35	Vpp	$R_L = \infty$
Video output voltage change (**figure 8**) by means of a control range of 55 dB	ΔV_{11}		0.2	0.5	dB	

Design Notes (no 100% final test)

Input resistance (symmetrical)	$R_{1/16}$	1.5	2	2.5	kΩ	
Input capacitance (symmetrical)	$C_{1/16}$		2	5	pF	
Low pass cut-off frequency (**figure 5**)	$f_{-3dB(10)}$	70	100	130	Hz	$C_{10/15}$ = 100nF ± 10%
Intercarrier noise voltage ratio (weighted according CCIR 468) (**figure 13**) with parallel tank circuit; 38.9 MHz, SAW 361 D, f_{SC} = 5.5 MHz (-13dB), demodulator: TBA 120 U						
	S/N		48		dB	$V_{1/16}$ = 10mVPP FuBK mod.
	S/N		17		dB	$V_{1/16}$ = 10mVPP 2.753MHz mod.
FuBK-test chart	$-\Delta S/N$		2		dB	with detuning Δf = − 400kHz
FuBK-test chart	$-\Delta S/N$		11		dB	with detuning Δf = + 400kHz
Dyn. output resistance						
pos. video output	R_{11}	80	115	150	Ω	
neg. video output	R_{12}	100	150	200	Ω	
Noise figure (**figure 14**) $V_{1/16}$ = −45dBm = +62dBμV R_{GEN} = 800Ω	F		5	7	dB	
Video noise voltage ratio (**figure 15**) with PC = 10mVrms						
0dB = 700mVppBA						
unweighted	S/N	50	55		dB	
weighted according to CCIR Rec. 567-1	S/N	55	60		dB	

Characteristics (cont 'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Video frequency response (**figure 16**)					
– 3dB	B_{-3dB}	8	10	13	MHz
– 12dB	B_{-12dB}	15	17	20	MHz
Residual carrier voltage at video output PC = 10mV$_{rms}$ Fundamental wave f = 38.9MHz	V_{11}		3.0	6.0	mV
1. harmonic wave f = 77.8MHz	V_{11}		0.3	0.6	mV
Differential gain CCIR Rec. 567– 1 (**figure 17**) with PC = 10mV peak-to-peak according to stairsignal test	DG		4	6	%
Changes via AGC	$\Delta DG/\Delta v$			1	%
Changes via detuning f_{BT} = 38.9MHz; Δf = ±400kHz	$\Delta DG/\Delta f$			1	%
Differential phase CCIR Rec. 567-1 (**figure 17**) with PC = 10mVrms peak-to-peak according to stairsignal test	DP		1.5	2.5	deg
Changes via AGC	$\Delta DP/\Delta v$			1	deg
Changes via detuning f_{BT} = 38.9MHz; Δf = ±400kHz	$\Delta DP/\Delta f$			2	deg

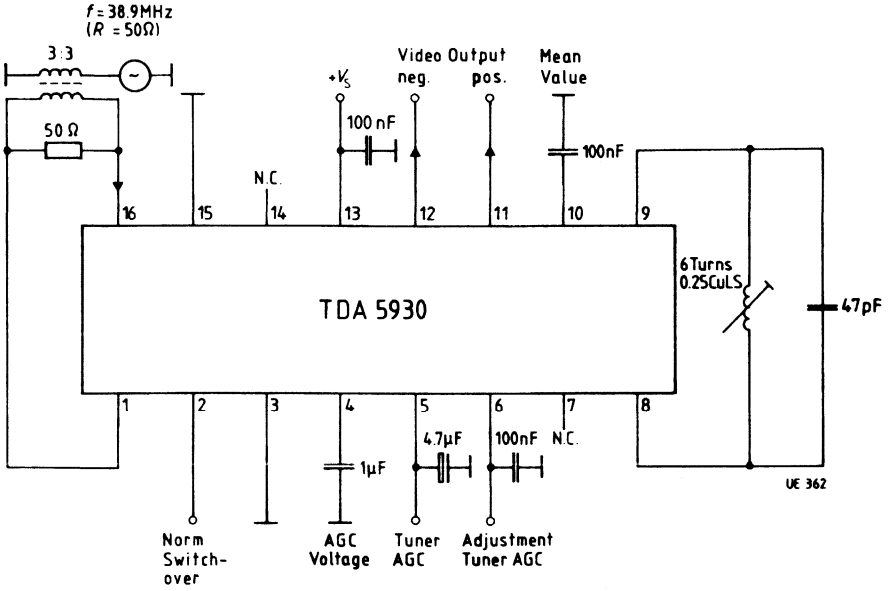
Characteristics (cont 'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Intermodulation ratio **(figure 18)** with f_{IM} =1.07MHz = f_{SC}-f_{CC} with PC =10mV$_{rms}$						
with sound porch -3dB	a_{IM}	32	38		dB	OFWG 3950
with sound porch -20dB	a_{IM}	54	60		dB	OFW 3610
with sound porch -17dB	a_{IM}	51	57		dB	OFWG 1956
Demodulator tank circuit voltage f_{PC} = 38.9MHz; C = 47pF L = 350nH 100 ≤ Q_0 ≤120; Q_B ≈ 60; B ≈ 0.8 ... 1.0MHz	$V_{8/9}$	300	450	600	mV$_{pp}$	
Synchronous pulse	ΔV_{Sync} / V_{11}			5	%	
Temperature drift of the tuner AGC threshold referred to the input voltage				2	dB	I_5 = $I_{5\,max}$/2 caused by the self-heating of the ICs 10 s to 15 min.
Ratio pulse bar tilt to sync. amplitude				4	%	
Reaction time of white level peak setting, L-standard				10	µs	low-pass filter in regulation slope ca. 300 kHz

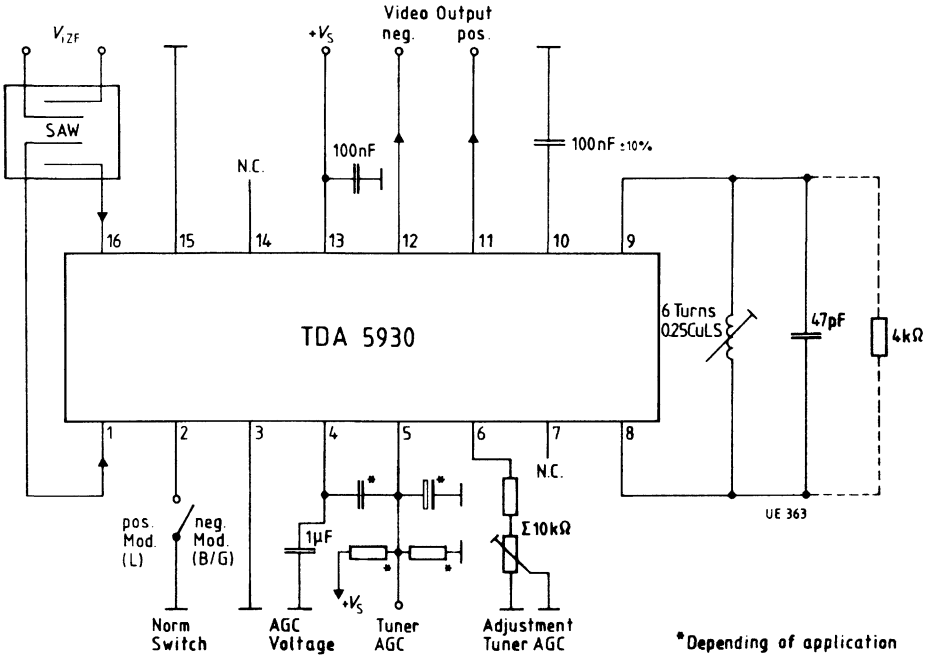
Alignment Instructions

At a video carrier input level of $V_{1/16}$ = 4 mV$_{rms}$, f_{PC} = 38.9MHz, and a superimposed AGC voltage of V_4 = 1.5V, the demodulator tank circuit is preliminarily aligned until a max. video signal V_{11PP} is obtained at the positive video output. Any suitable video test signal can be used for modulation. The AGC voltage V_4 is reduced until the signal is approx. 3V$_{pp}$ and the max. video signal is obtained when fine-aligning the demodulator tank circuit. The alignment is not critical due to relatively large bandwidth of the demodulator tank circuit. Fine- tuning to intercarrier S/N, differential phase or 2T pulse characteristics is possible.

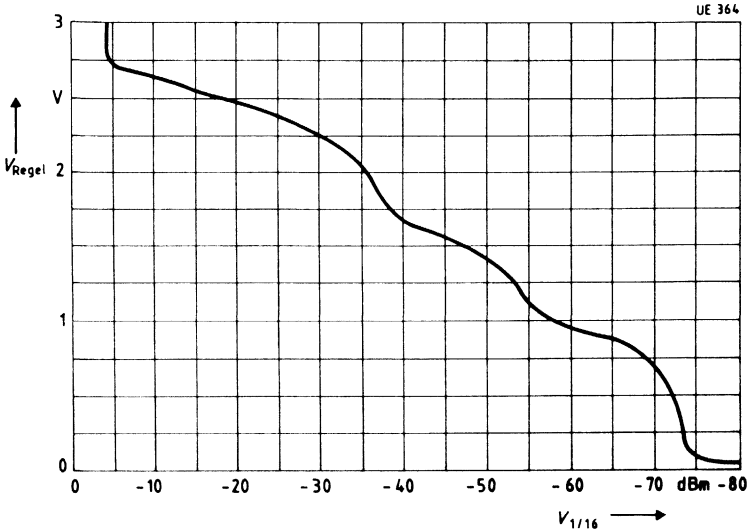
Test Circuit



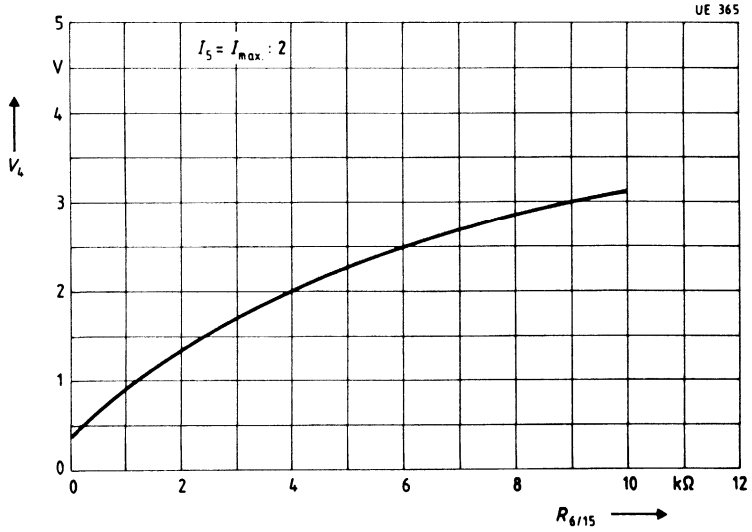
Application Circuit



AGC Voltage

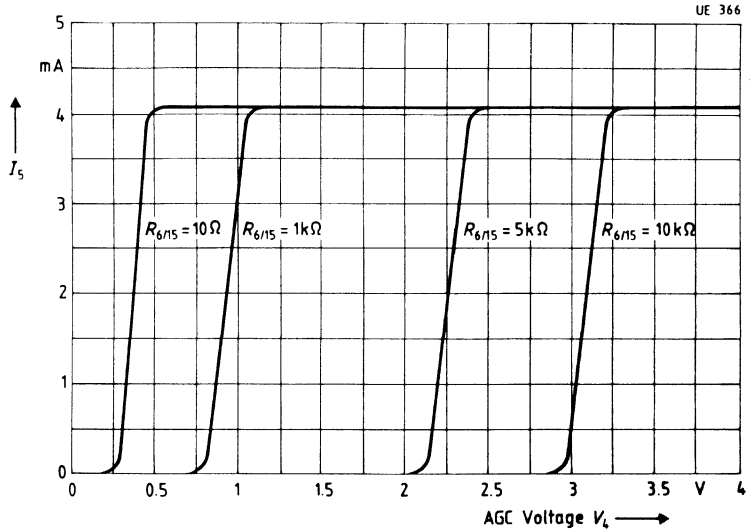


Inset Point AGC Voltage



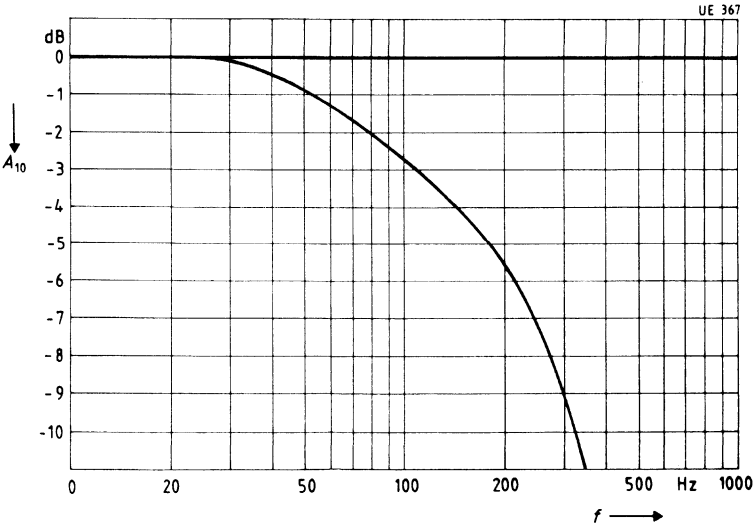
Tuner AGC Current

$I_5 = f(V_4)$

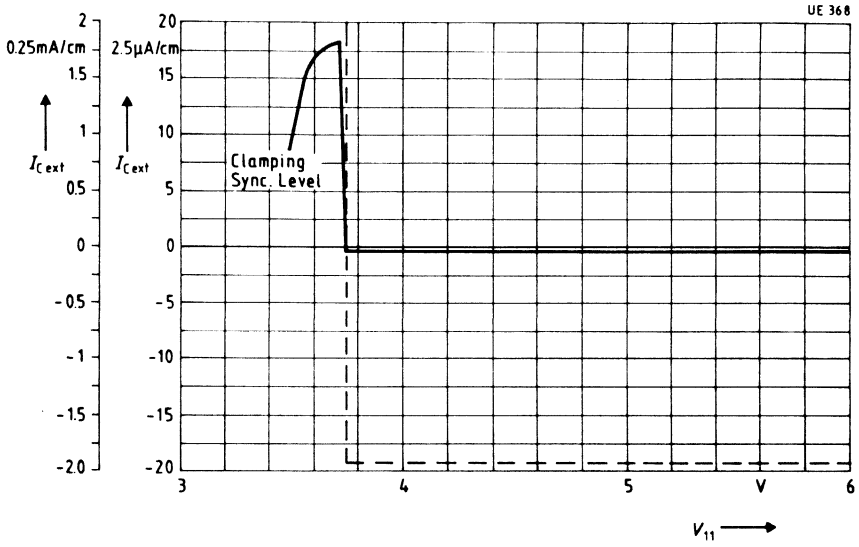


Low-Pass Cut-Off Frequency (pin 10)

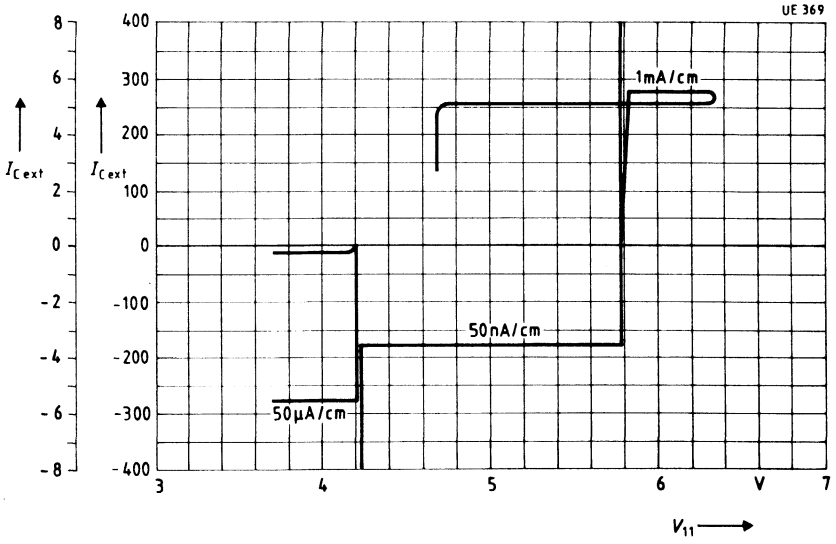
Measurement condition: ext. modulation: 10 Hz - 1 kHz sine 30 % AM
video generator: ext. negative set-up on half sync level, field off



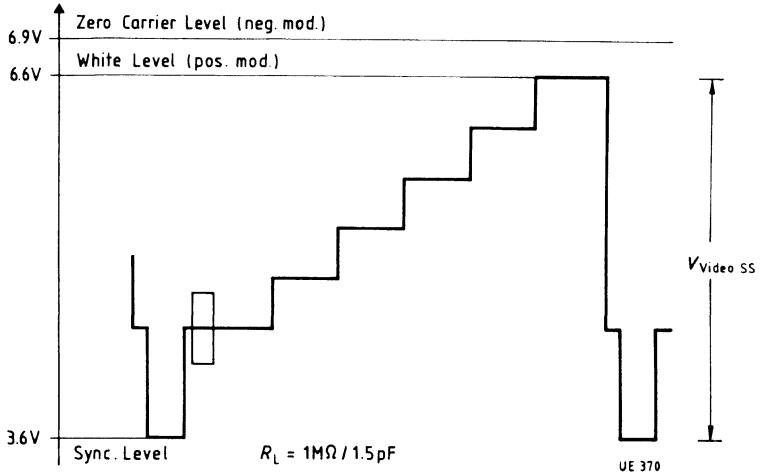
AGC Time Constant Neg. Modulation



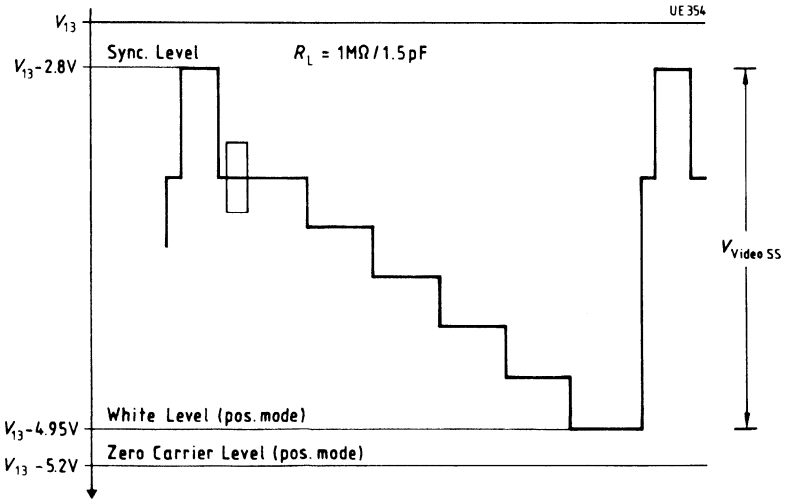
AGC Time Constant Pos. Modulation



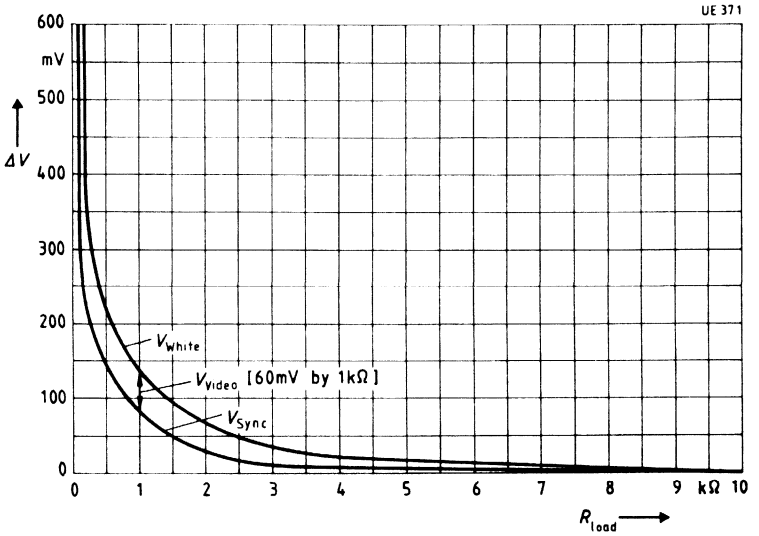
Pos. Video Output (pin 11)



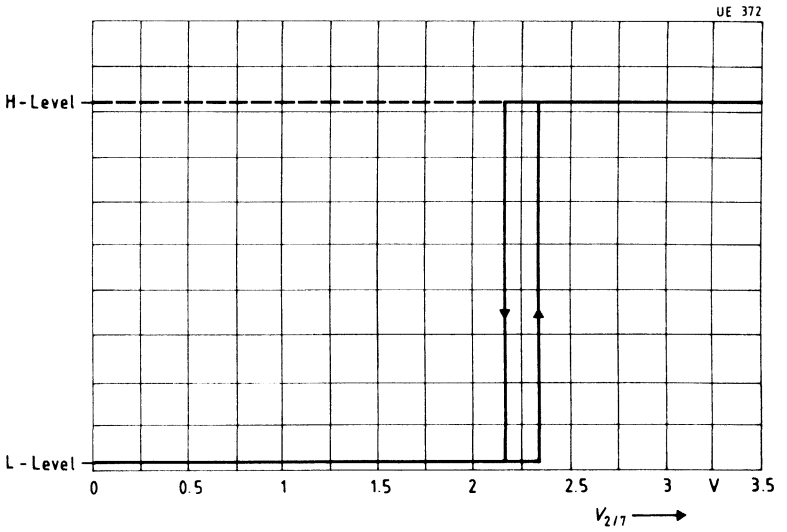
Neg. Video Output (pin 12)



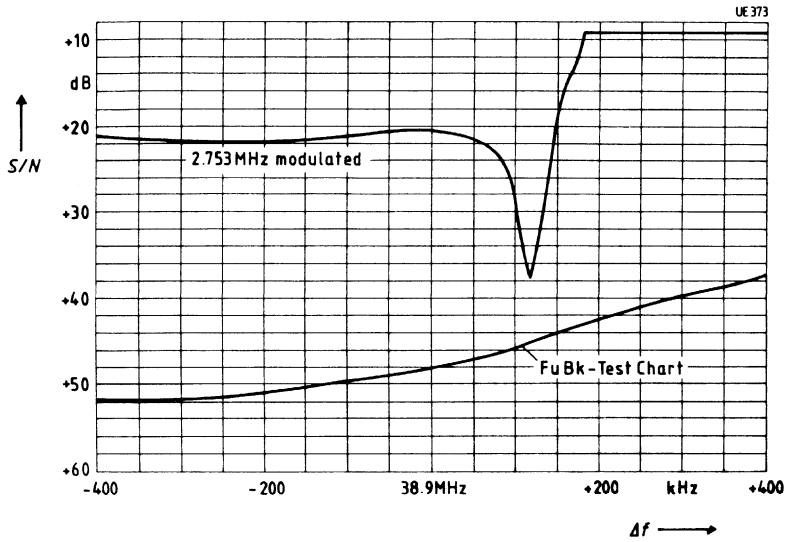
Voltage Dependent Load at Video Output



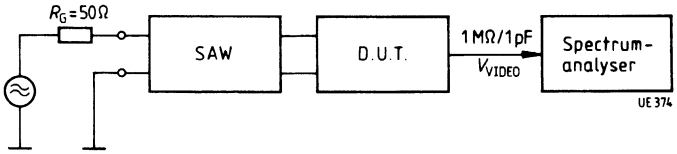
Switching Voltage



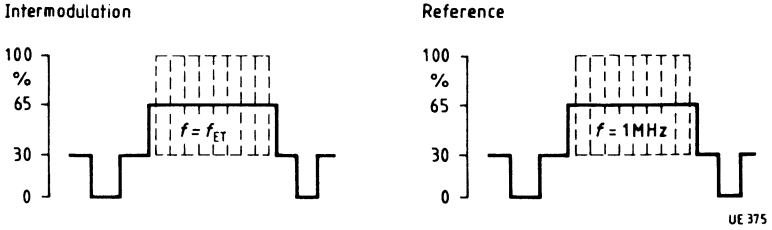
Intercarrier Interference Voltage
(weighted according to CCIR 468)



Measurement Configuration



Test signal: f_{VS}= 38.9 MHz with test signal modulated with 10% residual carrier; sound carrier - 13 dB (transmitter side)



Intermodulation ratio: $$a_{IM} = 20\ lg \frac{V_{VIDEO}\ (f = 1MHz)}{V_{VIDEO}\ (f = f_{TT} - f_{FT})}$$

The 50% IRE signal with ± 50% IRE color carrier corresponds to Cyan with 75% color saturation

SIEMENS

TV Stereo Tone Control IC with Quasi-Stereo Section, Channel 1/2 Switch, SCART Input, and I²C Bus Control

TDA 6200

Preliminary Data

Bipolar IC

Features

- Treble, bass, balance, and volume control by means of an integrated digital-to-analog converter
- Quasi-stereo circuit during mono operation
- Stereo basewidth expansion during stereo operation
- Physiological volume control
- Channel 1/2 switch-over during dual audio transmission
- SCART connection
- Control of all functions via the I²C bus and the bidirectional 4 level line of the TDA 6600-2 (stereo demodulator IC)
- LED driver
- Volume control range 80 dB
- Treble, bass control ± 12 dB
- Channel separation min. 60 dB, cross-talk rejection min. 60 dB
- Parasitic voltage spacing up to 78 dB

Type	Ordering Code	Package
TDA 6200	Q67000-A2461	P-DIP-28

The TDA 6200 is comprised of a SCART switch-over, channel 1/2 switch-over, quasi-stereo circuit, stereo basewidth expansion, physiological volume control, a treble, bass, and volume control of the injected AF signals as well as an LED driver. The IC is controlled by means of an I²C bus serial interface as well as by the bidirectional 4 level line from the TDA 6600-2. The component is used for AF sound signal processing in stereo TV sets.

Circuit Description

The monolithically integrated circuit is comprised of three sections:

1. AF input analog switch for SCART and channel 1/2 switch-over
2. Sound and volume control with quasi-stereo, physiology and stereo basewidth expansion section
3. Control section including the I^2C bus, 4 level line and digital-to-analog converter

1. A two-channel AF analog switch is used to switch from standard TV operation to the SCART playback mode. An additional analog switch is applied for the channel 1/2 switch-over during multichannel transmission. During standard TV operations, this switch will be functional during two-channel transmission and/or SCART playback if the Kbit has been set accordingly.

2. The quasi-stereo section in the signal path is applied to generate an acoustic sound impression similar to stereo during the mono signal. This circuitry section is comprised of one op amplifier per channel. While one amplifier is provided with an internally regulated gain factor of – 1, the second amplifier can be switched between a gain factor of – 1 and a freely selectable gain factor provided by means of external components. The quasi-stereo effect is achieved by forwarding two different types of signals to the input of the second amplifier. While a standard phase AF signal is forwarded via an external band stop filter, a phase inverted signal is forwarded via an external band filter. The attenuation of these networks is compensated by the op amplifier. The result is the generation of a largely amplitude-linear signal, however, turned by 180° in its phase during medium frequencies. This section of the circuit can be switched off.
   The sound and volume control section is comprised per stereo channel of 3 op amplifiers with electronic potentiometers and/or switches. By using one external capacitor each for the bass and treble control, 31 different levels for emphasis and deemphasis can be set for the bass and treble control during low and/or high frequencies. The subsequent stage enables a switch-controlled expansion of the basewidth. When the basewidth expansion has been switched on, an anti-phase cross-talk of approx. 60% will occur at an input frequency of approx. 300 Hz. The frequency to be applied as well as the percentage of cross-talk are determined by an external RC combination. The volume control, separate for each channel, is comprised of 64 stages each. As a result, the balance control can be realized by using different settings for the channels.

   A physiological volume characteristics is achieved by connecting the volume setting with the treble/bass control. For this purpose, the mean value of the two volume control settings is used. The physiology section can be switched off.

   Subsequent to the connection of the supply voltage, the AF output voltage will be delayed by a delay circuit until all voltages are stabilized. In this manner, interfering crackling noises are prevented.

3. The integrated circuit is controlled by means of an I²C bus interface and a 4 level line from the stereo decoder TDA 6600-2. Via this line the evaluation circuit of the TDA 6600-2 provides the necessary information with respect to the 3 modes mono, dual audio, and stereo by means of three different DC voltage levels. For a compulsory (manual) mono mode, a fourth DC voltage level in opposite direction can be used by the TDA 6600-2. This DC voltage level is programmed via the I²C bus interface of the TDA 6200. The system clock for the input SCL of the I²C bus interface is provided by the processor. Pin SDA functions as data input. It can also supply the setting of the identification signal decoder established via the 4 level output and/or an acknowledge message.

   The data forwarded by the processor are controlled by the I²C bus and subsequently filed in registers according to their functions (latch 1-6).

   If the bus is free (t off time), both lines will be in the marking state (SDA, SCL are HIGH). Each message begins with the start conditions of SDA returning into LOW, while SCL remains HIGH. All additional information transfer takes place during SCL = LOW, and the data is forwarded to the control with the positive clock edge. However, if SDA returns to HIGH, while SCL is in HIGH, the message is ended since the circuit acknowledges a stop condition.

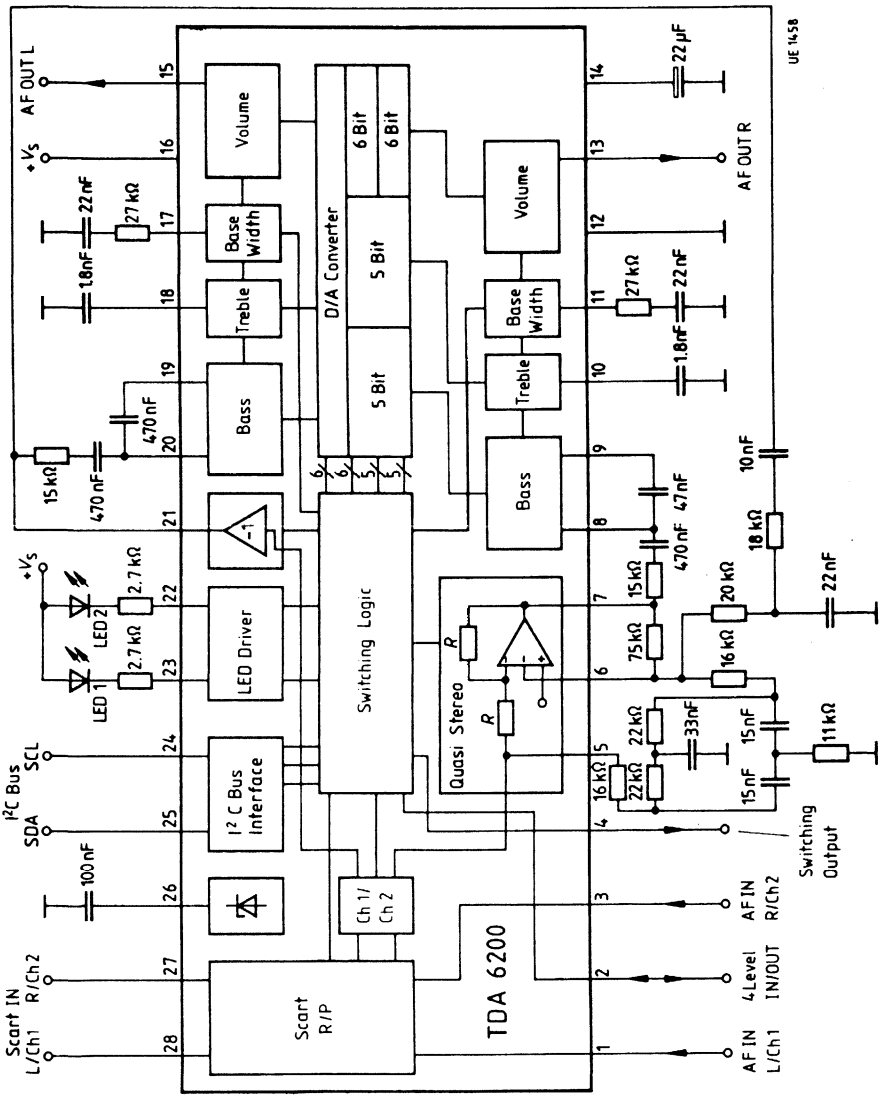
   The logic functions according to the tables on pages 643-645 . All messages are transmitted byte-by-byte, followed by a 9th clock pulse, while the control returns the SDA line to LOW (acknowledge condition). In the read mode, the processor transmits the acknowledge bit (will not be checked by the tone control). The first byte is comprised of 7 address bits used by the processor to select the tone control among several peripheral components (chip select). The 8. bit establishes the direction of the subsequent data flow (read/write bit). The 1. and 2. bit of the data bytes determine which latch will be called up (sub-address).

   The volume information is set with 6 bits (64 positions); the treble and bass control with 5 bits of which the 1. bit (4. bit of the byte) is the sign bit. The 4 bits of the digital-to-analog converter provide 31 different setting levels. The two volume bytes (left, right) and/or treble and bass bytes have to be transmitted in successive order, since they have the same sub-address. The two bytes for the switching function are subdivided into an AF setting byte and a byte for the operation of the SCART jack.

   If the R/W bit = 1 is set during chip addressing, the I²C bus operates in the transmission mode. The momentary position of the stereo decoder (corresponds with the status of the 4 level line) is transmitted.

   The two LED driver outputs enable the display of stereo, mono or dual audio transmission and/or the SCART playback mode.

Block Diagram



Pin Functions

Pin No.	Function
1	AF input for signal from matrix section of TDA 6600-2
2	Bidirectional 4 level control line between TDA 6200 and TDA 6600 used to transmit information with respect to dual audio, mono, stereo and compulsory mono mode
3	AF input for signal from matrix section of TDA 6600-2
4	Switching output to control additional functions (open collector), in turn controlled via I^2C bus
5	Low-impedance output to control the quasi-stereo network
6	Inverted input of the quasi-stereo op
7	Low-impedance output of quasi-stereo op, controls bass control
8, 9	Connections for external capacitor for right bass control $f_{-3\,dB} \sim 1/C_{8,9}$
10	Connection for external capacitor for right treble control $f_{-3\,dB} \sim 1/C_{10}$
11	Connection for network of stereo basewidth expansion percentage of cross- talk $\sim 1/R_{11}$ $f_{-3\,dB} = \frac{1}{2\,\pi\,C_{11}\,(R_{11} + 1\ k\Omega)}$
12	GND
13	AF output right (emitter follower)
14	Decoupling for internal DC operation points. Capacitor also determines the duration of the switch-on delay when connecting V_{16}.
15	AF output left (emitter follower)
16	Supply voltage
17	Connection for network of stereo basewidth expansion percentage of cross- talk $\sim 1/R_{17}$ $f_{-3\,dB} = \frac{1}{2\,\pi\,C_{17}\,(R_{17} + 1\ k\Omega)}$
18	Connection for external capacitor of left treble control $f_{-3\,dB} \sim 1/C_{18}$
19, 20	Connections for external capacitor of left bass control $f_{-3\,dB} \sim 1/C_{19,20}$
21	Low-impedance output to control the quasi-stereo network and the left bass control
22	LED driver output for LED 2 (open collector with current limiter)
23	LED driver output for LED 1 (open collector with current limiter)
24	Clock frequency input of I^2C bus control (Inter-IC)
25	Data input/output of I^2C bus control
26	Reference voltage of typ. 6 V
27	AF input of SCART interface
28	AF input of SCART interface

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	0	16	V
Reference current	I_{26}	0	2	mA
DC voltage	$V_{1, 2, 3}$	0	V_S	V
DC voltage	$V_{6, 8, 9}$	0	V_S	V
DC voltage	$V_{10, 14, 18}$	0	V_S	V
DC voltage	$V_{19, 20, 22}$	0	V_S	V
DC voltage	$V_{23, 24, 25}$	0	V_S	V
DC voltage	$V_{27, 28}$	0	V_S	V
DC current	$I_{4, 5, 7}$	0	2	mA
DC current	$I_{11, 13, 15}$	0	2	mA
DC current	$I_{17, 21}$	0	2	mA
Junction temperature	T_j		150	°C
Storage temperature range	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\ SA}$		60	K/W

Operating Range

Supply voltage	V_S	8	15.75	V
Ambient temperature	T_A	0	70	°C
Input frequency	f_i	0	20	kHz

Characteristics
V_S = 15 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_{16}		55	80	mA	LEDs OFF
Reference voltage	V_{26}	5.4	6	6.6	V	
Max. gain AF input/AF output L byte = BF; KL[2] byte = C0	G_{max}	– 2	0	2	dB	SC = 0; phys = 0; RK[1] = 0; Q-S/Bw = 0
SCART input/ AF output L byte = BF; KL byte = C0	G_{max}	– 2	0	2	dB	SC = 1; phys = 0; RK = 0; Q-S/Bw = 0
Min. gain AF input/AF output L byte = 80; KL byte = C0	G_{min}			– 80	dB	SC = 0; phys = 0; RK = 0; Q-S/Bw = 0
SCART input/ AF output L byte = 80; KL byte = C0	G_{min}			– 80	dB	SC = 1; phys = 0; RK = 0; Q-S/Bw = 0
Wow and Flutter L-R	$\Delta a_{L\text{-}R}$			– 2	dB	
Bass emphasis*) KL byte = C0 + DF	$G_{B\,max}$	9	12		dB	f_i = 40 Hz
Bass deemphasis KL byte = C0 + CF	$G_{B\,min}$		– 12	– 10	dB	f_i = 40 Hz
Treble emphasis*) KL byte = DF + C0	$G_{T\,max}$	8.5	12		dB	f_i = 15 Hz
Treble deemphasis KL byte = CF + C0	$G_{T\,min}$		– 12	– 10	dB	f_i = 15 Hz
Input voltage*) SCART, AF	$V_{I\,rms}$	1			V	any KL byte
Input voltage*) SCART, AF	$V_{I\,rms}$	3.5			V	KL byte = CX
Permissible gain quasi-stereo op	$G_{7/6}$			30	dB	Q-S/Bw = 1
Channel separation	$a_{L\text{-}R}$	60			dB	Q-S/Bw = 0; RK = 0
Antiphased cross talk with basewidth ON	$CT_{L\text{-}R}$	45	60	75	%	stereo; RK = 1

*) refer to page 641
[1]) RK ≡ room accustics
[2]) KL ≡ tone

Characteristics (cont,d)
V_S = 15 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Cross-talk rejection SCART switch	$a_{AF/SF}$	60			dB	V_I rms = 2 V
Ch1/Ch2 switch	$a_{CH\ 1/2}$	60			dB	V_I rms = 2 V; dual audio
Total harmonic distortion	$THD_{13/15}$			1	%	any KL[1] byte V_I rms = 1 V
Total harmonic distortion DIN 45 500*)	$THD_{13/15}$		0.3	0.6	%	KL byte = CX; V_I rms = 1 V
Disturbance voltage spacing f_i = 20 Hz – 20 kHz	$a_{S/N}$			78	dB	DIN 45 405; V_I rms = 1 V L byte = BF; KL byte = C0
Disturbance voltage at output f = 20 Hz – 20 kHz	$a_{S/N}$		120	150	µV	L byte = BF; KL byte = C0
				50	µV	L byte = AC; KL byte = C0
			10	20	µV	L byte = 94; KL byte = C0
Noise voltage CCIR DIN 45 405	V_n			650	µV	L byte = BF KL byte = DF + C0
Deviation in amplitude when tone control is in linear position	ΔG		± 0.5	± 1.5	dB	KL byte = C0 f_i = 40 Hz – 15 kHz
Volume decontrol for max. phys.	V_O/V_I		– 30		dB	phys = 1
Attenuation during MUTE mode	a_{MUTE}	80			dB	M1 = 1
Switching output	$V_{4\ ON}$			0.5	V	I_L = 1 mA
	$I_{4\ OFFI}$			1	µA	
LED driver	$I_{22,23}$			7.5	mA	LED ON
	$V_{22,23}$			1.5	V	$I_{22/23}$ = 7.5 mA
	$I_{22,23}$			50	µA	LED OFF
4 level line Input voltage	V_{I2}	0		1.8	V	recognizes mono
	V_{I2}	2.4		3.9	V	recognizes dual
	V_{I2}	5.2		6.6	V	recognizes stereo
Input current	V_{I2}			3	µA	
Compulsory mono	V_{O2}			0.2	V	M2 = 1; I_2 = 1 mA

*) refer next page

1) KL ≡ tone

Characteristics (cont,d)
V_S = 15 V; T_A = 25 °C

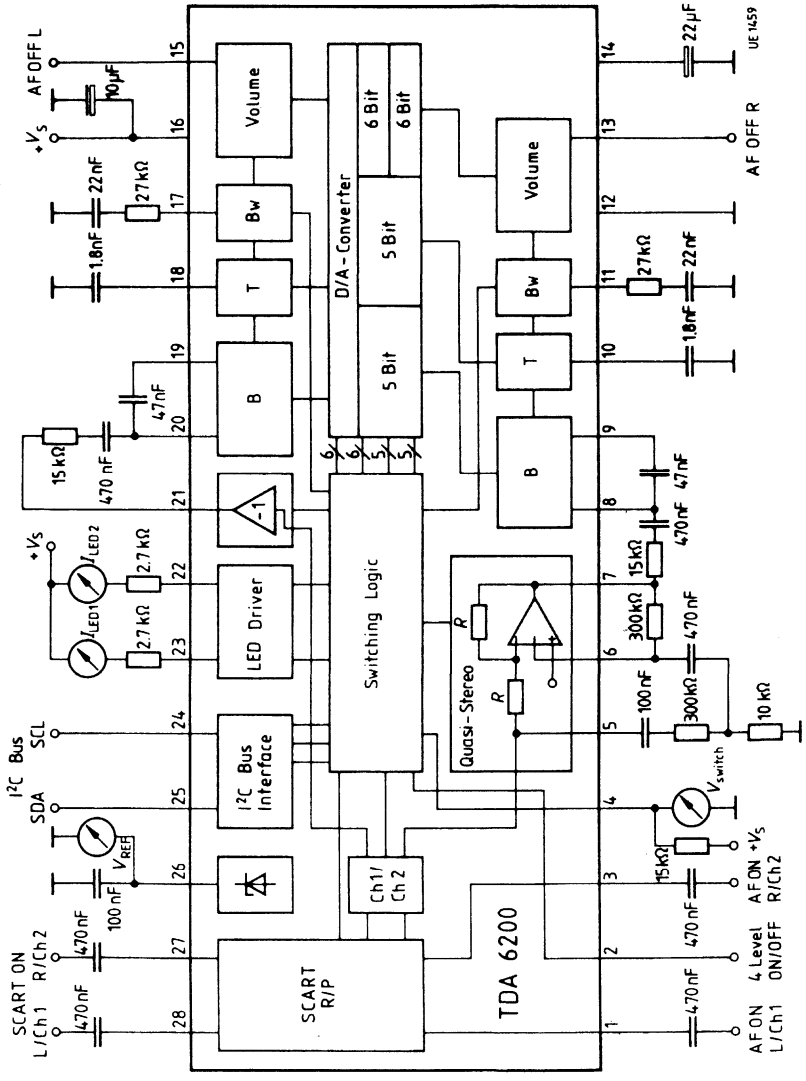
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
I²C Bus (SCL, SDA)					
SCL, SDA Edges					
Rise time	t_R			1	µs
Fall time	t_F			0.3	µs
Shift Register Clock Pulse SCL					
Frequency	f_{SCL}	0		100	kHz
H-pulse width	t_{HIGH}	4			µs
L-pulse width	t_{LOW}	4			µs
Start					
Set-up time	t_{SUSTA}	4			µs
Hold time	t_{HDSTA}	4			µs
Stop					
Set-up time	t_{SUSTO}	4			µs
Bus free time	t_{BUF}	4			µs
DataTransfer					
Set-up time	t_{SUDAT}	1			µs
Hold time	t_{HDDAT}	1			µs
Inputs SCL, SDA					
Input voltage	V_{IH} V_{IL}	2.4 0.3		5.5 1	V V
Input current	I_{IH} I_{IL}			50 100	µA µA
Output SDA (open collector)					
Output voltage R_L = 2.5 kΩ; I_{QL} = 2 mA	V_{QH} V_{QL}			5.5 0.4	V V

The data marked with an asterisk*) depend on the supply voltage.
With lower V_S the input voltage decreases accordingly.

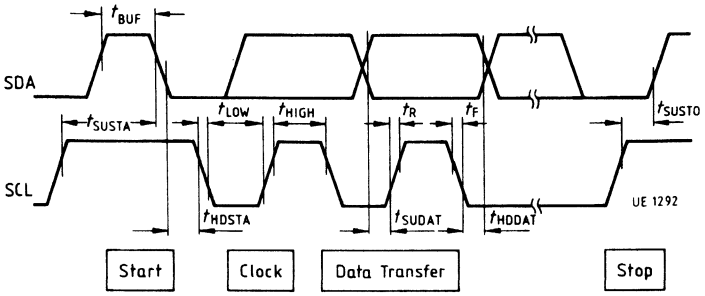
Characteristics
V_S = 15 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Design-Related Characteristics					
Input impedance SCART	$R_{I\,27,28}$	35			kΩ
Input impedance AF	$R_{I\,1,3}$	35			kΩ
Output impedance	$R_{Q\,5,7,21}$			200	Ω
Output impedance AF output	$R_{Q\,13,15}$			200	Ω
Internal resistance Bw	$R_{I\,11,17}$			1	kΩ

Measurement Circuit



I²C Bus Timing Diagram



t_{SUSTA}	Set-up time (start)
t_{HDSTA}	Hold time (start)
t_{HIGH}	Pulse width (clock)
t_{LOW}	Pulse width (clock)
t_{SUDAT}	Set-up time (data transfer)
t_{HDDAT}	Hold time (data transfer)
t_{SUSTO}	Set-up time (stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

The listed times are referenced to the V_{IH} and V_{IL} values.

Software

The following data format is used:

1) **Chip Address**

MSB							LSB	
1	0	0	0	0	0	0	R/W	ack.

MSB will be transmitted first
R/W = 0 IC in the receiving mode

2) **Data Bytes with Sub-Addresses**

a) Volume

MSB							LSB	
1	0	V05	V04	V03	V02	V01	V00	(left) +
1	0	V15	V14	V13	V12	V11	V10	(right)

The two bytes are always transmitted in successive order
V × 5 = MSB
V × 0 = LSB

1	0	0	0	0	0	0	0	min. volume
1	0	1	1	1	1	1	1	max. volume

b) Tone

MSB							LSB	
1	1	X	HV	H3	H2	H1	H0	+
1	1	X	TV	T3	T2	T1	T0	

The two bytes are always transmitted in successive order
HV or TV are sign bits
H3 or T3 = MSB
H0 or T0 = LSB

1	1	X	0	1	1	1	1	min. treble or bass
1	1	X	X	0	0	0	0	linear treble or bass
1	1	X	1	1	1	1	1	max. treble or bass

Software

c) AF set byte

MSB							LSB
0	0	M1	M2	Ch1/2	RK	Phys	Q-S/Bw

M1	= 1	Muting for AF output
M1	= 0	AF ON
M2	= 1	Compulsory mono (via 4 level line)
M2	= 0	Standard operation for identification signal decoder
Ch1/2	= 0	During dual audio mode, channel 1 at AF output
Ch1/2	= 1	During dual audio mode, channel 2 at AF output (only active with dual audio via 4 level line or during SCART playback and Kbit = 1)
RK	= 1	Space sound ON; TV operating mode: Quasi-stereo during mono and dual audio or stereo basewidth expansion during stereo transmission – automatic switch–over via 4 level line SCART playback mode: stereo basewidth expansion ON
RK	= 0	Stereo basewidth expansion and quasi-stereo OFF
Phys	= 1	Physiological volume control ON
Phys	= 0	Physiological volume control OFF
Q-S/Bw	= 1	TV operating mode: Quasi-stereo and stereo basewidth expansion ON SCART playback mode: stereo basewidth expansion ON
Q-S/Bw	= 0	Quasi-stereo and stereo basewidth expansion OFF

d) SCART set byte

MSB							LSB
0	1	SC	Sch	Ch	X	X	X

SC	= 1	SCART playback mode; SCART input connected with AF output
SC	= 0	Standard operation
Sch	= 1	Switching output ON (open collector)
Sch	= 0	Switching output OFF (output can e.g. be used for switch–over from recording to playback mode in the video section)
Ch	= 1	Playback of SCART dual transmission; channel selection via Ch1/2 bit for AF output
Ch	= 0	AF output operates in stereo mode. Playback of SCART stereo (mono) transmission.

Note:

The AF section is automatically controlled by the 4 level line. Compulsory mono M2 is given priority. After Power-ON-Reset all latches are set at 0 (volume min., tone linear, . . .); only the function Q-S/Bw is set at 1.

Software

3) **Transmission Mode**

requires new chip addressing with R/W bit = 1.

MSB							LSB
St	D	X	X	X	X	X	X

St	D	
1	1	Decoder recognizes mono
0	1	Decoder recognizes stereo
1	0	Decoder recognizes dual
0	0	Does not occur (internally suppressed)

The transmission function is not required for the operation of the IC. Instead this function is used to inform the µC about the status of the identification signal decoder to enable additional functions.

LED Driver

TV operating mode:

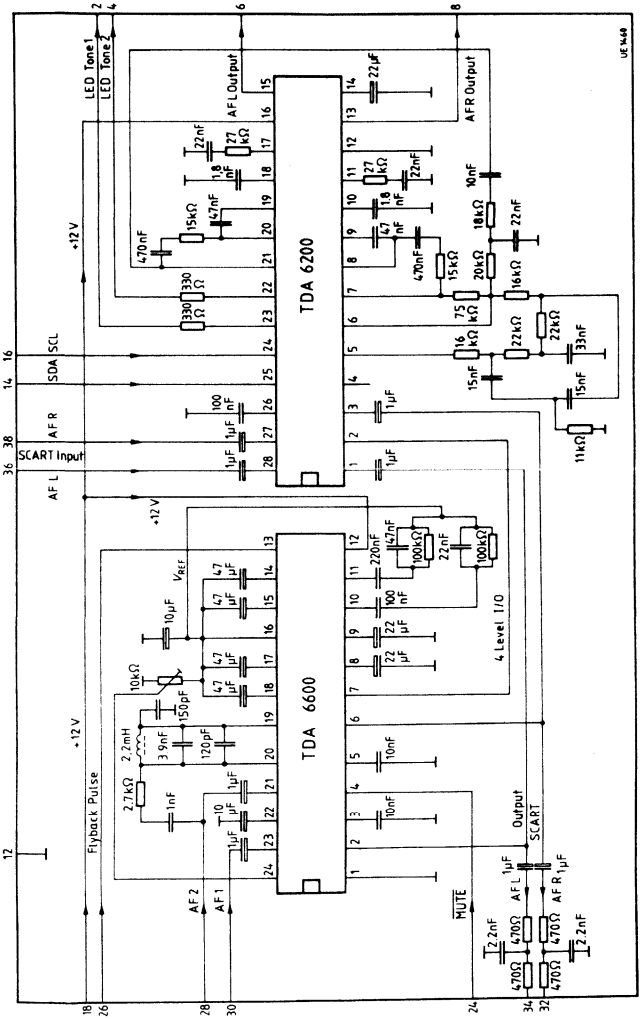
4 level line	Ch1/2 bit	LED 1	LED 2
Mono	X	OFF	OFF
Stereo	X	ON	ON
Dual	0	ON	OFF
Dual	1	OFF	ON

SCART playback mode:

SC bit	Ch bit	Ch 1/2 bit	LED 1	LED 2
1	0	X	ON	ON
1	1	0	ON	OFF
1	1	1	OFF	ON

Application Circuit

Stereo Decoder, Matrix and Tone Control



SIEMENS

TV Stereo Decoder with Matrix — TDA 6600-2

Preliminary Data — **Bipolar IC**

The TDA 6600-2 includes an advanced decoder for the identification signals for the multichannel TV sound systems according to the dual-carrier system as well as a matrix switched by the decoder to provide the L-R-information.

Features

- Increased switching reliability and recognition by means of two PLLs for stereo (117 Hz) and / or dual channel (274 Hz)
- Separate bandwidth selection for dual-tone (pins 17-18) and stereo (pins 14-15)
- Separate setting for the PLL time constants for dual-tone (pin 10) and stereo (pin 11)
- Adjustable cut level for dual-tone (pin 8) and stereo (pin 9)
- Cross-talk rejection independent of external component accuracy
- Adjustment to minimal cross-talk level through external DC voltage
- Suitable for TV sets with a 15625-Hz signal.

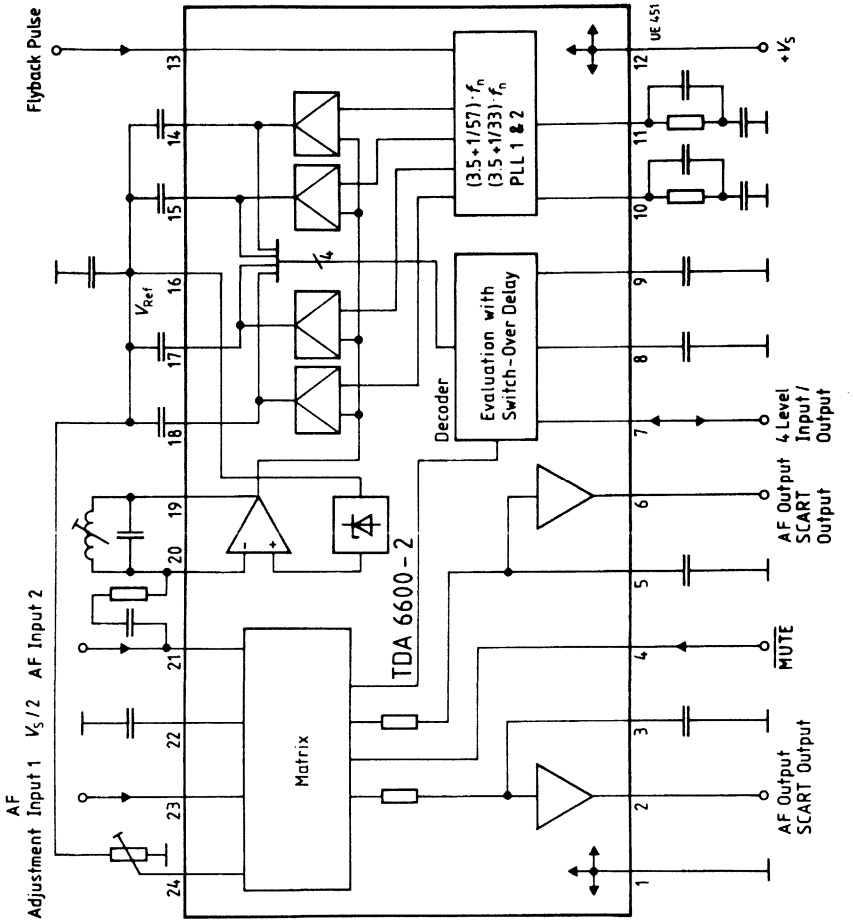
Type	Ordering Code	Package
TDA 6600-2	Q67000-A8210	P-DIP-24

Circuit Description

The circuitry has two functional sections:

1. A pilot frequency decoder including the following circuitries:
   Two phase locked loops for generating the required comparison frequencies (54.96 kHz and 54.8 kHz) from the line frequency. The phase detectors of the control loops operate in a frequency range of 117 Hz and/or 274 Hz.
   Four demodulators to evaluate the 54-kHz pilot signal. The capacitors at the mixer outputs determine the bandwidth (and thus the signal-to-noise ratio) of the pilot tone recognition.
   An evaluation circuitry for decoding "stereo", "dual sound", and "mono" from the mixer output levels. In order to assure interference-free operation in case of high noise level input signals, the individual signals "stereo" and "dual sound" are delayed via an externally adjustable integrator. The subsequent digital evaluation provides the information "mono", "dual sound", or "stereo" to the matrix and the 4 level input/output (to drive the TDA 6200). If this four level input/output is connected to ground externally (e.g. by the TDA 6200), the decoder will recognize this signal as "forced mono".
2. A stereo matrix with deemphasis and SCART output switched by the pilot frequency decoder. The SCART output can be disabled by a MUTE signal (coincidence).

Block Diagram

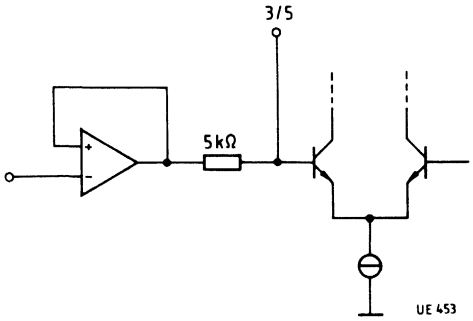


Pin Functions

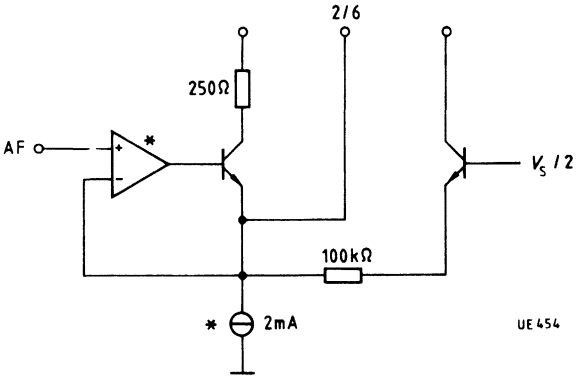
Pin No.	Function
1	Ground
2	AF output/SCART output left channel
3	Deemphasis left channel
4	$\overline{\text{MUTE}}$ input
5	Deemphasis right channel
6	AF output/SCART output right channel
7	4 level input/output
8	Integrator (dual sound)
9	Integrator (stereo)
10	PLL filter (dual sound)
11	PLL filter (stereo)
12	+ V_S (supply voltage)
13	Input line flyback pulse
14	Mixer output (stereo)
15	Mixer output (stereo)
16	Reference voltage
17	Mixer output (dual sound)
18	Mixer output (dual sound)
19	54-kHz filter
20	54-kHz input
21	AF input 2
22	V_S / 2
23	AF input 1
24	Crosstalk adjustment

Pin Descriptions and Functions

De-Emphasis (pin 3, 5)

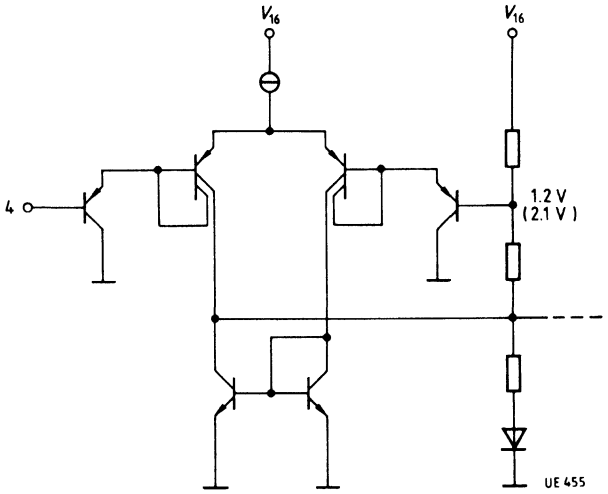


AF Output (pin 2, 6)

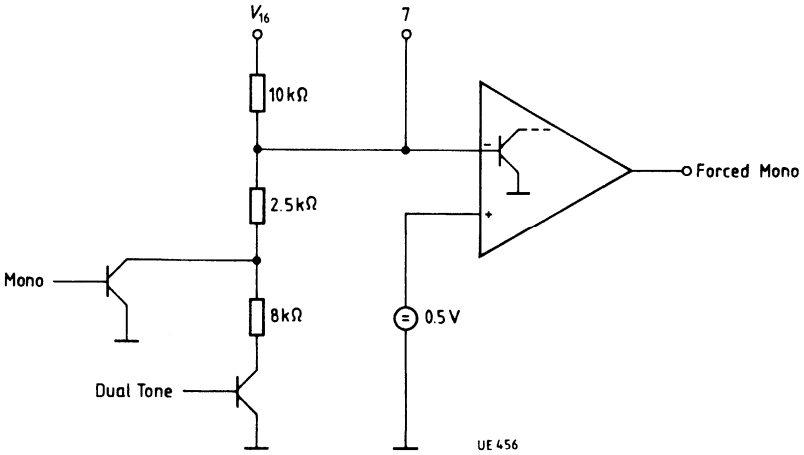


*With $\overline{\text{MUTE}}$ the power supply is switched OFF

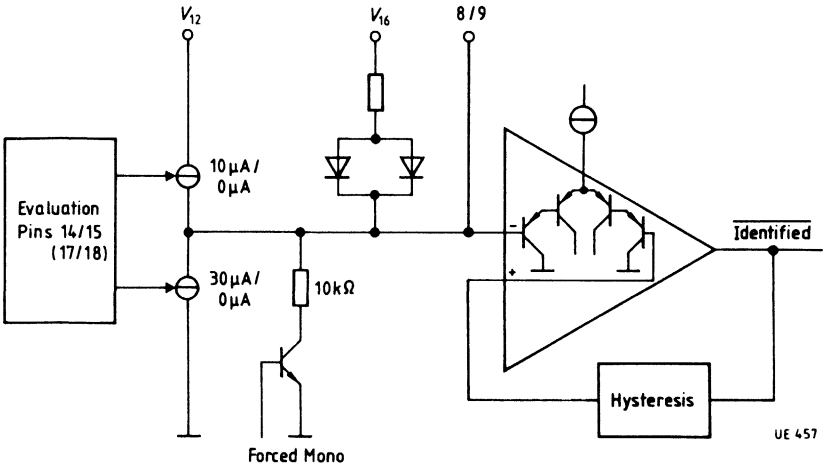
$\overline{\text{MUTE}}$ Schmitt-Trigger (pin 4)



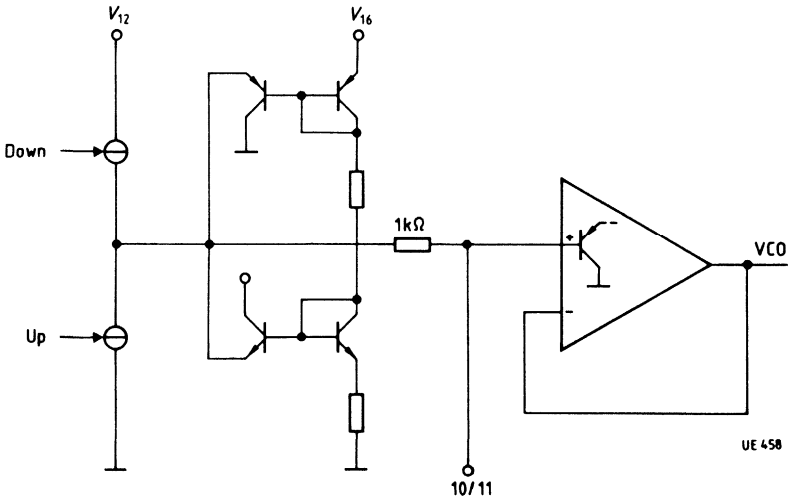
4 Level Input / Output (pin 7)



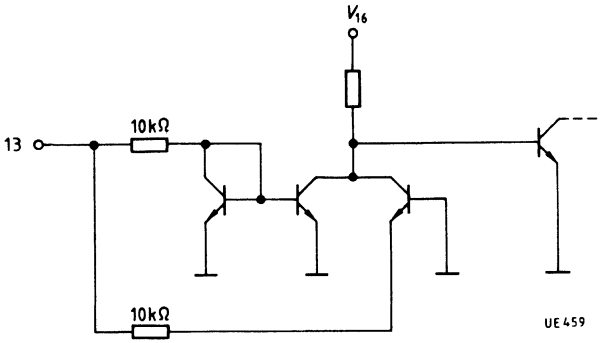
Integrator (pin 8, 9)



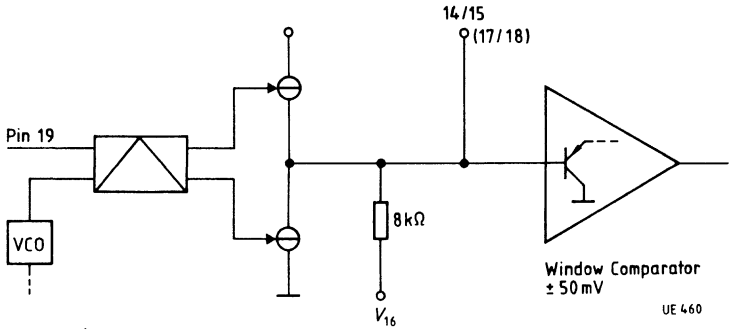
PLL Filter Point (pin 10, 11)



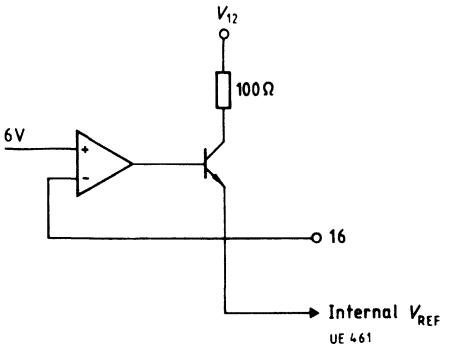
Synchronizing Pulse Input (pin 13)



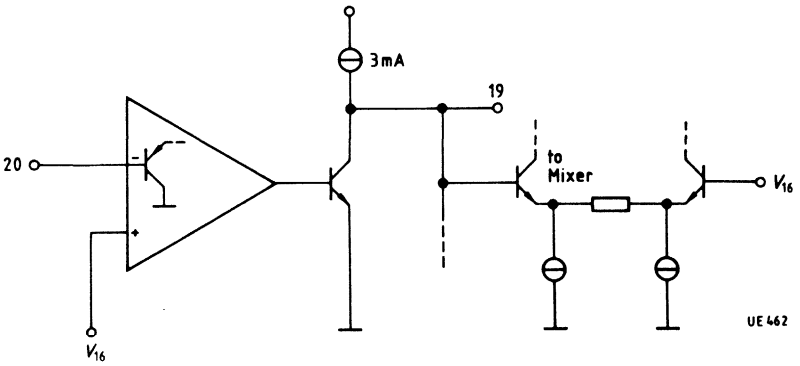
Mixer Outputs (pin 14, 15, 17, 18)



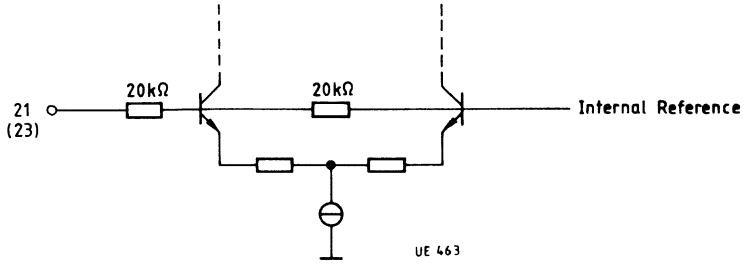
Reference Voltage (pin 16)



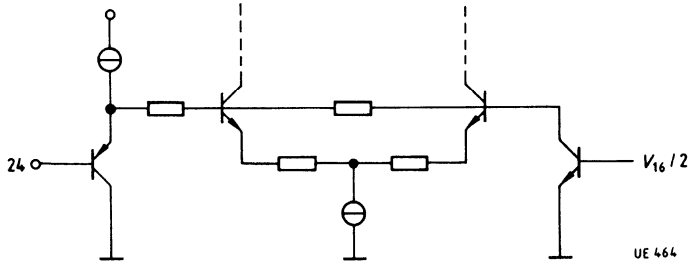
Operational Amplifier (pin 20, 19)



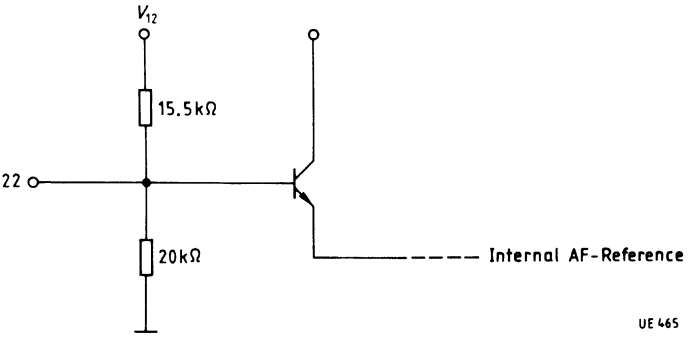
AF Inputs, Channels 1 and 2 (pin 21, 23)



Stereo Compensation (pin 24)



V_S/ **2** (pin 22)



Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	– 0.5	16.5	V
Input Voltage				
Line flyback pulse	V_{13}	$-V_S$	$+V_S$	V
54-kHz input; MUTE	V_{20}; V_4	– 0.5	$+V_S$	V
AF input 1, 2	V_{23}; V_{21}	– 0.5	$+V_S$	V
Crosstalk adjustment	V_{24}	– 0.5	$+V_S$	V
Output Voltage				
Deemphasis L, R	V_3; V_5	– 0.5	$+V_S$	V
V_S / 2; 4 level input/output	V_{22}; V_7	– 0.5	$+V_S$	V
Reference voltage	V_{16}		8	V
Mixer outputs	V_{14}; V_{15} V_{17}; V_{18}	– 0.5	$+V_S - 2$	V
Output Currents				
AF output L, R	I_2; I_6	– 4	4	mA
Integrators	I_8; I_9	– 1	1	mA
PLL filter	I_{10}; I_{11}	– 1	1	mA
Reference voltage	I_{16}	– 4	4	mA
54-kHz filter	I_{19}	– 4	4	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistances (system-air) (system-case)	 $R_{th\,SA}$ $R_{th\,SC}$	 64		K/W

Operating Range

Supply voltage	V_S	10	15.8	V
Temperature range	T_A	0	70	°C

Characteristics
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Current consumption	I_{12}	20	36	50	mA		1
Reference voltage	V_{16}	5.4	6	6.6	V		1
$V_S/2$	V_{22}	6.1	6.8	7.4	V	V_S = 12 V	1
Matrix Section							
Max. AF input voltage	$V_{21};V_{23}$	2			V_{rms}	$THD \leq 2\%$ f_I = 1 kHz	2
Total harmonic distortion factor	THD_2 / THD_6			1	%	V_I = 1 V_{rms} f_I = 1 kHz	2
Gain (V_{OFF} / V_{ON})	$V_2;V_6$		0		dB	$V_{24} = V_{16}/2$ V_I = 300 mV, 1 kHz without deemphasis capacitor	2
Adjustable gain difference channel1/channel2	ΔV		± 6		dB	V_I = 300 mV, 100 Hz V_{24} = 0 V/ V_{16} without deemphasis capacitor	2

Characteristics (cont;d)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Crosstalk Attenuation							
Mono		60	75		dB	decoder recognizes mono V_{I23}= 0V V_{I21}= 2Vrms 1kHz	2
Dual sound		60	75		dB	decoder recog. dual sound $V_{I use}$ = 0Vrms $V_{I interfer}$ = 2Vrms 1 kHz	2
Stereo		30	40		dB	decoder recognizes stereo $V_{I23} = V_{21} / 2$ V_{I21} = 2 Vrms 1 kHz crosstalk adjusted to	3
Input current pin 24 (stereo adjustment)	$-I_{24}$		3	15	µA	$V_{24} = V_{16}$	1
MUTE input level "HIGH" (AF is switched on)	V_4	2.5			V		2
"LOW"	V_4	0		0.7	V		2

Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Input current pin 4	$-I_4$			10	µA	V_4 = 0 V	2
Signal-to-noise voltage unweighted according DIN 45405	V_2, V_6		50	100	µV rms	$V_{24} = V_{16}$ / 2 V_4 = 6 V $V_{I\,21} = V_{I\,23}$ =0V rms (decoder recognizes mono or dual tone)	2
Signal-to-noise voltage unweighted according DIN 45405	V_2, V_6		90	140	µV rms	$V_{24} = V_{16}$ / 2 V_4 = 6 V $V_{I\,21} = V_{I\,23}$=0V rms (decoder recognizes stereo)	2
Signal-to-noise ratio measured with mono or dual tone	SNR	69	75		dB	$V_{I\,rms}$= 300 mV; V_4 = 6 V: $V_{24} = V_{16}$ / 2	2
DC jump of output voltage during switch-over of decoder	V_2, V_6			300	mV		2
Design-Related Data							
Input impedance	$R_{I\,21;23}$	20	40		kΩ		
Output impedance	$R_{Q\,2;6}$			200	Ω	V_4 = 6 V	
Output impedance	$R_{Q\,2;6}$		100		kΩ	V_4 = 0 V	
Deemphasis resistance	$R_{3;5}$	3.5	5	6.5	kΩ		

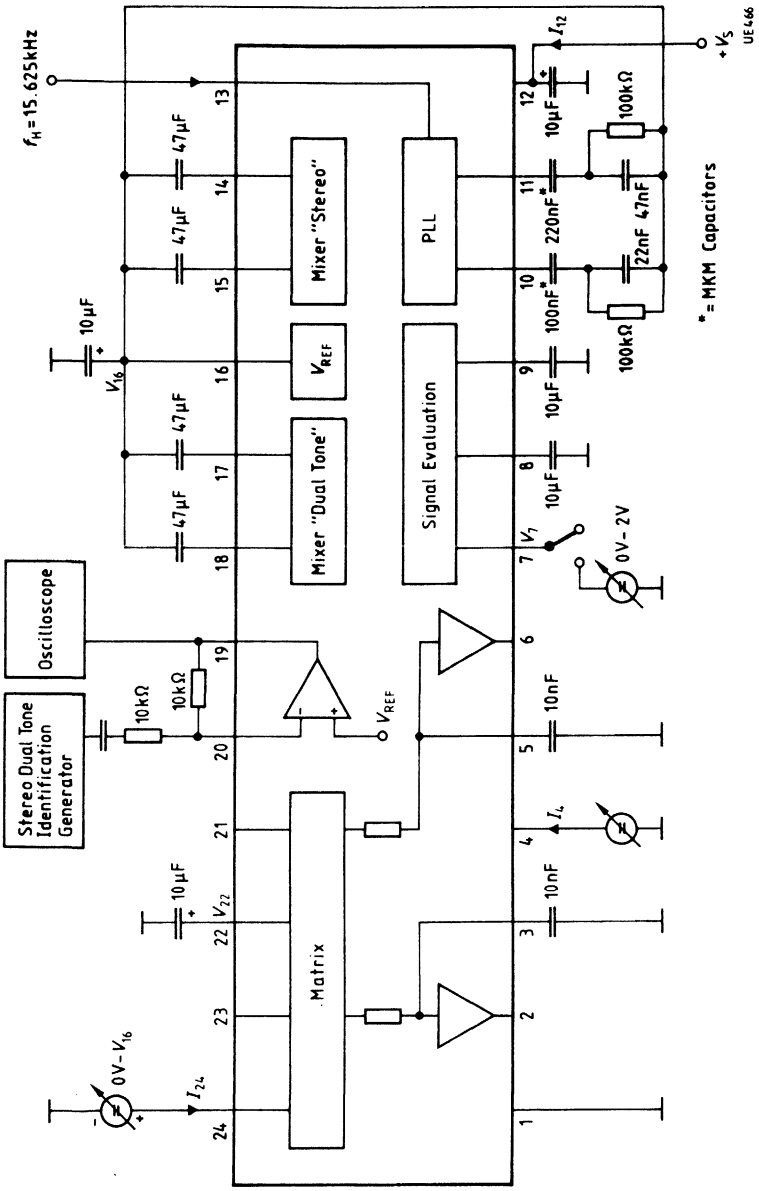
Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Decoder Section							
Identification sensitivity	V_{19}	71			mV rms	Pin 19: Pilot frequency is modulated with identification frequency at 50% modulation depth. The mean value of the pilot frequency is indicated at which the decoder will safely recognize "stereo" and/or "dual sound".	1
Identification sensitivity (lower limit)	V_{19}	0		11	mV rms	Pin 19: Pilot frequency is modulated with identification frequency at 50% modulation depth. The mean value of the pilot frequency will safely remain in the "mono" mode	1

Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Max. permissible mixer input voltage	$V_{I\,19max}$			600	mV_{pp}		1
Signal delay through integrators	$t_{8/9}$		700		ms		4
4 Level Input / Output							
Output current	I_7			1	mA	V_7 = 0 V	1
Output voltage at "Stereo"	V_7	5.3	6		V		1
Output voltage at "Dual Sound"	V_7	2.6	3.1	3.6	V		1
Output voltage at "Mono"	V_7	1.1	1.3	1.6	V		1
Forced mono identification	V_7	0		0.6	V	voltage externally injected	1
Pulse width of forced mono	t_7	500			µs		1
Threshold gating pulse input	V_{13}	± 1.5		± 3.5	V		1
Design Related Data							
Mixer output resistance	$R_{14;15}$		8		kΩ		
4 level output impedance	$R_{17;18}$ R		8	 15	kΩ		

Test Circuit 1



Test Circuit 2

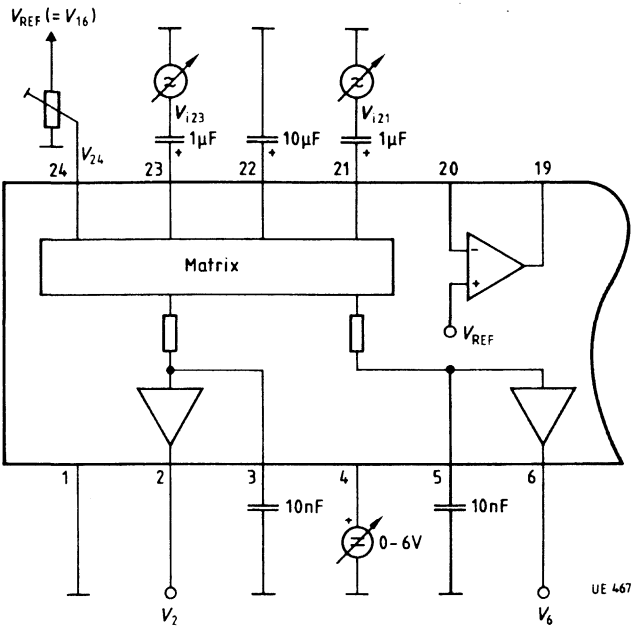


Diagram illustrating circuit layout between pin 7 and 20 identical to test circuit 1

Test Circuit 3

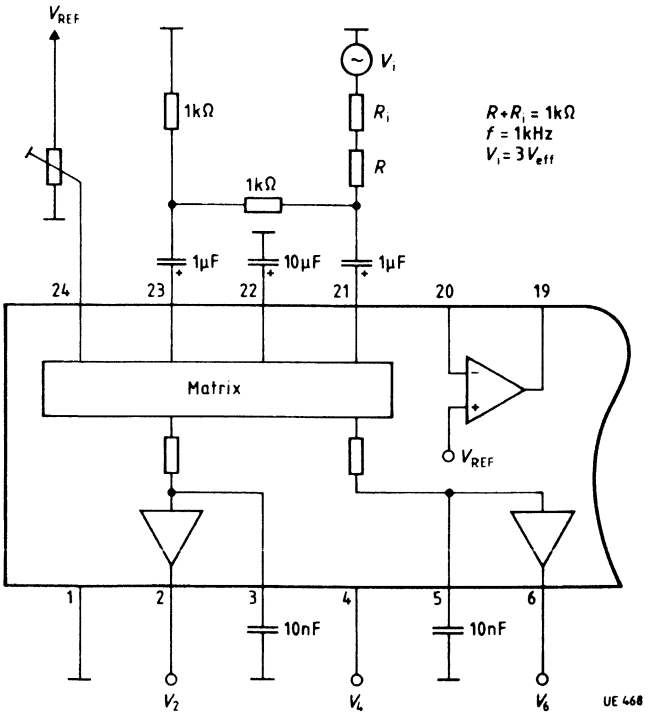
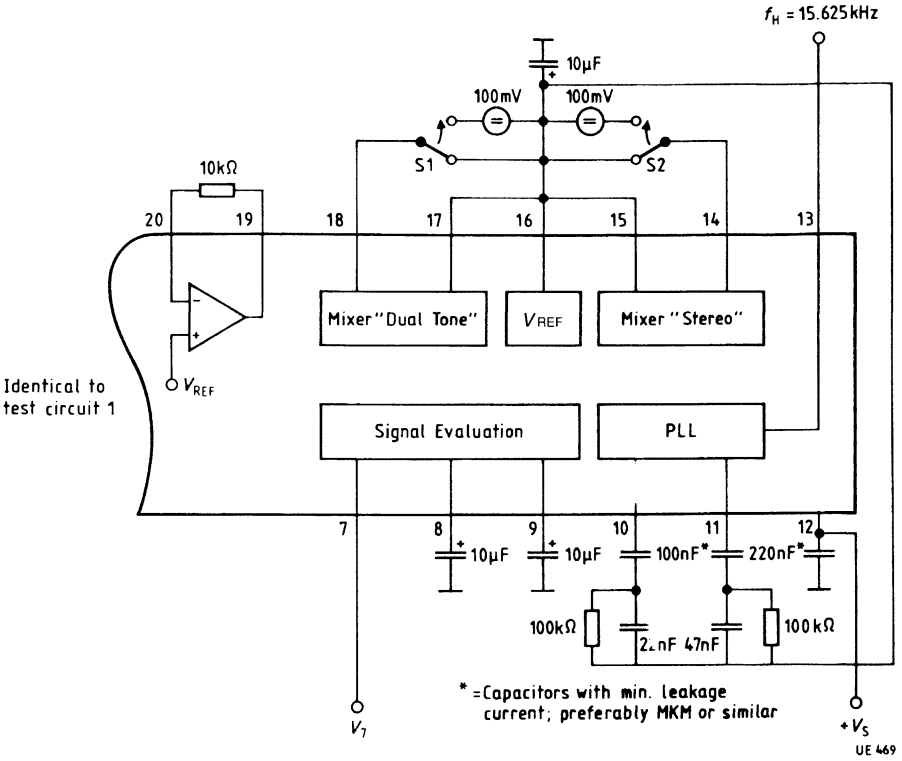
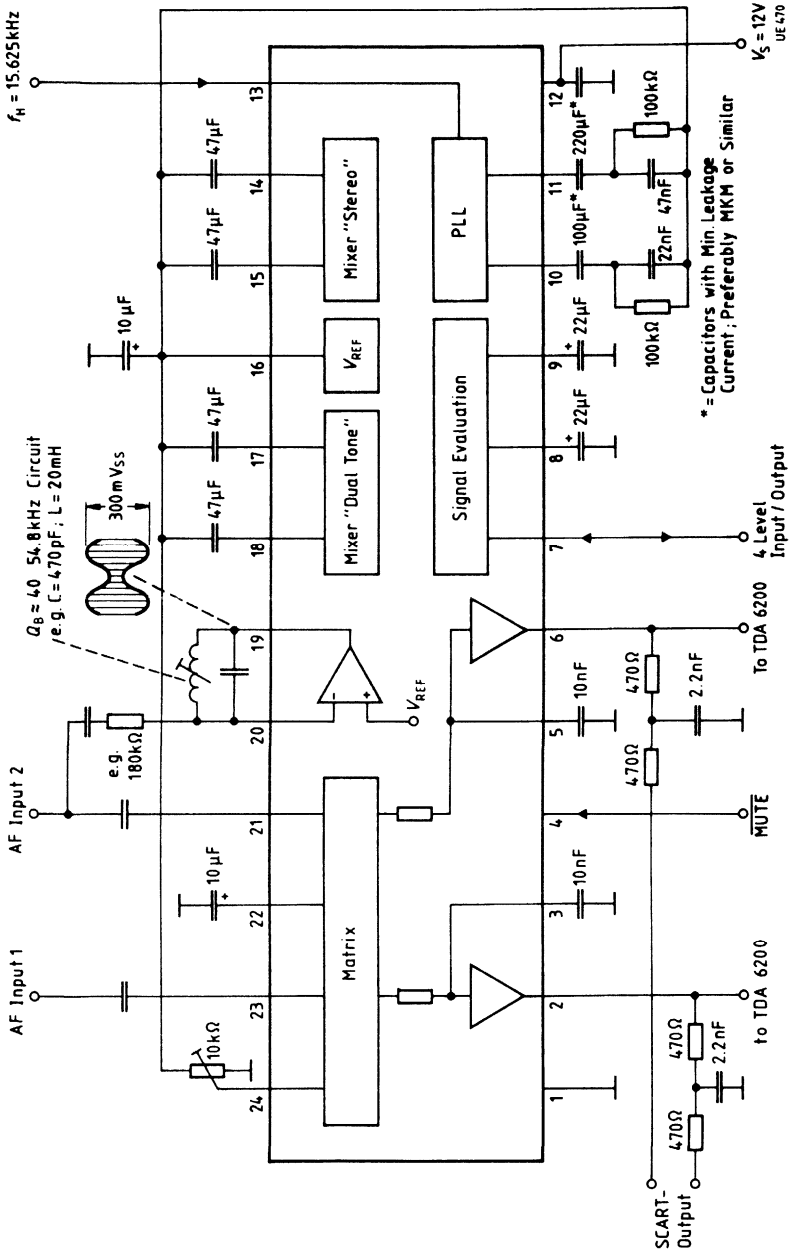


Diagram illustrating circuit layout between pin 7 and 20 identical to test circuit 1

Test Circuit 4



Application Circuit



SIEMENS

TV Stereo Processor — TDA 6611

Preliminary Data — **Bipolar IC**

Features

The TDA 6611 represents a complete TV stereo system controlled by the I^2C bus.

- All functions inclusive matrix adjustment are I^2C bus controlled
- SCART-Interface
- Independent headphones
- Higher signal noise ratio
- Extremely low distorsion
- High security rata against mis-switching of the decoder performed by the digital interference suppression and the very narrow bandwidth

Type	Ordering Code	Package
TDA 6611	Q67000-A8260	P-DIP-28

The IC is divided into three functional blocks

1) **Stereo sound processing with high quality (exceeds DIN 45500; suitable for NICAM and CD)**
   a) matrix for G standard with crosstalk compensation controlled via the I^2C Bus
   b) additional single-channel AF input (for e.g. AF signal accord. L standard)
   c) stereo SCART interface in accordance with FTZ official brochure
   d) stereo loudspeaker signal section with Ch1/Ch2 switch, high/low regulation, quasi-stereo/stereo basic processing and separate loudspeaker regulation for left and right
   e) signal section with Ch1/Ch2 switch and loudspeaker regulation for stereo headphones

2) **TV sound identification signal decoder consisting of:**
   a) active pilot signal filter
   b) phase-independent rectifier with very narrow bandwidth for evaluation of the identification signal
   c) digital integrator to reduce interference
   d) multiplexer for cyclical switch over between "stereo" or "dual" evaluation
   e) PLL for the generation of the reference signal. External synchronization with either the flyback pulse or external reference clock signals of 62.5 kHz or 4 MHz can also be generated using the internal crystal generator with an external crystal.

3) **Control section for:**
   a) I^2C bus interface with listener/talker function
   b) control of the complete AF sound processing
   c) control of the identification signal decoder
   d) reading of the identification signal decoder
   e) test modes

Circuit Description

Signal Section

The audio signal processing in the matrix and the switch-over for multichannel TV sound signals according to the two-carrier system used in Germany takes place in the matrix and switching sections. Crosstalk compensation is carried out in the Sound 1 input. The compensation range has an adjustment range of ± 3 dB with a minimum step of 0.2 dB. In addition to the two inputs for the demodulated sound carrier, a two-channel scart input and an additional mono input (e.g. for demodulated L-standard sound) are provided. The two AF inputs can be bypassed internally in such a way that decoded stereo sound signals of other audio systems (NICAM) can be processed. The switching section is terminated with the SCART output and an independently switchable Ch1/Ch2 switch for the loudspeaker and headphone outputs.

In the loudspeaker signal path a switchable quasi-stereo section follows the Ch1/Ch2 switch. This section gives a special audio effect with mono signals due to a 180° phase shift at medium frequencies (about 1 kHz) in one channel. The following base control exhibits a step of 3 dB with an adjustment range of + 15/– 12 dB. The cutoff frequency is set for each channel with an external capacitor. The circuit for stereo basewidth expansion, which, with switchable stereo signals, provides a more special audio effect due to 50 % of frequency dependent crosstalk in opposing phases, operates with the same cutoff frequency as the base control, but the function is largely independent. The treble control, whose cutoff frequency is also controlled by a capacitor in each channel, also has a step of 3 dB with an adjustment range of ± 12 dB. The loudspeaker signal path is terminated with a loudspeaker control, independently adjustable for left and right. With 57 steps of 1.25 dB the adjustment range is 70 dB, where step 57 activates the "MUTE" function. Functions such as "balance" or "loudness" are realized by software adjustment of the appropriate tone and volume controls.

The signal path for the headphones contains a volume control after the Ch1/Ch2 switch with a common adjustment for left and right. Thirty-two steps of 2 dB give an adjustment range of 62 dB (31 × 2 dB = 62 dB, the 32nd step is MUTE).

Identification Signal Decoder

The input of the identification signal decoder consists of an op-amp for the pilot signal with its sidebands. An external LC circuit is used. The signal is then passed to a phase-independent active bandpass filter with a very narrow bandwidth (adjustable externally). This filter detects whether the lower sideband of the pilot carrier, which is modulated with the identification signal, is present. The center frequency of the filter is switched between "dual" and" stereo" by a multiplexer. The multiplexing frequency is adjustable by software. If a sideband is detected, the multiplexer stops. The first "detected" criterion is rendered free from interference by a digital integrator with a following comparator and can be read out via I^2C bus (talk mode) as the "stereo" or "dual" mode. The control of the corresponding signal can be either directly internally or through the μC. All the necessary clock signals are derived from a fast settling PLL which is synchronized by a reference frequency. This reference frequency must be sufficiently close to the horizontal frequency, but a **rigid phase coupling is not required**. Therefore, alternatively the use of a crystal-controlled 62.5-kHz frequency commonly found in PLL tuning systems is possible.

Control Section

All functions are controlled via I²C bus interface with listen/talk functions. The current applicable data are stored in a block of latches.

The telegram structure is formed in the following manner:

start condition – chip address – any number of bytes – stop condition

The following conditions apply to the data bytes:
Before the actual data byte (with the adjustment information), a subaddress by the I²C bus byte must **always** be transmitted. This byte is however interpreted by the I²C bus as a data byte interface.

Example: The headphone volume is to be increased in a number of steps.

Right	**Wrong**
start condition	start condition
chip address 84 (hex)	chip address 84 (hex)
subaddr. vol. HP 03 (hex)	subaddr. vol HP 03 (hex)
vol. step 8 08 (hex)	vol. step 8 08 (hex)
subaddr. vol. HP 03 (hex)	vol. step 9.09 (hex)
vol. step 9 09 (hex)	vol. step 10 0A (hex)
subaddr. HP 03 (hex)	stop condition
vol. step 10 0A (hex)	
stop condition	

Within a telegram (i.e. without a new start condition) any different subaddresses can be accessed. The changeover between "listen" and "talk" must however always occur via the sequence stop condition – start condition – chip address. Before each readout always a start condition and chip address (talk) must be transmitted. The data to be read out are loaded into the I²C bus interface and can be transferred to the µC.

Chip Address

	MSB	.	.	.	.	.	.	LSB
	1	0	0	0	0	1	0	R/W

R/W = 0 → read (listen)
R/W = 1 → write (talk)

Subaddress Bytes

	MSB	.	.	.	.	.	.	LSB
Vol. of left speaker	X	X	X	X	X	0	0	1
Vol. of right speaker	X	X	X	X	X	0	1	0
Vol. of headphones	X	X	X	X	X	0	1	1
Treble/bases	X	X	X	X	X	1	0	1
Switch byte I	X	X	X	X	X	1	1	1
Switch byte II	X	X	X	X	X	0	0	0
Crosstalk compensation	X	X	X	X	X	1	1	0

Setting Bytes

a) Volume of left/right loudspeaker

	MSB	.	.	.	.	.	.	LSB
Maximum volume	X	X	1	1	1	1	1	1
Max - 1	X	X	1	1	1	1	1	0
Max - 15	X	X	1	1	0	0	0	0
Max - 55	X	X	0	0	1	0	0	0
MUTE	X	X	0	0	0	1	1	1
MUTE	X	X	0	0	0	0	0	0
MUTE	X	X	0	0	0	X	X	X
Power on	0	0	0	0	0	0	0	1

b) Volume of headphones

	MSB	.	.	.	.	.	.	LSB
Max. volume	T2	T1	T0	1	1	1	1	1
Max - 1	T2	T1	T0	1	1	1	1	0
Max - 15	T2	T1	T0	1	0	0	0	0
Max - 31	T2	T1	T0	0	0	0	0	1
MUTE	T2	T1	T0	0	0	0	0	0
Power on	0	0	0	0	0	0	0	1

T0-T2 are test bits; these must be set to 0 for normal operation

c) Crosstalk compensation matrix (sound 1)

	MSB	.	.	.	.	.	.	LSB
Max. amplification	X	X	X	1	1	1	1	1
Max - 1	X	X	X	1	1	1	1	0
Gain 0 dB	X	X	X	1	0	0	0	0
Min. gain	X	X	X	0	0	0	0	1
Min. gain	X	X	X	0	0	0	0	X
Power on	0	0	0	0	0	0	0	1

d) Treble/bass

	MSB	.	.	.	.	.	.	LSB
Linear	1	0	0	0	1	0	0	0
Max. treble, lin. bass	1	1	0	0	1	0	0	0
Max. treble, lin. bass	1	1	X	X	1	0	0	0
Min. treble, lin. bass	0	1	0	0	1	0	0	0
Min. treble, lin. bass	0	0	X	X	1	0	0	0
Lin. treble, max. bass	1	0	0	0	1	1	0	1
Lin. treble, max. bass	1	0	0	0	1	1	X	1
Lin. treble, max. bass	1	0	0	0	1	1	1	X
Lin. treble, min. bass	1	0	0	0	0	1	0	0
Lin. treble, min. bass	1	0	0	0	0	0	X	X
Max. treble, max. bass	1	1	X	X	1	1	X	1
Min. treble, min. bass	0	0	X	X	0	0	X	X
Power on	0	0	0	0	0	0	0	1
	MSB treble			LSB treble	MSB bass			LSB bass

e) Switch byte I

MSB LSB

MUTE I MUTE II < $Ch1/Ch2_{vol}$ $Ch1/Ch2_{HP}$ Mono SCART SCART-D AM

MUTE I = 0 All AF outputs are muted (speakers, headphones, SCART); power on
MUTE I = 1 All AF outputs on
MUTE II = 0 Loudspeaker outputs muted; power on
MUTE II = 1 Loudspeaker outputs on
MUTE I and MUTE II are OR gated with respect to the loudspeaker outputs

MUTE I	MUTE II	loudspeaker outputs	headphones, SCART o/p
0	0	muted	muted
0	1	muted	muted
1	0	muted	on
1	1	on	on

$Ch1/Ch2_{vol}$ = 0 Sound 1 on the loudspeaker outputs; power on
$Ch1/Ch2_{vol}$ = 1 Sound 2 on the loudspeaker outputs
$Ch1/Ch2_{HP}$ = 0 Sound 1 on the headphone outputs; power on
$Ch1/Ch2_{HP}$ = 1 Sound 2 on the headphone outputs

$Ch1/Ch2_{vol}$ and $Ch1/Ch2_{HP}$ are only effective if the matrix is set to the position "dual sound".

Mono = 0 identification signal decoder is set to the position mono and held; power on
Mono = 1 normal operation of ID signal decoder
SCART = 0 normal TV operation; power on
SCART = 1 SCART playback; connection of SCART inputs – AF outputs. SCART = 1 has priority over AM = 1 (loudspeaker and headphones)
SCART-D = 0 SCART playback stereo (mono); power on
SCART-D = 1 Enable for the Ch1/Ch2 switch during SCART playback (only effective when SCART = 1)
AM = 0 normal operation (G standard)
AM = 1 AM AF input is activated; power on
AM = 1 has priority over Bypass = 1

f) Switch byte II

MSB							LSB
MPX0	MPX1	quasi-st	Be	H pul	Matrix 0	Matrix 1	Bypass

MPX0	MPX1	MPX period		recommended $C_{25,26}$
0	0	2 s	power on	1 µF
0	1	4 s		2.2 µF
1	0	8 s		4.7 µF
1	1	1 s		470 nF

MPX period = 2 s signifies: ID signal decoder searches 1 second dual and 1 second stereo

Quasi-st	= 0	Quasi-stereo off; power on
Quasi-st	= 1	Quasi-stereo on
Be	= 0	stereo basewidth expansion off; power on
Bb	= 1	stereo basewidth expansion on;
H pul	= 0	ID signal decoder synchronization with f_H = 15.625 kHz; power on
H pul	= 1	ID synchronization with 4 × f_H

Matrix 0	Matrix 1	matrix status	
0	0	mono	power on
0	1	stereo	
1	0	dual	
1	1	automatic according to ID signal decoder	

Bypass	= 0	normal operation (G standard)
Bypass	= 1	matrix is bridged so that left/right signals can be fed in; power on (AM = 1 has priority over Bypass = 1)

Priority list of setting bits

1. MUTE I
2. MUTE II (only with regard to the loudspeaker output)
3. SCART
4. AM
5. Bypass
6. Matrix 0, 1

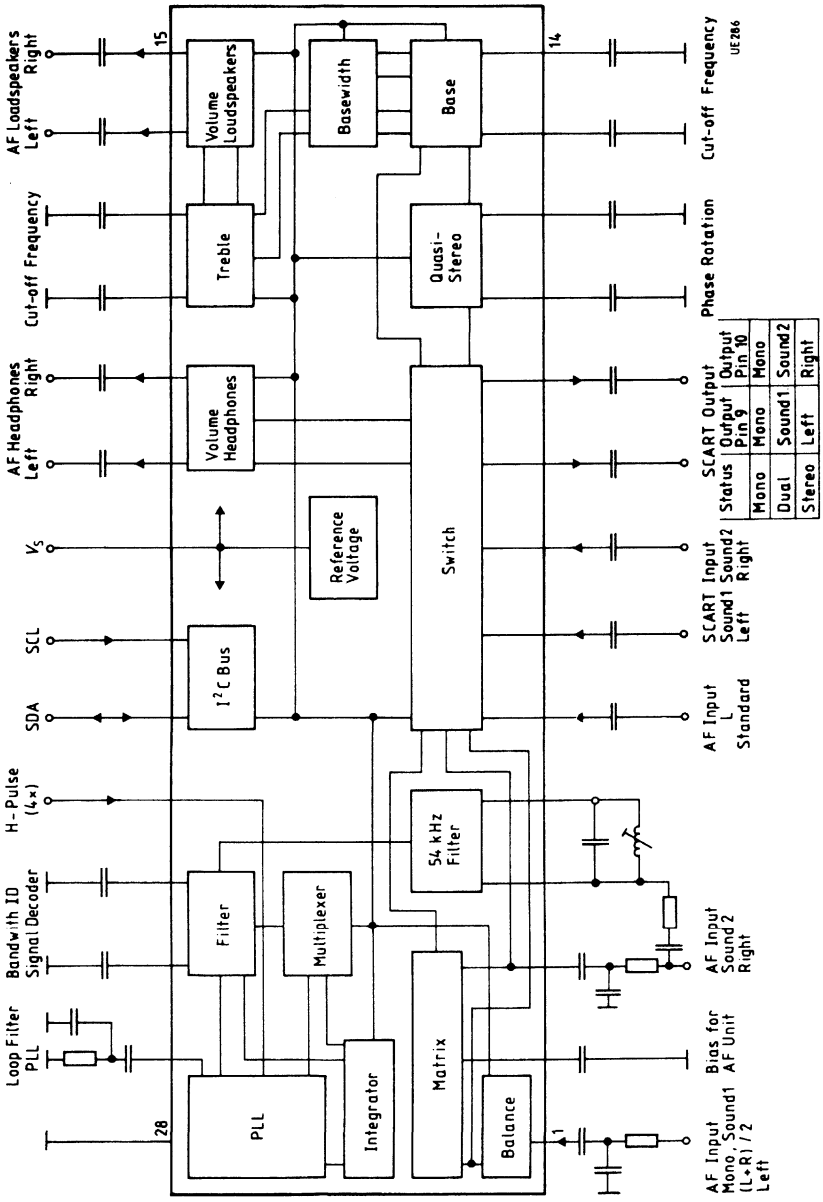
g) Talk mode

MSB	.	.	.	.	.	.	LSB
St	D	T5	T4	T3	X	X	X

0	0	decoder detects mono
1	0	decoder detects stereo
0	1	decoder detects dual
1	1	internally inhibited

T3 – T5 are test bits

Block Diagram



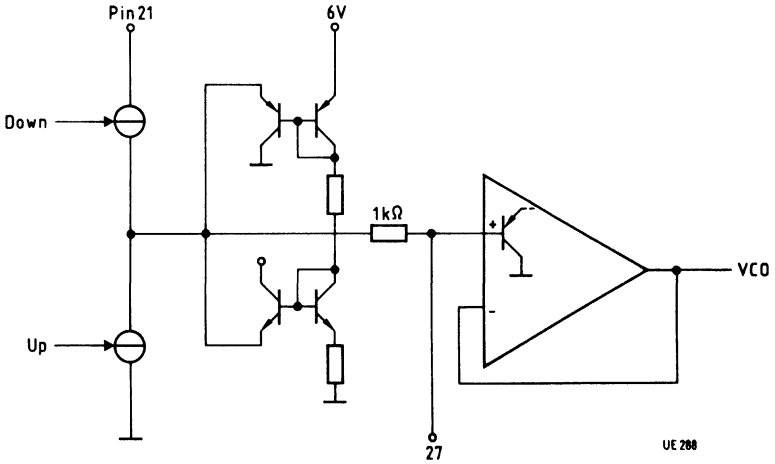
Status	SCART Output Pin 9	SCART Output Pin 10
Mono	Mono	Mono
Dual	Sound1	Sound2
Stereo	Left	Right

Pin Functions

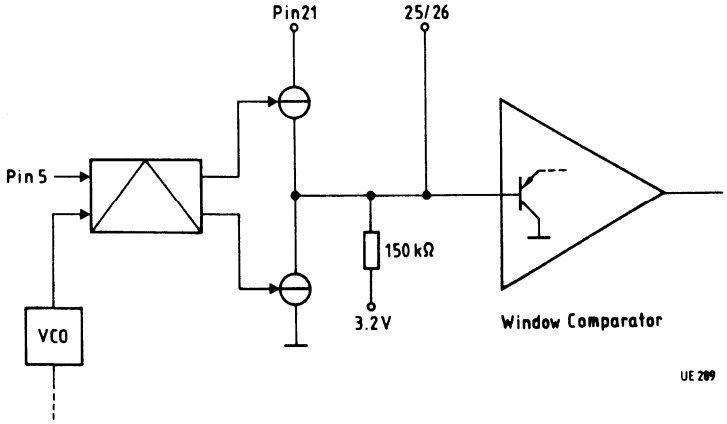
Pin No.	Function
1	AF input mono, left, sound 1 (may be balanced)
2	Bias for AF operating point
3	AF input right, sound 2
4	54-kHz input
5	54-kHz filter
6	AF input (L standard)
7	AF input SCART left (sound 1)
8	AF input SCART right (sound 2)
9	AF output SCART (mono, sound 1, left)
10	AF output SCART (mono, sound 2, right)
11	Phase-shifter quasi-stereo
12	Phase-shifter quasi-stereo
13	Cutoff frequency base (basewidth) left
14	Cutoff frequency base (basewidth) right
15	AF output, loudspeaker left
16	AF output, loudspeaker right
17	Cutoff frequency treble left
18	Cutoff frequency treble right
19	AF output, headphones left
20	AF output, headphones right
21	Supply voltage
22	I^2C bus SCL
23	I^2C bus SDA
24	Input H pulse (4 × H pulse)
25	Filter ID signal decoder
26	Filter ID signal decoder
27	PLL filter ID signal decoder
28	Ground

Pin Functions

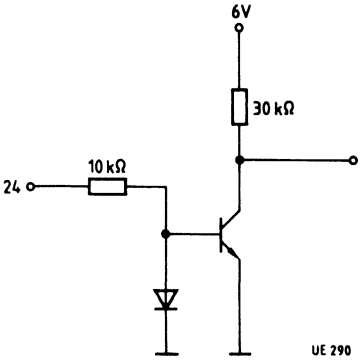
PLL Filter ID Signal Decoder (Pin 27)



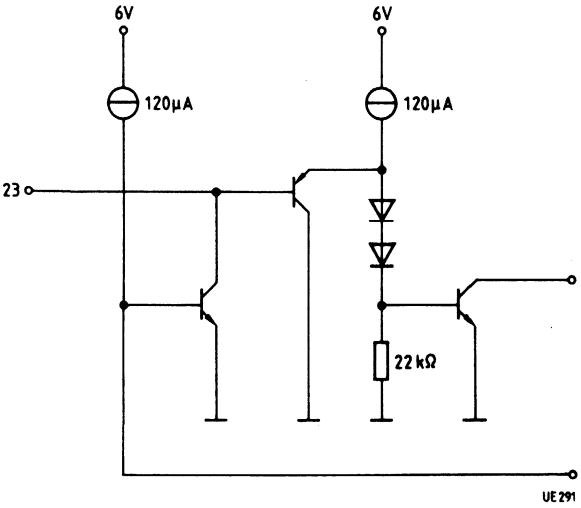
Filter ID Signal Decoder (Pin 25/26)



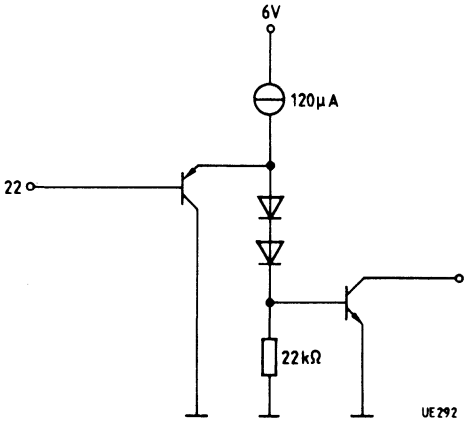
Input H Pulse (Pin 24)



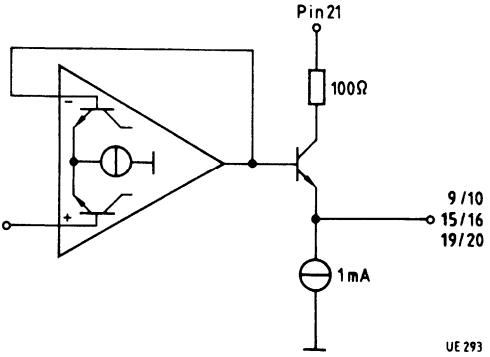
I²C Bus SDA (Pin 23)



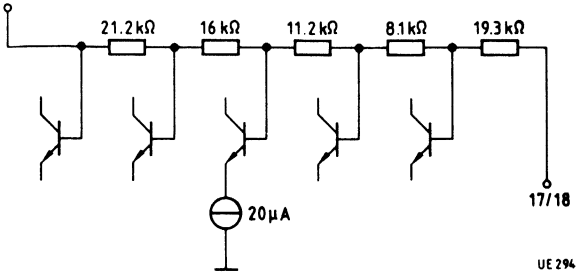
I²C Bus SCL (Pin 22)



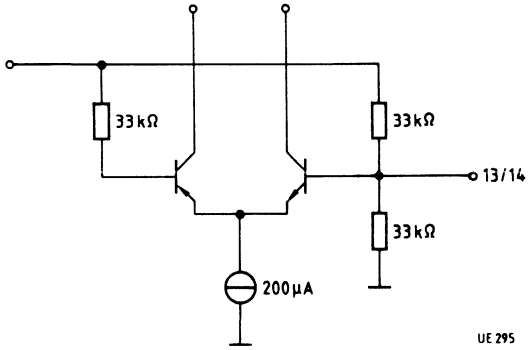
AF Outputs Headphones (Pin 19/20)
Loudspeaker (Pin 15/16)
SCART (Pin 9/10)



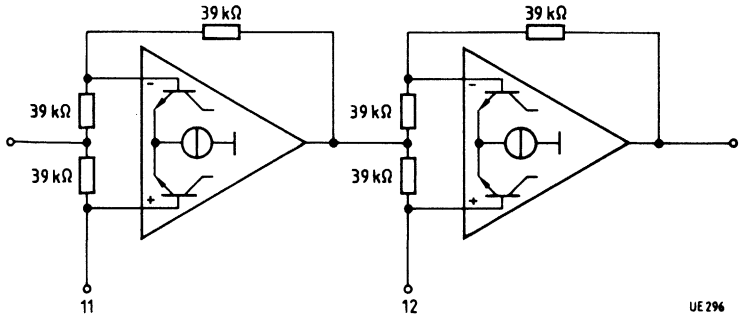
Cutoff Frequency Treble (Pin 17/18)



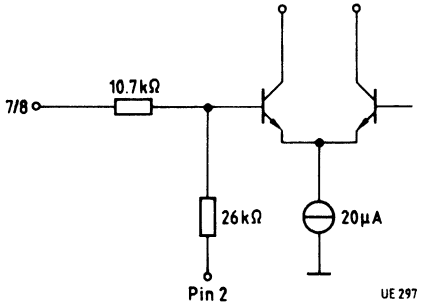
Cutoff Frequency Bass (Pin 13/14)



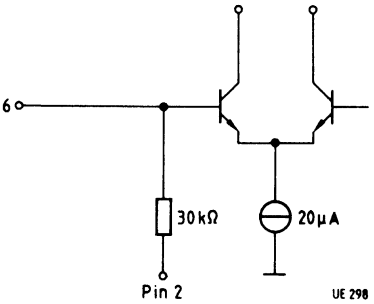
Phase Advancer Quasi Stereo (Pin 11/12)



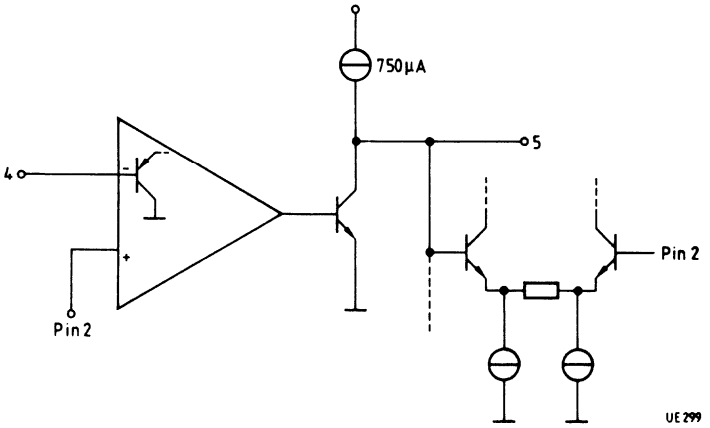
AF Inputs SCART (Pin 7/8)



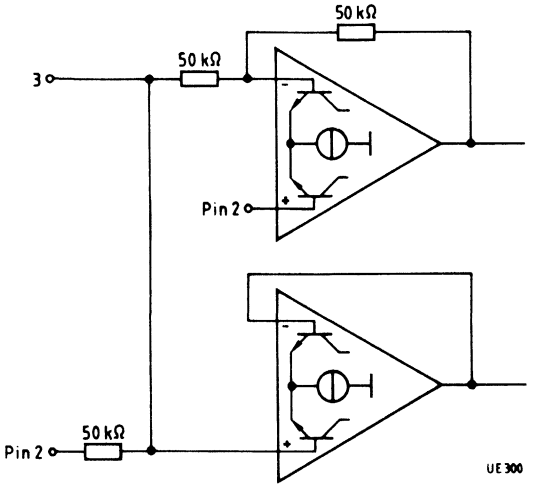
AF Input AM (Pin 6)



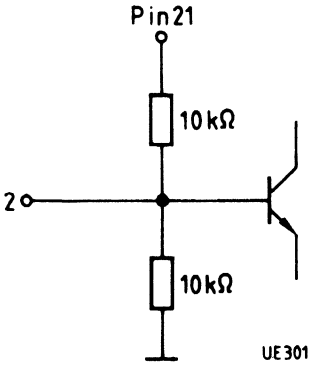
54 – kHz Filter (Pin 4/5)



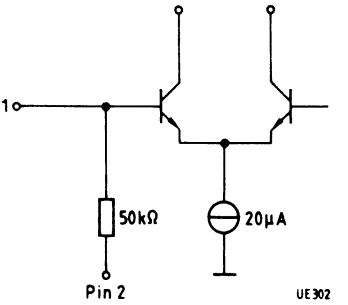
AF Input (Pin 3)



Input for AF Unit Bias Blocking Capacitor (Pin 2)



AF Input (Pin 1)



Absolute Maximum Ratings

T_A = 25 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{21}	0	14	V
Max. DC voltage	V_1	0	V_{21}	V
Max. DC voltage	V_2	0	V_{21}	V
Max. DC voltage	V_3	0	V_{21}	V
Max. DC voltage	V_4	0	V_{21}	V
Max. DC voltage	V_6	0	V_{21}	V
Max. DC voltage	V_7	0	V_{21}	V
Max. DC voltage	V_8	0	V_{21}	V
Max. DC voltage	V_{11}	0	V_{21}	V
Max. DC voltage	V_{12}	0	V_{21}	V
Max. DC voltage	V_{12}	0	V_{21}	V
Max. DC voltage	V_{14}	0	V_{21}	V
Max. DC voltage	V_{17}	0	V_{21}	V
Max. DC voltage	V_{18}	0	V_{21}	V
Max. DC voltage	V_{22}	0	V_{21}	V
Max. DC voltage	V_{23}	0	V_{21}	V
Max. DC voltage	V_{24}	0	V_{21}	V
Max. DC voltage	V_{25}	0	V_{21}	V
Max. DC voltage	V_{26}	0	V_{21}	V
Max. DC current	I_5	0	2	mA
Max. DC current	I_9	0	2	mA
Max. DC current	I_{10}	0	2	mA
Max. DC current	I_{15}	0	2	mA
Max. DC current	I_{16}	0	2	mA
Max. DC current	I_{19}	0	2	mA
Max. DC current	I_{20}	0	2	mA
Max. DC current	I_{27}	0	1	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-ambient)	$T_{th\,SA}$		53	K/W

Operating Range

Supply voltage	V_6	10	13.2	V
Ambient temperature	T_A	0	70	°C
Input frequency range	f	0.01	20	kHz

Characteristics

V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

I²C bus present: start-84-01,3F-0 2,3F-0 3,1F-0 5,88-0 6,10-07,C8-00,01-stop
Chip address - Vol_{LSl}63-Vol_{LSr}63.-.Vol_{HP}31 - tone lin - adj 0dB - MUTE I,MUTE II, mono-bypass
The basic setting for each point in the specification is always preset; only settings which deviate from this are given in the test conditions. Details in *italics* only provide explanation of the hexadecimal code and with switch bits on the set bits and features are stated.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_{21}		50		mA	
Signal Section						
Max. gain	$V_{16\text{-}1}$	– 2	0	2	dB	
Max. gain	$V_{15\text{-}3}$	– 2	0	2	dB	
Max. gain	$V_{20\text{-}1}$	– 2	0	2	dB	
Max. gain	$V_{19\text{-}3}$	– 2	0	2	dB	
Max. gain	$V_{16\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 01 Matrix: stereo
Max. gain	$V_{15\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 01 Matrix: stereo
Max. gain	$V_{20\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 0 Matrix: stereo
Max. gain	$V_{19\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 0 Matrix: stereo
Max. gain	$V_{16\text{-}1}$	4	6	8	dB	00,02; V_3 = 0 Matrix: stereo
Max. gain	$V_{20\text{-}1}$	4	6	8	dB	00,02; V_3 = 0 Matrix: stereo
Max. gain	$V_{16\text{-}7}$	– 5	– 3	– 1	dB	07,CC, SCART
Max. gain	$V_{15\text{-}8}$	– 5	– 3	– 1	dB	07,CC, SCART
Max. gain	$V_{20\text{-}7}$	– 5	– 3	– 1	dB	07,CC, SCART
Max. gain	$V_{19\text{-}8}$	– 5	– 3	– 1	dB	07,CC, SCART
Max. gain	$V_{16\text{-}6}$	– 2	0	2	dB	07,C9, AM
Max. gain	$V_{15\text{-}6}$	– 2	0	2	dB	07,C9, AM
Max. gain	$V_{20\text{-}6}$	– 2	0	2	dB	07,C9, AM
Max. gain	$V_{19\text{-}6}$	– 2	0	2	dB	07,C9, AM
Gain	$V_{9\text{-}1}$	– 2	0	2	dB	
Gain	$V_{10\text{-}3}$	– 2	0	2	dB	
Gain	$V_{9\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 0 Matrix: stereo
Gain	$V_{10\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 0 Matrix:stereo
Gain	$V_{9\text{-}1}$	4	6	8	dB	00,02; V_3 = 0 Matrix: stereo

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Gain	$V_{10\text{-}6}$	– 2	0	2	dB	07,C9, *AM*
Gain	$V_{9\text{-}6}$	– 2	0	2	dB	07,C9, *AM*
Min. gain	$V_{16\text{-}1}$		– 70		dB	01,08-02,08 VolLSI8-VolLSr8
Min. gain	$V_{15\text{-}3}$		– 70		dB	01,08-02,08 VolLSI8-VolLSr8 01,08-02,08
Min. gain	$V_{20\text{-}1}$		– 62		dB	03,01Vol HP1
Min. gain	$V_{19\text{-}3}$		– 62		dB	03,01Vol HP1
Min. gain	$V_{16\text{-}7}$		– 73		dB	07,CC-01,08-02,08 SCART-VolLSI8-VolLSr8
Min. gain	$V_{15\text{-}8}$		– 73		dB	07,CC-01,08-02,08 SCART-VolLSI8-VolLSr8
Min. gain	$V_{20\text{-}7}$		– 65		dB	07,CC-03,01 SCART-VolKH1
Min. gain	$V_{19\text{-}8}$		– 65		dB	07,CC-03,01 SCART-VolKH1
Min. gain	$V_{16\text{-}6}$		– 70		dB	07,C9-01,08-02,08 AM-VolLSI8-VolLSr8
Min. gain	$V_{15\text{-}6}$		– 70		dB	07,C9-01,08-02,08 AM-VolLSI8-VolLSr8
Min. gain	$V_{20\text{-}6}$		– 62		dB	07,C9-03,01 SCART-VolKH1
Min. gain	$V_{19\text{-}6}$		– 62		dB	07,C9-03,01 SCART-VolKH1
Flutter and wow	$\Delta V_{15\text{-}16}$			± 2	dB	01,3F to 01,24 02,3F to 02,24 Vol_{LSI}63-36-Vol_{LSr}63-36
Flutter and wow	$\Delta V_{19\text{-}20}$			± 2	dB	03,1F to 03,13 Vol_{KH}31-19
Step width Vol_{15}	ΔV_{15}	0	1.25	2.5	dB	01,X-01,(X±1) Vol_{LSi}X-Vol_{LSi}(X±1)
Step width Vol_{16}	ΔV_{16}	0	1.25	2.5	dB	02,X-02,(X±1) Vol_{LSr}X-Vol_{LSr}(X±1)
Step width Vol_{19}	ΔV_{19}	0	2	4	dB	03,X-03,(X±1) Vol_{KH}X-Vol_{KH}(X±1)
Step width Vol_{20}	ΔV_{20}	0	2	4	dB	03,X-03,(X±1) Vol_{KH}X-Vol_{KH}(X±1)

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Matrix adjustment	$V_{16\text{-}1}$	2.5	3	3.5	dB	06, 1F, *Adjust. max*
Matrix adjustment	$V_{20\text{-}1}$	2.5	3	3.5	dB	06, 1F, *Adjust. max*
Matrix adjustment	$V_{9\text{-}1}$	2.5	3	3.5	dB	06, 1F, *Adjust. max*
Matrix adjustment	$V_{16\text{-}1}$	– 3.5	– 3	– 2.5	dB	06, 01, *Adjust. min*
Matrix adjustment	$V_{20\text{-}1}$	– 3.5	– 3	– 2.5	dB	06, 01, *Adjust. min*
Matrix adjustment	$V_{9\text{-}1}$	– 3.5	– 3	– 2.5	dB	06, 01, *Adjust. min*
Adjust. step wide	ΔV_{16}	0.1	0.2	0.3	dB	06, X- 06(X ± 1) *Adjust.X -Adjust.*(X ±1)
Adjust. step wide	ΔV_{20}	0.1	0.2	0.3	dB	06, X- 06(X ± 1) *Adjust.X-Adjust.*(X ± 1)
Adjust. step wide	ΔV_9	0.1	0.2	0.3	dB	06, X- 06(X ± 1) *Adjust.X-Adjust.*(X ± 1)
Bass boost	$V_{16\text{-}1}$	13	15		dB	05,8F; f_i = 40 Hz *Bass max, treble lin.*
Bass boost	$V_{15\text{-}3}$	13	15		dB	05,8F; f_i = 40 Hz *Bass max, treble lin.*
Bass boost	$V_{16\text{-}1}$		– 12		dB	05,8 0; f_i = 40 Hz *Bass min, treble lin.*
Bass boost	$V_{15\text{-}3}$		– 12		dB	05,8 0; f_i = 40 Hz *Bass min, treble lin.*
Step wide bass	ΔV_{15}	1	3	5	dB	05,8X- 05,8(X ± 1) *Bass X-bass*(X ± 1)
Step wide bass	ΔV_{16}	1	3	5	dB	05,8X- 05,8(X ± 1) *Bass X-bass*(X ± 1)
High-frequency emphasis	$V_{16\text{-}1}$	10	12		dB	05,F8 f_i = 15kHz *Treble max, bass lin.*
High-frequency emphasis	$V_{15\text{-}3}$	10	12		dB	05,F8 f_i = 15kHz *Treble max, bass lin.*
High-frequency emphasis	$V_{16\text{-}1}$		– 12		dB	05, 08 f_i = 15kHz *Treble min, bass lin.*
High-frequency emphasis	$V_{15\text{-}3}$		– 12		dB	05, 08 f_i = 15kHz *Treble min, bass lin.*
Step wide treble	ΔV_{15}	1	3	5	dB	05,X8- 05,(X ± 1)8 *Treble X-treble*(X ± 1)
Step wide treble	ΔV_{16}	1	3	5	dB	05,X8- 05,(X ± 1)8 *Treble X-treble*(X ± 1)
Linearity sound	ΔV_{15}			± 2	dB	05,88; fi = 40 Hz -15 kHz *Treble, bass lin.*
Linearity sound	ΔV_{16}			± 2	dB	05,88; f_i = 40 Hz -15 kHz *Treble, bass lin.*

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Channel separation	$\Delta V_{15\text{-}16}$	50			dB	V_3 or V_1 = 600 mV rms
Channel separation	$\Delta V_{19\text{-}20}$	50			dB	V_3 or V_1 = 600 mV rms
Channel separation	$\Delta V_{9\text{-}10}$	50			dB	V_3 or V_1 = 600 mV rms
Cross talk attenuation switch	a Input interf/ Output rms					
						$V_{I\,rms}$ = 0
						$V_{I\,Int1,3,6}$ = 600 mV rms
		60			dB	$V_{I\,Int\,7,8}$ = 2 V rms
Attenuation MUTE	$a_{1\text{-}16}$	80			dB	01, 0 0- 02, 0 0 *Vol* $_{LSl}$*0-Vol* $_{LSr}$*0* V_1 = 600 mV rms
Attenuation MUTE	$a_{1\text{-}16}$	80			dB	07,48; V_1 = 600 mV rms *MUTE I:0*
Attenuation MUTE	$a_{1\text{-}16}$	80			dB	07,88; V_1 = 600 mV rms *MUTE II:0*
Attenuation MUTE	$a_{3\text{-}15}$	80			dB	01, 0 0- 02, 0 0 $Vol_{LSl}0$-$Vol_{LSr}0$ V_3 = 600 mV rms
Attenuation MUTE	$a_{3\text{-}15}$	80			dB	07,48; V_3 = 600 mV rms *MUTE I:0*
Attenuation MUTE	$a_{3\text{-}15}$	80			dB	07,88; V_3 = 600 mV rms *MUTE II:0*
Attenuation MUTE	$a_{1\text{-}20}$	80			dB	03, 0 0; V_1 = 600 mV rms $Vol_{KH}0$
Attenuation MUTE	$a_{1\text{-}20}$	80			dB	07,48; V_1 = 600 mV rms *MUTE I:0*
Attenuation MUTE	$a_{3\text{-}19}$	80			dB	03, 0 0; V_3 = 600 mV rms $Vol_{KH}0$
Attenuation MUTE	$a_{3\text{-}19}$	80			dB	07,48; V_3 = 600 mV rms *MUTE I:0*
Analogous values are valid for feed-in at the pin 6, 7, 8; $V_{7,8}$ = 2 V_{rms}; V_6 = 600 mV_{rms}						
Attenuation MUTE	$a_{3\text{-}10}$	80			dB	07,48; V_3 = 600 mV rms *MUTE I:0*
Attenuation MUTE	$a_{1\text{-}9}$	80			dB	07,48; V_1 = 600 mV rms *MUTE I:0*
Attenuation MUTE	$a_{6\text{-}10}$	80			dB	07,49; V_6 = 600 mV rms *MUTE I:0, AM*
Attenuation MUTE	$a_{6\text{-}9}$	80			dB	07,49; V_6 = 600 mV rms *MUTE I:0, AM*

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Max.input voltage	V_6	600			mV_{rms}	$THD_{15,16}$ = 1 %
Max.input voltage	V_3	600			mV_{rms}	THD_{15} = 1 %
Max.input voltage	V_1	600			mV_{rms}	THD_{16} = 1 %
Max.input voltage	V_1	300			mV_{rms}	THD_{16} = 1 %; 00,02 *Matrix: Stereo*
Max.input voltage	V_7	2			V_{rms} V_{rms}	THD_{16} = 3 %; 07, CC, *SCART*
Max.input voltage	V_8	2			%	THD_{15} = 3 %; 07, CC, *SCART*
Distorsion	THD_{19}	0	0.01	0.1	%	V_3 = 250 mV_{rms}
Distorsion	THD_{20}		0.01	0.1	%	V_1 = 250 mV_{rms}
Distorsion	THD_{19}		0.01	0.1	%	V_3 = 250 mV_{rms}; 03,15 *Vol KH21*
Distorsion	THD_{20}		0.01	0.1	%	V_1 = 250 mV_{rms}; 03,15 *Vol KH21*
Analogous values are valid for feed-in at the pin 6, 7, 8 ; $V_{7,8}$ = 400 mV_{rms}; V_6 = 250 mV_{rms}						
Distorsion	THD_{16}		0.01	0.1	%	V_1 = 250 mV_{rms}
Distorsion	THD_{15}		0.01	0.1	%	V_3 = 250 mV_{rms}
Distorsion	THD_{16}		0.01	0.2	%	V_1 = 250 mV_{rms}; 01, 2 F-02,2F *Vol LSl47-Vol LSr47*
Distorsion	THD_{15}		0.01	0.2	%	V_3 = 250 mV_{rms}; 01, 2 F-02,2F *Vol LSl47-Vol LSr47*
Distorsion	THD_{16}		0.1	0.4	%	V_1 = 250 mV_{rms}; 05,XX *any sound*
Distorsion	THD_{15}		0.1	0.4	%	V_3 = 250 mV_{rms}; 05,XX *any sound*
Analogous values are valid for feed-in at the pin 6, 7, 8 ; $V_{7,8}$ = 400 mV_{rms}; V_6 = 250 mV_{rms}						

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.0	typ.0	max.0		
Distorsion	THD_{10}		0.01	0.1	%	V_3 = 250 mV rms
Distorsion	THD_9		0.01	0.1	%	V_1 = 250 mV rms
Distorsion	THD_{10}		0.01	0.1	%	V_6 = 250 mV rms, 07,C9,*AM*
Distorsion	THD_9		0.01	0.1	%	V_6 = 250 ,mV rms; 07,C9, *AM*
Antiphase Cross talk atten.	$\Delta V_{16\text{-}15}$					V_3 = 600 mV rms
Base width		0.5	0.55			f_i = 2kHz; 00,11, *Basis width*
Antiphase Cross talk atten.	$\Delta V_{15\text{-}16}$					V_1 = 600 mV rms
Base width		0.5	0.55			f_i = 2 kHz; 0011, *Basis width*
Base width phase	$\Phi_{16\text{-}15}$	150	180	210	deg	V_1 = 600 mV rms; 00,11 *Basis width*, f = 2 kHz
Base width phase	$\Phi_{15\text{-}16}$	150	180	210	deg	V_3 = 600 mV rms; 0011 *Basis width*, f = 2 kHz
Phase rotation quasi-stereo	$\Phi_{16\text{-}15}$	0	10	40	deg	$V_{3,1}$ = 600 mV rms; 00,21 *Quasi-stereo*, f = 40 Hz

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.0	typ.	max.		
Phase rotation quasi-stereo	$\Phi_{16\text{-}15}$	130	180	230	deg	$V_{3,1}$ = 600 mV rms; 0021 *Quasi-stereo*, f = 1 kHz
Phase rotation quasi-stereo	$\Phi_{16\text{-}15}$	– 30	10	0	deg	$V_{3,1}$ = 600 mV rms; 00,21 *Quasi-stereo*, f = 15 kHz
Unweighted signal-to-noise ratio	$a_{S/N\,16}$	1	90	97	dB	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0,6 V rms
Unweighted signal-to-noise ratio	$a_{S/N\,15}$	1	90	97	dB	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$; V_3 = 0,6 V rms
Unweighted signal-to-noise ratio	$a_{S/N\,16}$	70	80		dB	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0,6 V rms 01,27-02,27 *Vol* $_{LSl}$*39*-*Vol* $_{LSr}$*39*
Unweighted signal-to-noise ratio	$a_{S/N\,15}$	70	80		dB	$V_{N\,rms\ 20\ hz\text{-}20\ kHz}$; V_3 = 0,6 V rms 01,27-02,27 *Vol* $_{LSl}$*39*-*Vol* $_{LSr}$*39*
External voltage	V_{N15}		2	10	µV rms	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$ 01,00-02,00 *Vol* $_{LSl}$*0*-*Vol* $_{LSr}$*0*
External voltage	V_{N16}		2	10	µV rms	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$ 01,00-02,00 *Vol* $_{LSl}$*0*-*Vol* $_{LSr}$*0*
Unweighted signal-to-noise ratio	$a_{S/N\,20}$	90	97		dB	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0,6 V rms
Unweighted signal-to-noise ratio	$a_{S/N\,19}$	1	90	97	dB	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$; V_3 = 0,6 V rms
Unweighted signal-to-noise ratio	$a_{S/N\,20}$	70	80		dB	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0,6 V rms 03, 10, Vol $_{KH}$16
Unweighted signal-to-noise ratio	$a_{S/N\,19}$	70	80		dB	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$; V_3 = 0,6 V rms 03, 10, Vol $_{KH}$16
External voltage	V_{N20}		2	10	µV rms	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$; 03,00 *Vol* $_{KH}$*0*
External voltage	V_{N19}		2	10	µV rms	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$; 03,00 *Vol* $_{KH}$*0*
Unweighted signal-to-noise ratio	$a_{S/N\,9}$	1	90	97	dB	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$; V_1 = 0,6 V rms
Unweighted signal-to-noise ratio	$a_{S/N\,10}$	1	90	97	dB	$V_{N\,rms\ 20\ Hz\text{-}20\ kHz}$; V_3 = 0,6 V rms

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Change of DC-switch Δ1 Bit	ΔV_{16}			± 10	mV	01,X-01,X ± 1 *Vol_{LSl}X-Vol_{LSl}(X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{15}			± 10	mV	02,X-02,X±1 *Vol_{LSr}X-Vol_{LSr}* (X ± 1)
Change of DC-switch Δ1 Bit	ΔV_{16}			± 10	mV	05,X-05,X 1 *Sound X-Sound (X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{15}			± 10	mV	0,X-05,X ± 1 *Sound X-Sound (X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{19}			± 10	mV	03,X-03,X ± 1 *Vol_{KH}X-Vol_{KH} (X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{20}			± 10	mV	03,X-03,X ± 1 *Vol_{KH}X-Vol_{KH} (X ± 1)*

Design-Related Data

Input resistance	R_7	35			kΩ	
Input resistance	R_8	35			kΩ	
Input resistance	R_6	20			kΩ	
Input resistance	R_3	20			kΩ	
Input resistance	R_1	20			kΩ	
Output resistance	R_{19}			200	Ω	
Output resistance	R_{20}			200	Ω	
Output resistance	R_{15}			200	Ω	
Output resistance	R_{16}			200	Ω	
Output resistance	R_9			200	Ω	
Output resistance	R_{10}			200	Ω	

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
ID Signal Decoder							
Gain Filter OP-amp	V_5	13	14	15	dB	V_{IF} = 80 mV$_{pp}$	1
Max. input voltage	V_5	600			mV$_{pp}$	Function	2
VCO voltage PLL	V_{27}	tbf			V	f_{24} = 14.6 kHz; V_{24} = 2.5 V$_{os}$	2
VCO voltage PLL	V_{27}	tbf	3	tbf	V	f_{24} = 15.625 kHz; V_{24} = 2.5 V$_{os}$	2
VCO voltage PLL	V_{27}			tbf	V	f_{24} = 16.6 kHz; V_{24} = 2.5 V$_{os}$	2
VCO voltage PLL	V_{27}					f_{24} = 58.4 kHz; V_{24} = 2.5 V$_{os}$	
		tbf			V	00,09, H-Imp	2
VCO voltage PLL	V_{27}					f_{24} = 66.4 kHz; V_{24} = 2.5 V$_{os}$	
				tbf	V	00,09, H-Imp	2

$$V_{KT\ Filter} = \frac{\sqrt{(V_{25} - V_{25}^*)^2 + (V_{26} - V_{26}^*)^2}}{V_5}$$

V_{25} or V_{26} when V_5 = 0
V_{25}^* or V_{26}^* when V_5 = 400 mV$_{pp}$

ID filter gain		tbf		tbf		$V_{KT\ Filter}$ f_5 = 54.962 kHz I²C talk: Dual	2
ID filter gain		tbf		tbf		$V_{KT\ Filter}$ f_5 = 54.805 kHz I²C talk: Stereo	2

$V_{25\ test} = V_{25\,(V_{5\,=\,0})} \pm \Delta V_{25}$; $V_{26\ test} = V_{26\,(V_{5\,=\,0})} \pm \Delta V_{26}$

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Detection threshold	ΔV_{25}	tbf			mV	I²C talk: Stereo o. Dual	3
Detection threshold	$-\Delta V_{25}$	tbf			mV	I²C talk: Stereo o. Dual	3
Detection threshold	ΔV_{26}	tbf			mV	I²C talk: Stereo o. Dual	3
Detection threshold	$-\Delta V_{26}$	tbf			mV	I²C talk: Stereo o. Dual	3
Mono threshold	ΔV_{25}	0		tbf	mV	I²C talk: Mono	3
Mono threshold	$-\Delta V_{25}$	0		tbf	mV	I²C talk: Mono	3
Mono threshold	ΔV_{26}	0		tbf	mV	I²C talk: Mono	3
Mono threshold	$-\Delta V_{26}$	0		tbf	mV	I²C talk: Mono	3
Response of detection	t_{det}	1/4		1/2	t_{MPX}	I²C talk: Stereo o Dual $\pm\Delta V_{25}$ = 1V	3
Response of detection	t_{det}	1/4		1/2	t_{MPX}	I²C talk: Stereo o Dual $\pm\Delta V_{26}$ = 1V	3
Switching threshold f_{REF}-input	V_{24L}	0		1.5	V		2
Switching threshold f_{REF}-input	V_{24H}	3.5		V_{21}	V		2
Multiplexer takt	t_{MPX}		1.08		s	00,C0, MPX = 1 s	
Multiplexer takt	t_{MPX}		2.17		s	00,00, MPX = 2 s	
Multiplexer takt	t_{MPX}		4.34		s	00,40, MPX = 4 s	
Multiplexer takt	t_{MPX}		8.68		s	00,80, MPX = 8 s	

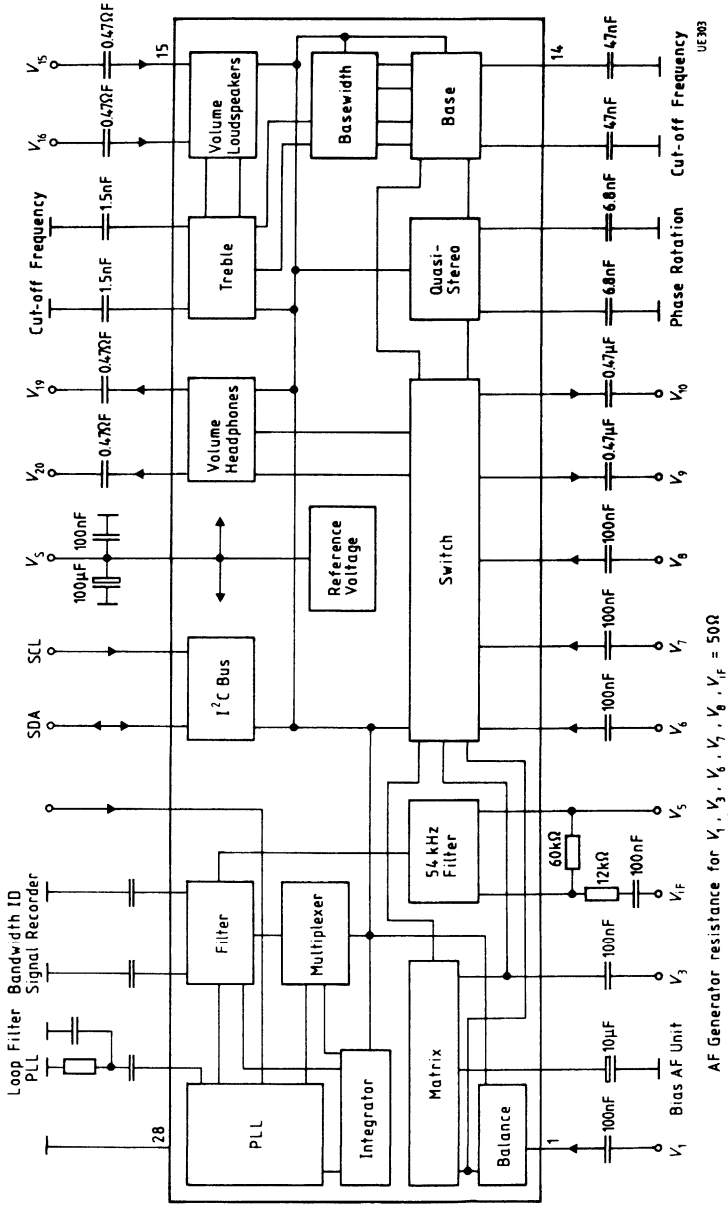
Design-Related Data

Filter output resistance	$R_{25,26}$	110			kΩ		
f_{REF} input resistance	R_{24}	7			kΩ		

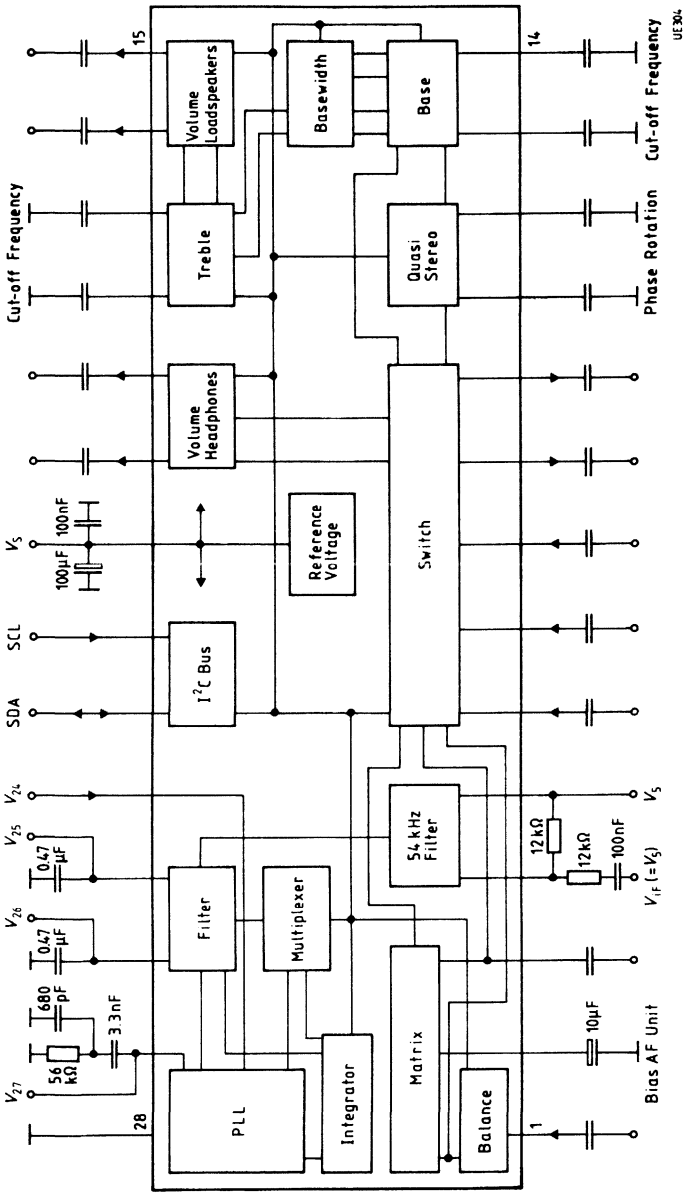
Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
I²C-B Bus (SCL, SDA)					
SCL, SDA edges					
Rise time	t_R			1	µs
Fall time	t_F			300	ns
Shift register clock pulse SCL					
Frequency	f_{SCL}	0		100	kHz
H-pulse width	t_{HIGH}	4			µs
L-pulse width	t_{LOW}	4			µs
Start					
Set-up time	t_{SUSTA}	4			µs
Hold time	t_{HDSTA}	4			µs
Stop					
Set-up time	t_{SUSTO}	4			µs
Bus free time	t_{BUF}	4			µs
Data transfer					
Set-up time	t_{SUDAT}	1			µs
Hold time	t_{HDDAT}	1			µs
Input SCL, SDA					
Input voltage	V_{QH}	2.4		5.5	V
	V_{QL}			1	V
Input current	I_{QH}			50	µA
	I_{QL}			100	µA
Output SDA (open collector)					
Output voltage	V_{QH}	5.4			V
R_L = 2.5 kΩ	V_{QL}			0.4	V
I_{QL} = 3 mA					

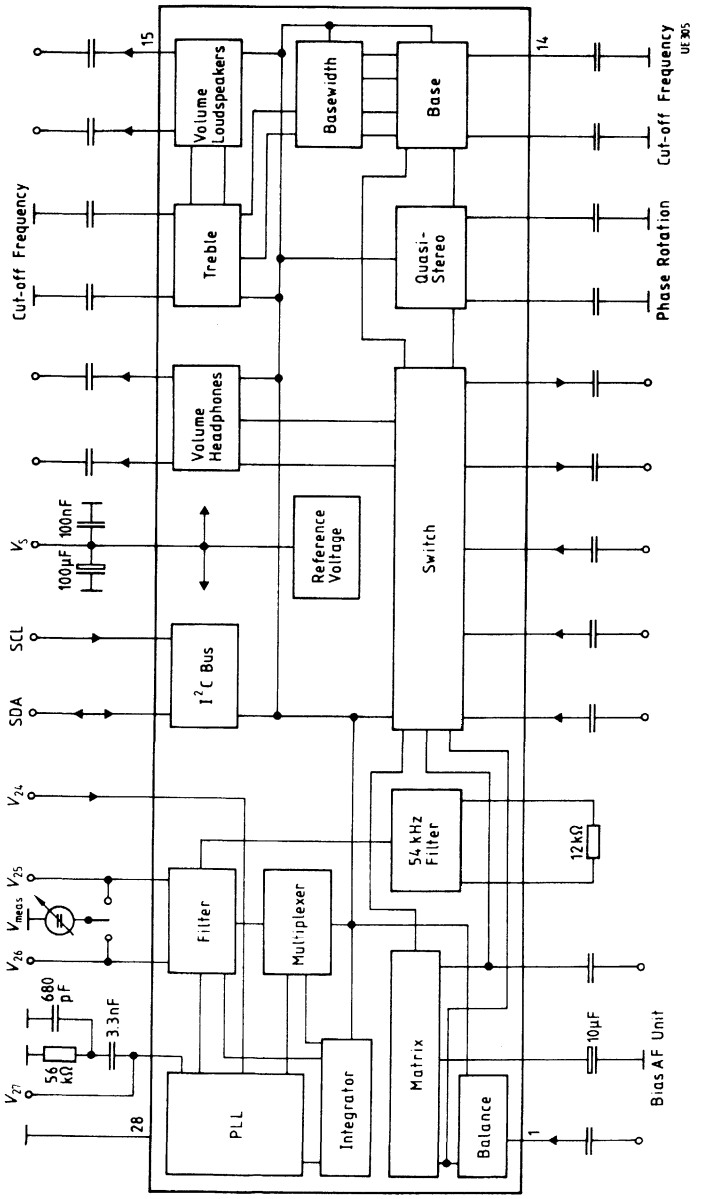
Test Circuit 1



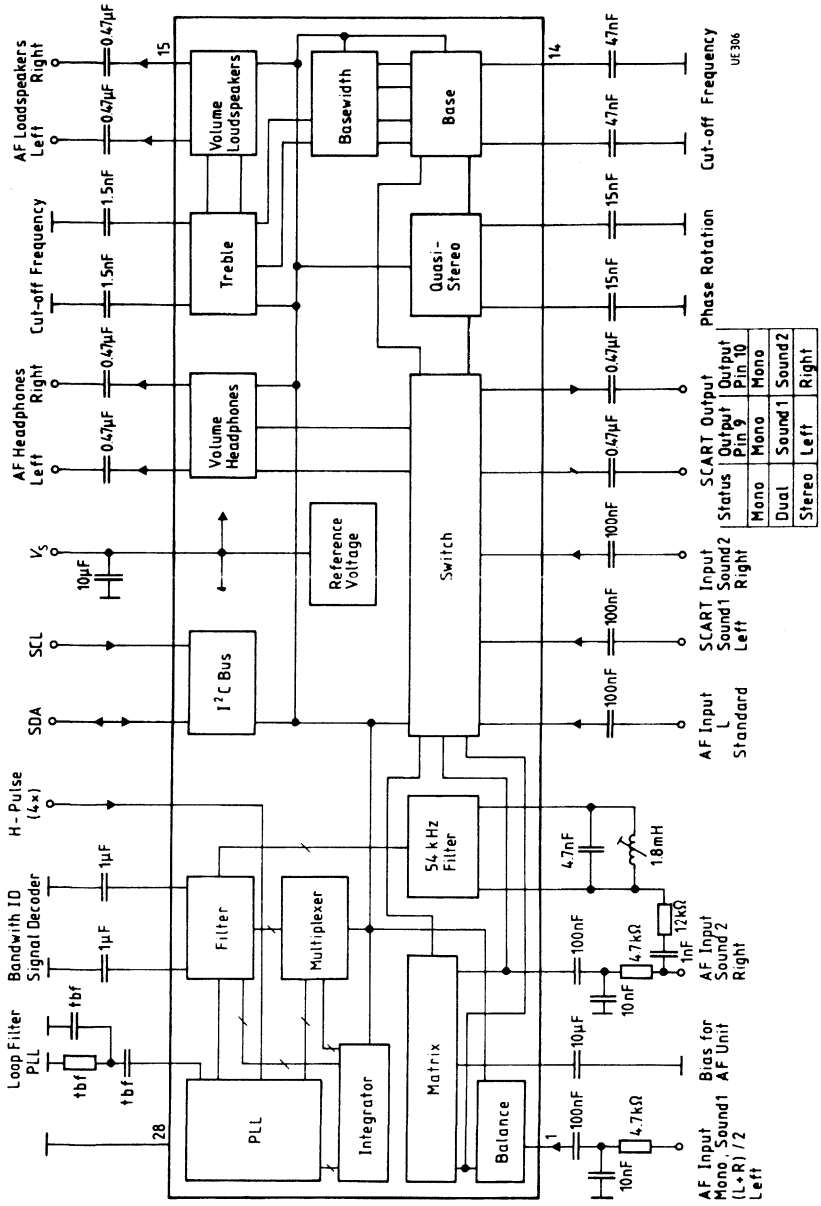
Test Circuit 2



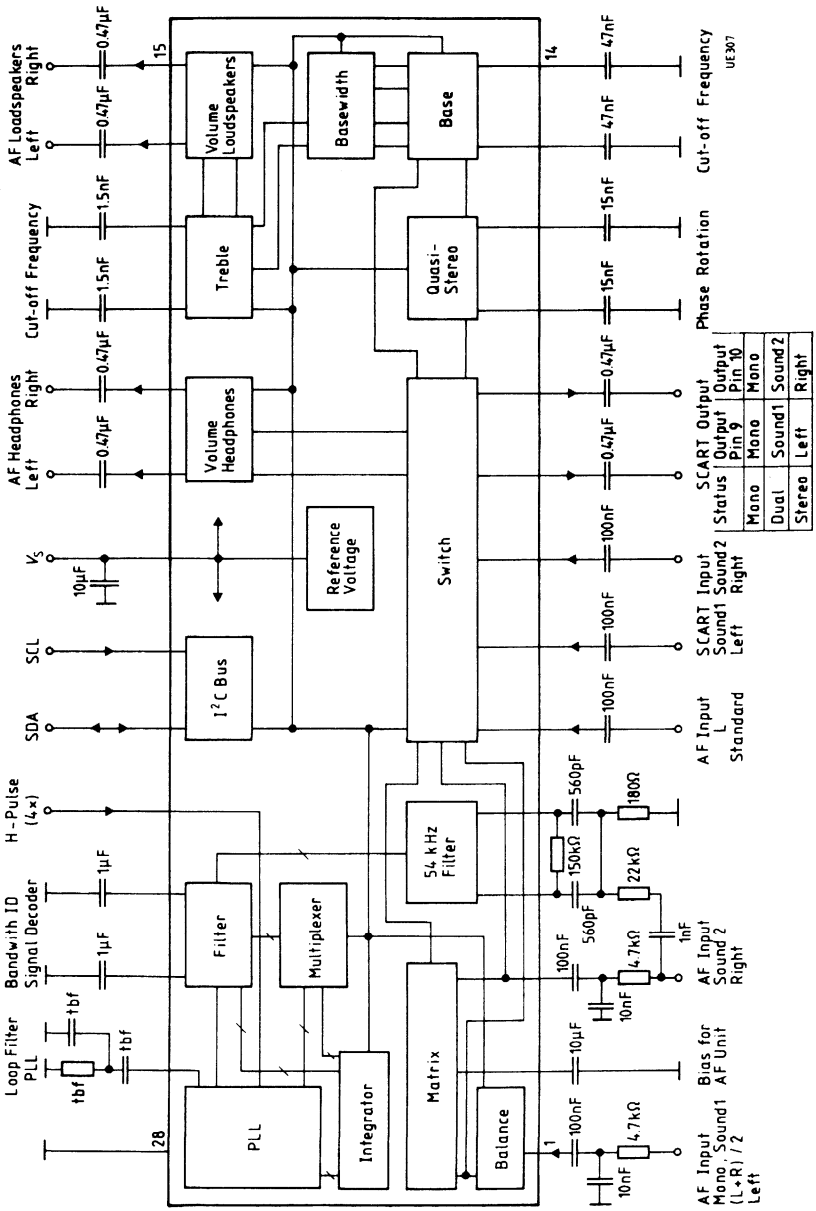
Test Circuit 3



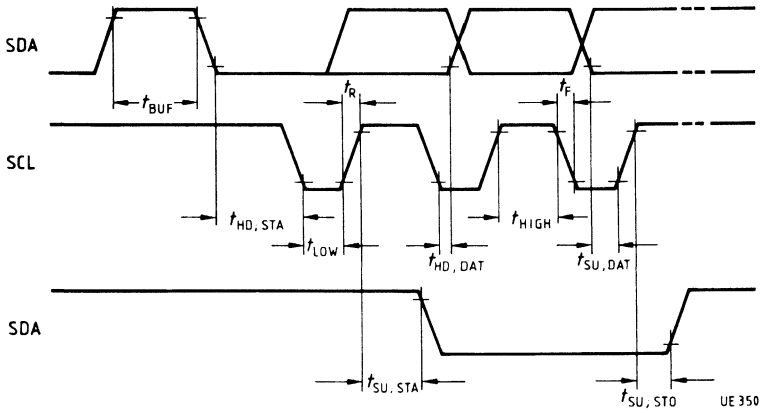
Application Circuit 1



Application Circuit 2



I²C Bus Timing Diagram



t_{SUSTA}	Set-up time (start)
t_{HDSTA}	Hold time (start)
t_{HIGH}	HIGH pulse width (clock)
t_{LOW}	LOW pulse width (clock)
t_{SUDAT}	Set-up time (data transfer)
t_{HDDAT}	Hold time (data transfer)
t_{SUSTO}	Set-up time (stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

All times are referenced to the V_{IH} and V_{IL} values

SIEMENS

VCR Stereo Processor — TDA 6620

Preliminary Data — **Bipolar IC**

Features

- Inexpensive solution for VCR sets due to a low cost external writing
- Identification signal based on the PLL-principle
- The PLL reference frequency can be derived from external or internal clock generator
- Bandwidth of the identification signal decoder can be elected (narrow band selection)

The TDA 6620 represents a complete VCR stereo sound system controlled via the I^2C bus. The IC is divided into three functional blocks:

Stereo sound processing

- Stereo matrix for two carrier stereo sound systems
- Additional single-channel AF input (for e.g. AF signal accord. L-standard)
- AF output with options to select the sound signal to be recorded during dual tone

TV sound identification signal decoder consisting of

- Active pilot signal filter.
- Phase-independent rectifier with very narrow bandwidth for evaluation of the identification signal.
- Digital integrator to reduce interference
- Multiplexer for cyclical switch over between "stereo" or "dual" evaluation
- PLL for the generation of the reference signal. External synchronization with either the flyback pulse or external reference clock signals of 62.5 kHz or 4 MHz is possible. 4 MHz can also be generated using the internal crystal generator with an external crystal

Control section for

- I^2C bus interface with listen and talk function
- Control of the complete AF sound processing
- Control of the identification signal decoder
- Reading of the identification signal decoder status
- Test modes

Type	Ordering Code	Package
TDA 6620	Q67000-A8197	P-DIP-18

Circuit Description

1. Signal Section

The audio signal processing in the matrix and the switch-over for multichannel TV sound signals according to the two-carrier system used in Germany takes place in the matrix and switching sections.
In addition to the two inputs for the demodulated sound carriers, an additional mono input (e.g. for demodulated L-standard sound) is provided. The two AF inputs can be bypassed internally in such a way that decoded stereo sound signals of other audio systems (NICAM) can be processed. The switching section includes also the Ch1/Ch2 switch for the AF signal to be recorded during dual sound transmission. (Sound 1 or Sound 2, or Sound 1 and Sound 2).

2. Identification Signal Decoder

The input of the identification signal decoder consists of a selective op-amp for the pilot signal with its sidebands. An external LC circuit is used. The signal is then passed to a phase-independent active bandpass filter with a very narrow bandwidth (adjustable externally). This filter detects whether the lower sideband of the pilot carrier, which is modulated with the identification signal, is present. The center frequency of the filter is switched between "dual" and "stereo" by a multiplexer. The multiplexing frequency is adjustable by software. If a sideband is detected, the multiplexer will stop. This first "detected" criterion is rendered free from interference by a digital integrator with a following comparator and can be read out via I^2C bus (talk mode) as the "stereo" or "dual" mode. The control of the corresponding signal can be either directly internally or through the µC. All the necessary clock signals are derived from a fast settling PLL which is synchronized by a reference frequency. This reference frequency must be sufficiently close to the horizontal frequency, but **a rigid phase coupling is not required.** Therefore, alternatively the use of a crystal-controlled 62.5-kHz frequency commonly found in PLL tuning systems is possible. Further options are given by an integral crystal oscillator which must be provided with a 4-MHz, crystal is a 4-MHz clock frequency is available.

3. Control Section

All functions are controlled via an I^2C bus interface with listen/talk functions. The current applicable data are stored in a block of latches.

The telegram structure is formed in the following manner:
Start Condition - Chip Address – any number of bytes – Stop Condition

The following conditions apply to the data bytes:
Before the actual data byte (with the adjustment information), a subaddress by the I^2C bus byte must **always** be transmitted. This byte however, is interpreted as a data byte interface.

Within a telegram (i.e. without a new start condition) any different subaddresses can be accessed. The changeover between "listen" and "talk" however must always occur via the sequence stop condition – start condition – chip address. Before each readout a start condition and chip address (talk) must always be transmitted. The data to be read out are loaded into the I^2C bus interface and can be transferred to the μC

Chip Address

	MSB	.	.	.	.	.	.	LSB
	1	0	0	0	0	1	1	R/W

R/W = 0 → read (listen)

R/W = 1 → write (talk)

Subaddress Bytes

	MSB	.	.	.	.	.	.	LSB
Switch byte I	X	X	X	X	X	1	1	1
Switch byte II	X	X	X	X	X	0	0	0

Switch Byte I

MSB							LSB
MUTE	Qu-H	Ch1/Ch2	X	Mono	X	$Ch1/Ch2_{EN}$	AM

MUTE = 0 AF outputs muted; Power on
MUTE = 1 AF outputs on

Qu-H = 0 PLL synchronization with H pulse; power on
Qu-H = 1 PLL synchronization with crystal oscillator

Ch1/Ch2 = 0 Sound 1 on the AF outputs; power on
Ch1/Ch2 = 1 Sound 2 on the AF outputs

Ch1/Ch2 and $Ch1/Ch2_{EN}$ are only effective when the matrix is set to status "dual sound"

Mono = 0 Identification signal decoder is set into the monstatus and held; power on
Mono = 1 Normal operation of the identification signal decoder

$Ch1/Ch2_{EN}$ = 0 Enable for the Ch1/Ch2 switches; power on
$Ch1/Ch2_{EN}$ = 1 Playback stereo, mono or dual (Sound 1 and Sound 2)

AM = 0 Normal operation (G standard)
AM = 1 AM AF input is activated; power on
AM = 1 has priority over bypass = 1

Switch Byte II

MSB							LSB
MPX0	MPX1	X	X	H pul.	Matrix 0	Matrix 1	Bypass

MPX0	MPX1	MPX period		recommended $C_{15,16}$
0	0	2 s	power on	1 µF
0	1	4 s		2.2 µF
1	0	8 s		4.7 µF
1	1	1 s		470 nF

MPX period = 2 s signified: ID signal decoder searches during 1 second for "dual" and during the next second for "stereo".

H pul.	= 0	ID signal decoder synchronization with f_H = 15.625 kHz; power on
H pul.	= 1	ID signal decoder synchronization with 4 x f_H

Matrix 0	Matrix 1	matrix status	
0	0	mono	power on
0	1	stereo	
1	0	dual	
1	1	automatic according to ID signal decoder	

Bypass	= 0	normal operation (G standard)
Bypass	= 1	matrix is bypassed so that left/right signals can be fed in the audio inputs, power on (AM = 1 has priority over bypass = 1)

Priority List of the Setting Bits

1. MUTE
2. AM
3. Bypass
4. Matrix 0, 1

Control of the Matrix

The control of the matrix can be done either directly by means of the identification signal decoder or the status be forced via the I^2C bus. If the transmitter changes the sound status this is recognized and the related information is stored in the corresponding registers. If the two bits "matrix 0" and "matrix 1" are set to 1, the switching of the matrix is done automatical according to correct status of the program source.

If these bits are set to all other possible combinations of these bits (00,01 and 10) the switching of the matrix has to be done by means of the processor.
The identification signal decoder implemented into this device is operating continously The evaluated informations about the sound status are available for the tranfer to the processor via the I^2C bus.

Initialisation during a Change of the Preset (on Program)

The status "mono" has to be set during the preset change. Otherwise a short misdecoding is possible. The normal operation of the identification decoder is activated

Control of the "Dual" Switch

During the activation phase the bit "Ch1/Ch2 $_{en}$" is set to logical "0". In the operation mode "dual", both audio signals are switched to the output and recorded on the tape.
The setting of the bit "Ch1/Ch2 $_{en}$" to logical "1" enables a switch which makes it possible to make a selection of the audio signal previous to the recording.

This is shown in the following table:

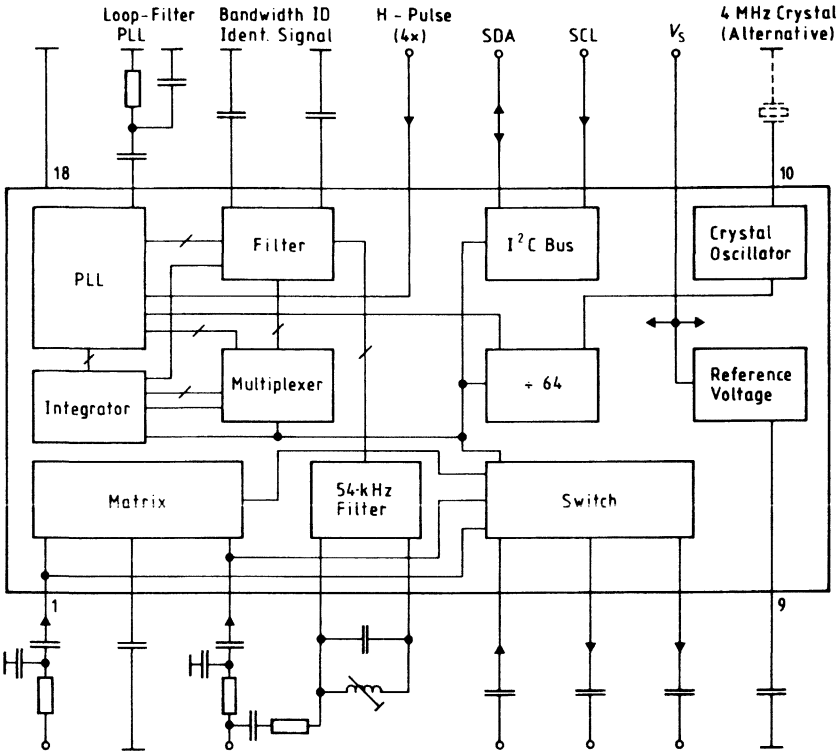
	Output Signals of Both of the AF Outputs:		
Decoder Status	**Stereo**	**Mono**	**Dual**
Ch1/Ch2 $_{en}$ = "0"	right + left	Mono	Sound 1 and Sound
Ch1/Ch2 $_{en}$ = "1"	right + left	Mono	Sound 1 or Sound 2

Talk Mode

MSB	.	.	.	.	.	.	LSB
St	D	T5	T4	T3	X	X	X
0	0	decoder detects mono					
1	0	decoder detects stereo					
0	1	decoder detects dual					
1	1	internally inhibited					

T3 – T5 are test bits.

Block Diagram



Status	Output Pin 7	Output Pin 8
Mono	Mono	Mono
Dual	Sound 1	Sound 2
Stereo	Left	Right

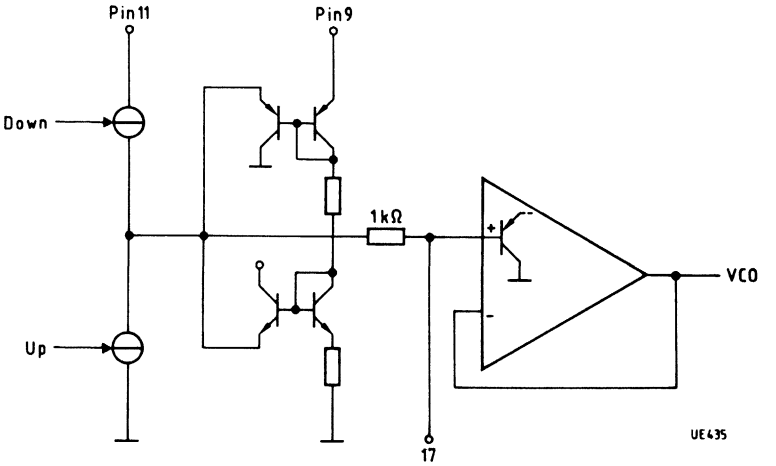
UE 433

Pin Functions

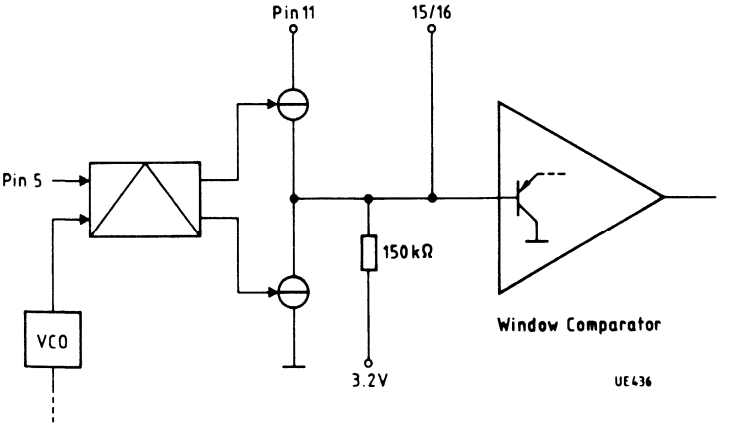
Pin No.	Function
1	AF input, left, Sound 1
2	Bias for AF operating point
3	AF input, right, Sound 2
4	54-kHz input filter amplifier
5	54-kHz filter amplifier output
6	AF input (L-standard)
7	AF output (left, Sound 1, mono, dual)
8	AF output (right, Sound 2, mono, dual)
9	6 V reference voltage
10	Crystal oscillator
11	$+V_S$ (supply voltage)
12	I^2C bus SCL
13	I^2C bus SDA
14	Input, flyback pulse (or 4 × H pulse)
15	Filter ID decoder
16	Filter ID decoder
17	PLL filter ID decoder
18	Ground

Pin Descriptions and Functions

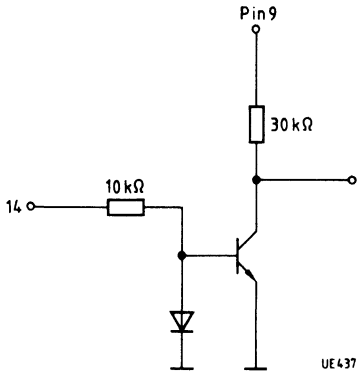
PLL Filter ID Signal Decoder (Pin 17)



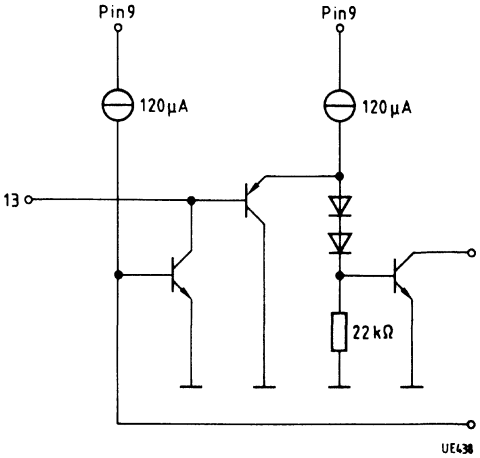
Filter ID Signal Decoder (Pin 15, 16)



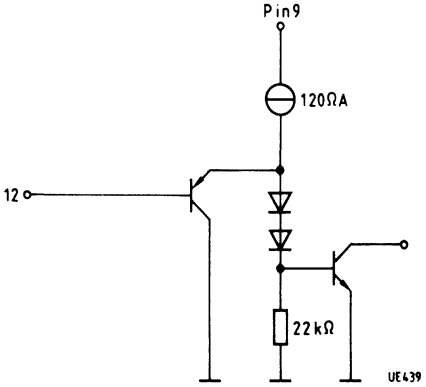
Input H Pulse (Pin 14)



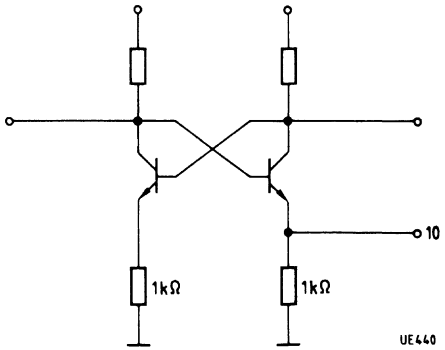
I²C Bus SDA (Pin 13)



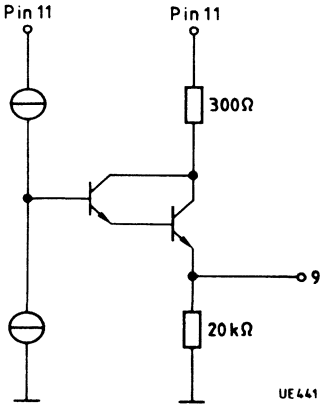
I²C Bus SCL (Pin 12)



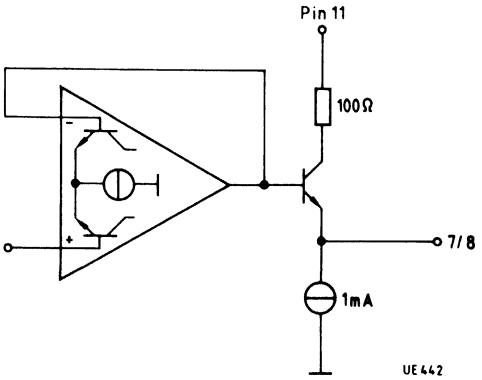
Crystal Oscillator (Pin 10)



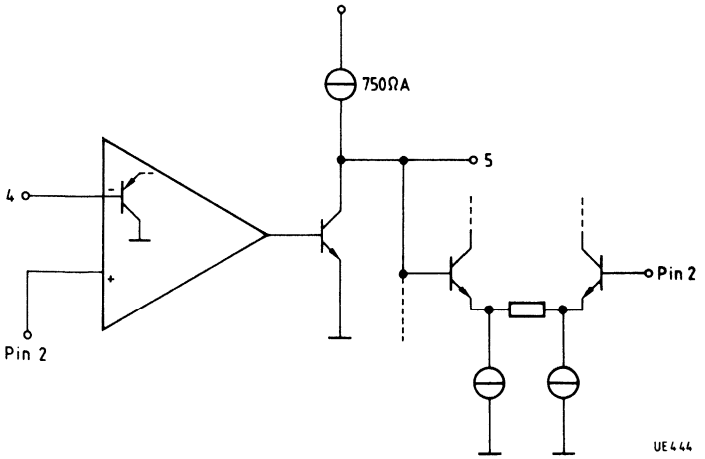
Reference Voltage (Pin 9)



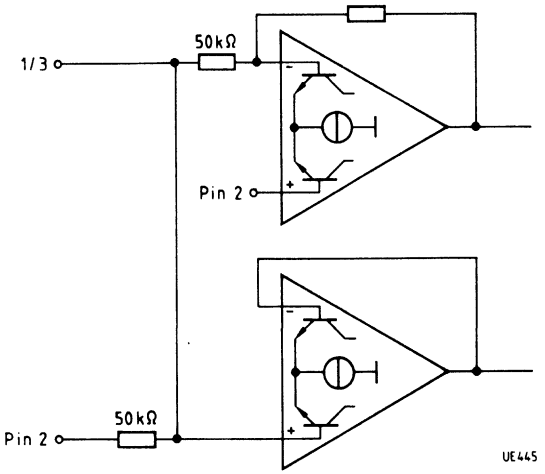
AF Outputs (Pin 7, 8)



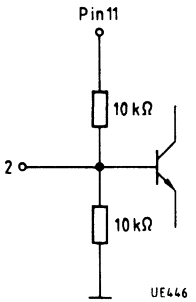
54-kHz Filter (Pin 4, 5)



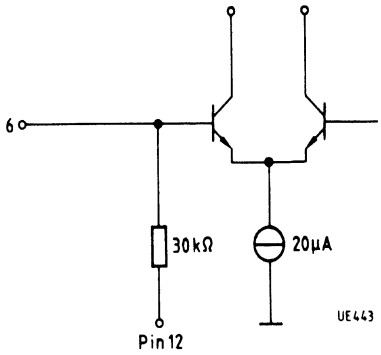
AF Inputs (Pin 1, 3)



Blocking AF Operating Point (Pin 2)



AF Input AM (Pin 6)



Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{11}	0	20	V
Max. DC voltage	V_1	0	V_{11}	V
Max. DC voltage	V_2	0	V_{11}	V
Max. DC voltage	V_3	0	V_{11}	V
Max. DC voltage	V_4	0	V_{11}	V
Max. DC voltage	V_6	0	V_{11}	V
Max. DC voltage	V_7	0	V_{11}	V
Max. DC voltage	V_8	0	V_{11}	V
Max. DC voltage	V_{12}	0	V_{11}	V
Max. DC voltage	V_{13}	0	V_{11}	V
Max. DC voltage	V_{14}	0	V_{11}	V
Max. DC voltage	V_{15}	0	V_{11}	V
Max. DC voltage	V_{16}	0	V_{11}	V
Max. DC current	I_5	0	2	mA
Max. DC current	I_9	0	2	mA
Max. DC current	I_{10}	0	2	mA
Max. DC current	I_{17}	0	1	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-ambient)	$T_{th\,SA}$		59	K/W

Operating Range

Supply voltage	V_S	10	13.2	V
Ambient temperature	T_A	0	70	°C
Input frequency range	f	0.01	20	kHz

Characteristics

V_S = 12 V; T_A = 25 °C

I²C Bus Preset: Start - 07,C8 - 0 0, 01 - Stop

MUTE, Mono - Bypass

The basic setting for each point in the specification is always present; only settings which deviate from this are given in the test condition. Details in *italics* only provide explanation of the hexadecimal code and which switch bits on the set bits and feature are stated.

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Current consumption	I_{11}		tbf		mA		1

Signal Section

Gain	$V_{7\text{-}1}$	– 2	0	2	dB		1
Gain	$V_{8\text{-}3}$	– 2	0	2	dB		1
Gain	$V_{8\text{-}3}$	– 2	0	2	dB	*00,02; Matrix: Stereo* $V1 = 0$	1
Gain	$V_{7\text{-}3}$	– 2	0	2	dB	00,02; *Matrix: Stereo* $V_1 = 0$	1
Gain	$V_{7\text{-}1}$	4	6	8	dB	00,02; *Matrix: Stereo* $V_3 = 0$	1
Gain	$V_{7\text{-}6}$	– 2	0	– 2	dB	07,C9, *AM*	1
Gain	$V_{8\text{-}6}$	– 2	0	– 2	dB	07,C9, *AM*	1
Tracking deviation	$\Delta V_{7\text{-}8}$			± 2	dB		1
Crosstalk rejection switch	a_{Input}	60			dB	interference/ useful output $V_{\text{I useful}} = 0$ $V_{\text{I int I,3,6}} = 600$ mV$_{\text{rms}}$	1
Attn. during MUTE	$a_{1\text{-}7}$	80			dB	07,08; *MUTE:0* $V_1 = 600$mV$_{\text{rms}}$	1
Attn. during MUTE	$a_{3\text{-}8}$	80			dB	07,08; *MUTE:0* $V_3 = 600$ mV$_{\text{rms}}$	1

Similar values apply for input to pin 6; $V_6 = 600$ mV$_{\text{rms}}$

Max. input voltage	V_6	600			mV$_{\text{rms}}$	$THD_{7,8} = 1$ %	1
Max. input voltage	V_3	600			mV$_{\text{rms}}$	$THD_8 = 1$ %	1
Max. input voltage	V_1	600			mV$_{\text{rms}}$	$THD_7 = 1$ %	1
Max. input voltage	V_1	300			mV$_{\text{rms}}$	$THD_7 = 1$ %; 00,02 *Matrix: Stereo*	1

Characteristics (cont 'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Harmonic distorsion	THD_7			0.2	%	V_1 = 250 mVrms	1
Harmonic distorsion	THD_8			0.2	%	V_3 = 250 mVrms	1
Similar values apply for input to pin 6; V_6 = 250 mVrms							
Noise level, unweight.	$a_{S/N7}$	90	97		dB	V_N rms 20 Hz – 20 kHz; V_1 = 0.6V rms	1
Noise level, unweight.	$a_{S/N8}$	90	97		dB	V_N rms 20 Hz – 20 kHz; V_3 = 0.6 V rms	1
Change of DC switch	ΔV_7			± 10	mV		1
Change of DC switch	ΔV_8			± 10	mV		1
Design-Related Data							
Input resistance	R_3	20			kΩ		
Input resistance	R_1	20			kΩ		
Output resistance	R_7			200	Ω		
Output resistance	R_8			200	Ω		
ID Signal Decoder							
Gain Filter OP-amp	V_5	13	14	15	dB	V_{IF} = 80 mVpp	1
Max. input voltage	V_5	600			mVpp	operation	2
VCO voltage PLL	V_{17}	tbf			V	f_{14} = 14.6 kHz; V_{14} = 2.5 Vop	2
VCO voltage PLL	V_{17}	tbf		tbf	V	f_{14} = 15.625 kHz; V_{14} = 2.5Vop	2
VCO voltage PLL	V_{17}			tbf	V	f_{14} = 16.6 kHz; V_{14} = 2.5Vop	2
VCO voltage PLL	V_{17}	tbf tbf			V V	f_{14} = 58.4 kHz; V_{14} = 2.5 Vop 00,09, H pulse	2 2
VCO voltage PLL	V_{17}			tbf	V	f_{14} = 66.4 kHz; V_{14} = 2.5Vop 00,09, *H pulse*	2
VCO voltage PLL	V_{17}	tbf		tbf	V	07,C8, *crystal operation*	2

$$V_{KT\ Filter} = \frac{\sqrt{(V_{15} - V_{15}^*)^2 + (V_{16} - V_{16}^*)^2}}{V_5}$$

V_{15} or V_{16} when V_5 = 0
V_{15}^* or V_{16}^* when V_5 = 400 mVpp

ID filter gain	$V_{KT\ Filter}$	tbf		tbf		f_5 = 54.962 kHz I²C talk: Dual	2
ID filter gain	$V_{KT\ Filter}$	tbf		tbf		f_5 = 54.805 kHz I²C talk: Stereo	2

*$V_{15\ meas} = V_{15\ (V5\ =\ 0)} \pm \Delta V_{15}$; $V_{16\ meas} = V_{16\ (V5\ =\ 0)} \pm \Delta V_{16}$

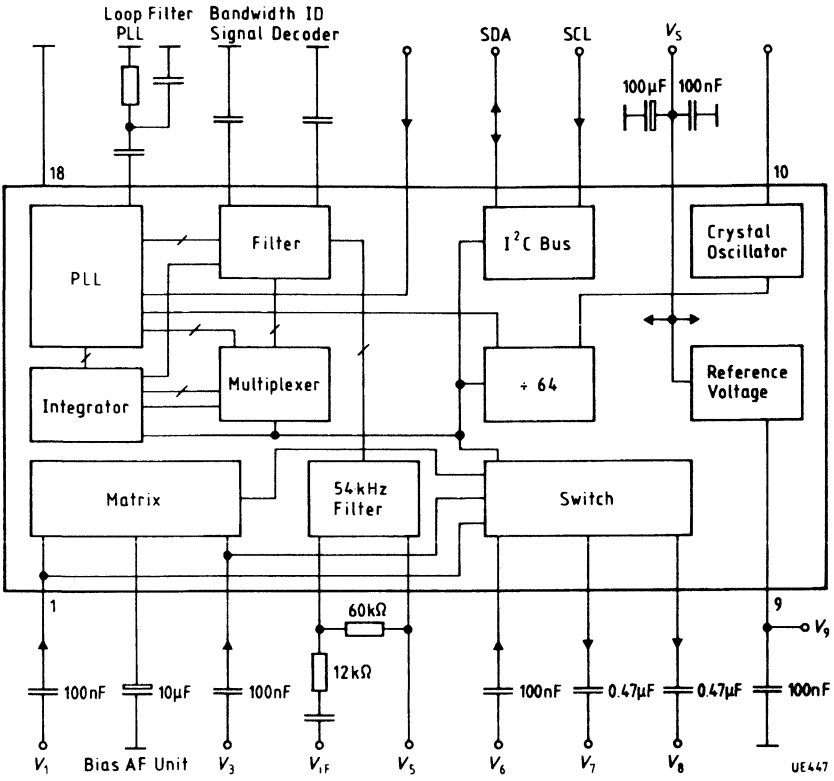
Characteristics (cont 'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Detection threshold	ΔV_{15}	tbf			mV	I²C talk: Stereo o. Dual	3
Detection threshold	$-\Delta V_{15}$	tbf			mV	I²C talk: Stereo o. Dual	3
Detection threshold	ΔV_{16}	tbf			mV	I²C talk: Stereo o. Dual	3
Detection threshold	$-\Delta V_{16}$	tbf			mV	I²C talk: Stereo o. Dual	3
Mono threshold	ΔV_{15}	0		tbf	mV	I²C talk: Mono	3
Mono threshold	$-\Delta V_{15}$	0		tbf	mV	I²C talk: Mono	3
Mono threshold	ΔV_{16}	0		tbf	mV	I²C talk: Mono	3
Mono threshold	$-\Delta V_{16}$	0		tbf	mV	I²C talk: Mono	3
Response of detection	$t_{detect.}$	1/4		1/2	t_{MPX}	I²C talk: Stereo o. Dual $\pm\Delta V_{15}$ = 1 V	3
Response of detection	$t_{detect.}$	1/4		1/4	t_{MPX}	I²C talk: Stereo o. Dual $\pm\Delta V_{16}$ = 1 V	3
Switching threshold f_{REF}-input	V_{14L}	0		1.5	V		2
Switching threshold f_{REF}-input	V_{14H}	3.5		V_{11}	V		2
Amplitude crystal oscillator ext. 4-MHz clock signal	V_9 V_9	tbf 0.3		tbf	V_{pp} V_{pp}	f_{OSC} = 4.00000 MHz series resonance	2 3
Multiplexer clock	t_{MPX}		1.08		s	00,C0, *MPX = 1 s*	
Multiplexer clock	t_{MPX}		2.17		s	00,00, *MPX = 2 s*	
Multiplexer clock	t_{MPX}		4.34		s	00,40, *MPX = 4 s*	
Multiplexer clock	t_{MPX}		8.68		s	00,80, *MPX = 8 s*	

Design-Related Data

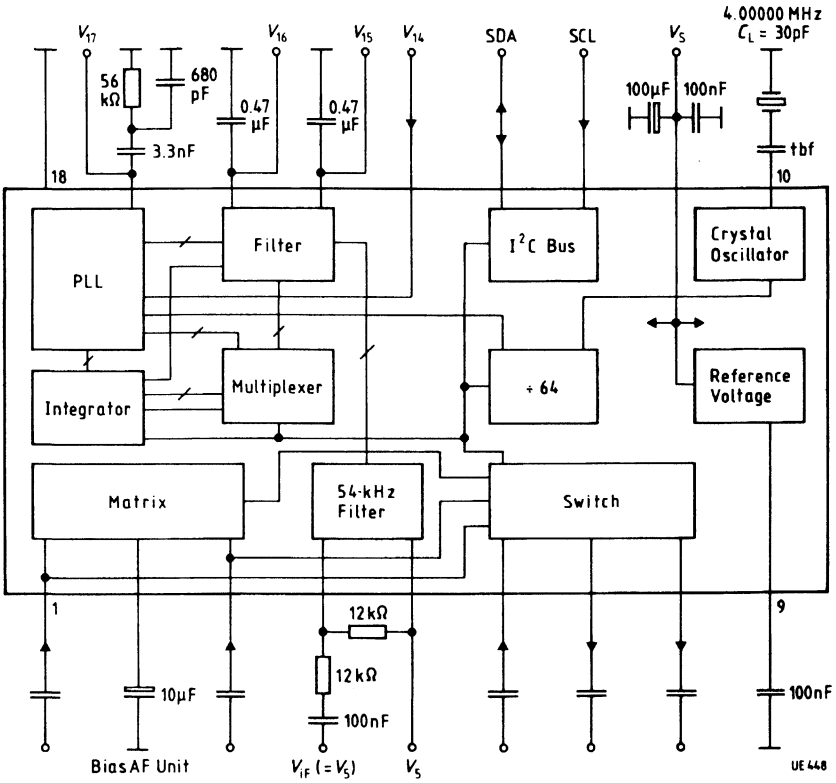
Filter output resistance	$R_{15, 16}$	110			kΩ kΩ		
f_{REF}-input resistance	R_{14}	7			kΩ		

Test Circuit 1

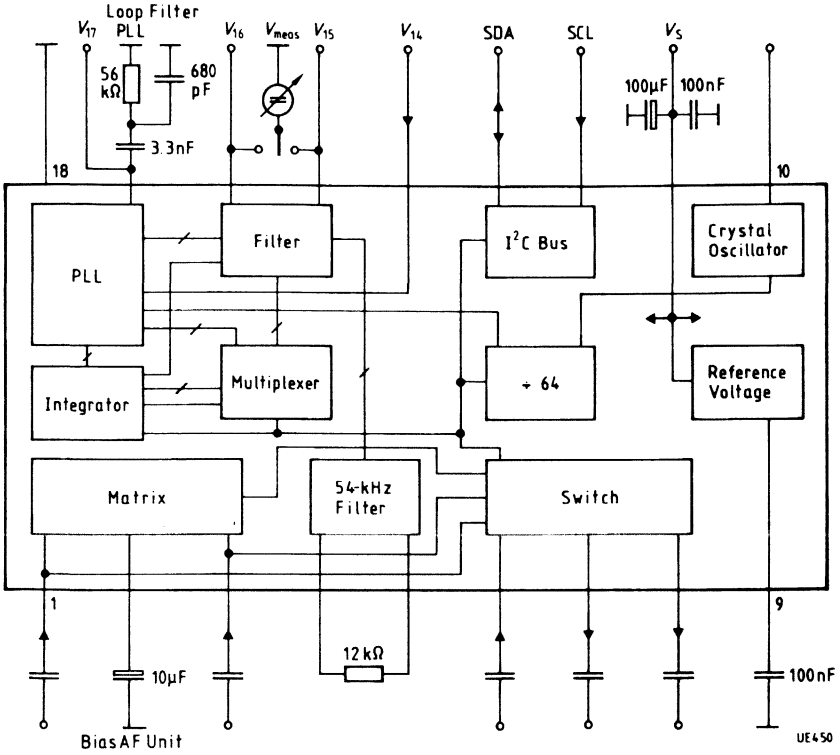


AF Generator resistance for V_1 . V_3 . V_6 . V_{IF} = 50Ω
Terminating impedance at the AF inputs for noise and crosstalk measurement = 1kΩ

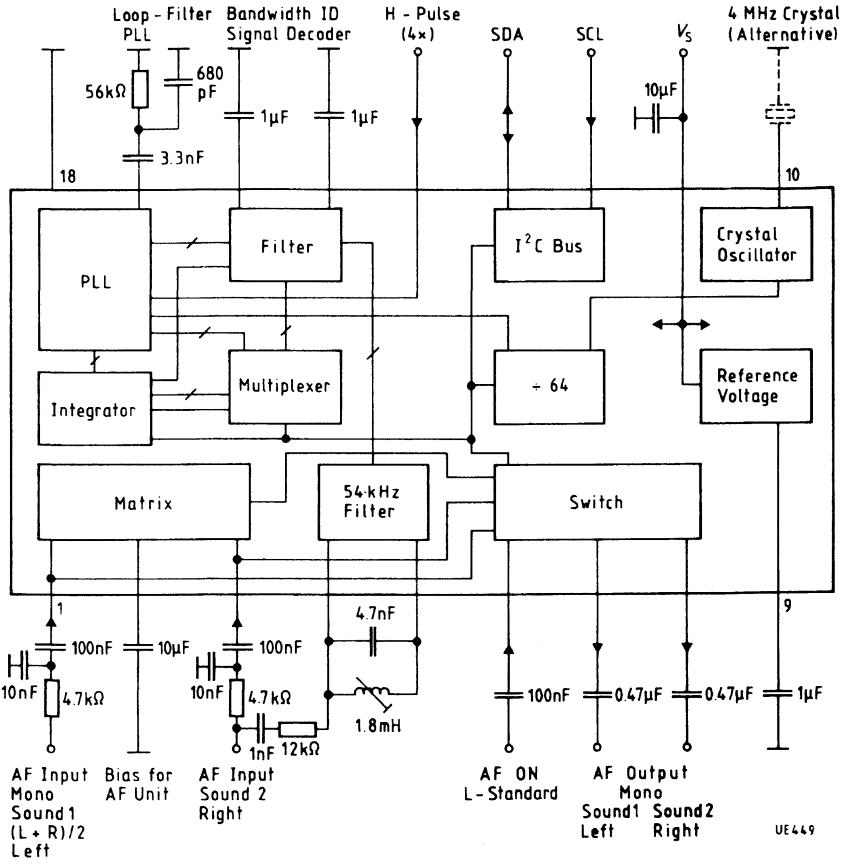
Test Circuit 2



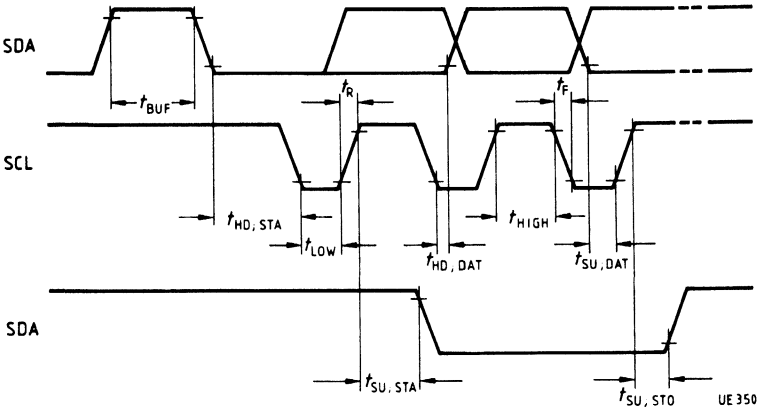
Test Circuit 3



Application Circuit



I²C Bus Time Diagram



t_{SUSTA}	Set-up time (start)
t_{HDSTA}	Hold time (Start)
t_{HIGH}	H-pulse width (Clock)
t_{LOW}	L-pulse width (Clock)
t_{SUDAT}	Set-up time (data transfer)
t_{HDDAT}	Hold time (data transfer)
t_{SUSTO}	Set-up time (Stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

All times refer to the V_{IH} and V_{IL} values

SIEMENS

FM-Tuner IC

TUA 1574

Preliminary Data

Bipolar IC

Features

- Double-balanced mixer
- AGC generation
- Strictly symmetrical RF parts
- Standby switch
- Decoupled counter output
- IF-driver

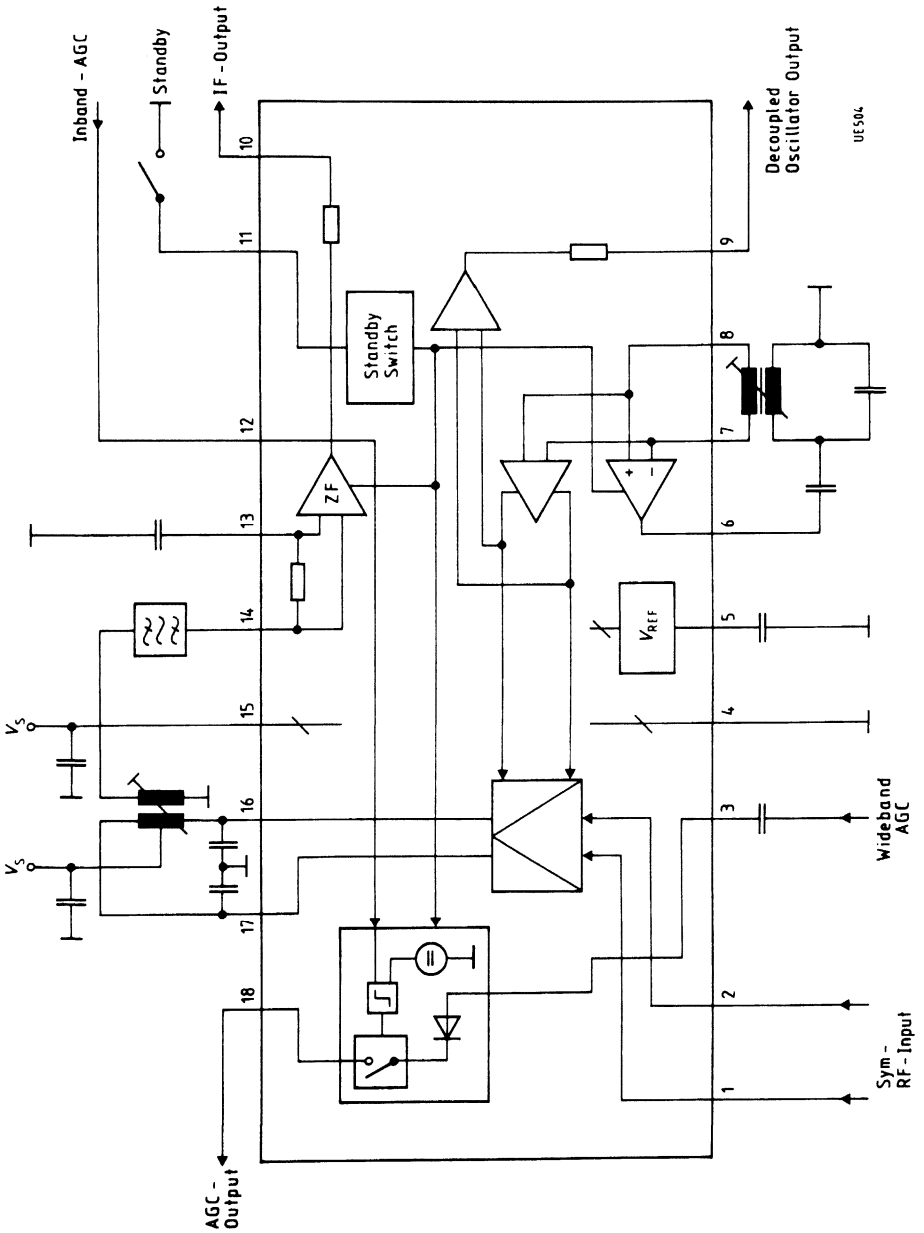
Type	Ordering Code	Package
TUA 1574	Q67000-A8101	P-DIP-18

The TUA 1574 has been designed as monolithic integrated tuner with strictly symmetrical RF parts. In addition the IC provides a pre-stage control by means of narrow and wideband information and IF post amplification.

The integrated circuit includes an oscillator with symmetrical input, buffered output and a double balanced mixer for frequency conversion. The resulting IF is post-amplified in a linear IF driver. The AGC stage integrated for pre-stage control generates combined wide and narrowband information. The IC also includes a reference voltage source and a standby switch.

The TUA 1574 is especially suitable for use in car radios and home receivers with pre-stage control and distributed IF selection.

Block Diagram



Pin Functions

Pin No.	Function
1, 2	**RF input for mixer** Low-impedance (basic circuitry) input directly to the mixer pair
3	**Input for wideband information** RF signal is present after pre-stage selection. Strong adjacent channel transmitter activates control.
4	**Ground** Decoupling should be referenced to this pin.
5	**Reference voltage** To be decoupled to pin 4.
6, 7, 8	**Oscillator** 3 point oscillator with low levels especially for tuning vector diodes.
9	**Decoupled oscillator output** Buffered output specially designed for synthesizer.
10	**Output IF driver** Output with 300 Ω corresponding to impedance of conventional IF ceramic filters.
11	**Standby-switch** The tuner is activated when this pin is tied to ground.
12	**Input for narrowband information** Field strength information of inband signal is forwarded to this pin for use in pre-stage control.
13, 14	**IF driver input** IF signal is forwarded to mixer via selection.
15	**Supply voltage** Pin should be RF decoupled against pin 4.
16, 17	**Mixer output** Symmetrical open collector output.
18	**C output** Output can be used as current output (pin diodes) or as voltage output (for bipolar and/or field effect transistors).

Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{15}	– 0.3	13.5	V
Mixer	V_{16},V_{17}	– 0.3	13.5	V
Standby- switch	V_{11}	– 0.3	V_{15}	V
Reference voltage	V_5	– 0.3	7	V

Operating Range

Supply voltage	V_{15}	7	12	V
Ambient temperature	T_A	– 25	85	°C

Characteristics
V_{15} = 8.5 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption		19	27	33	mA	$I_{15} + I_{16} + I_{17}$
Reference voltage	V_5	3.9	4.1	4.4	V	
Total gain	V_0	37	39	41	dB	V_0 = 20 lg (V_{IF}/EMF1)

Mixer

Third order intercept point	I_{P3}		115		dB/µV	random sample test
Noise figure	F		11	14	dB	
Mixer gain	V		10		dB	

Characteristics

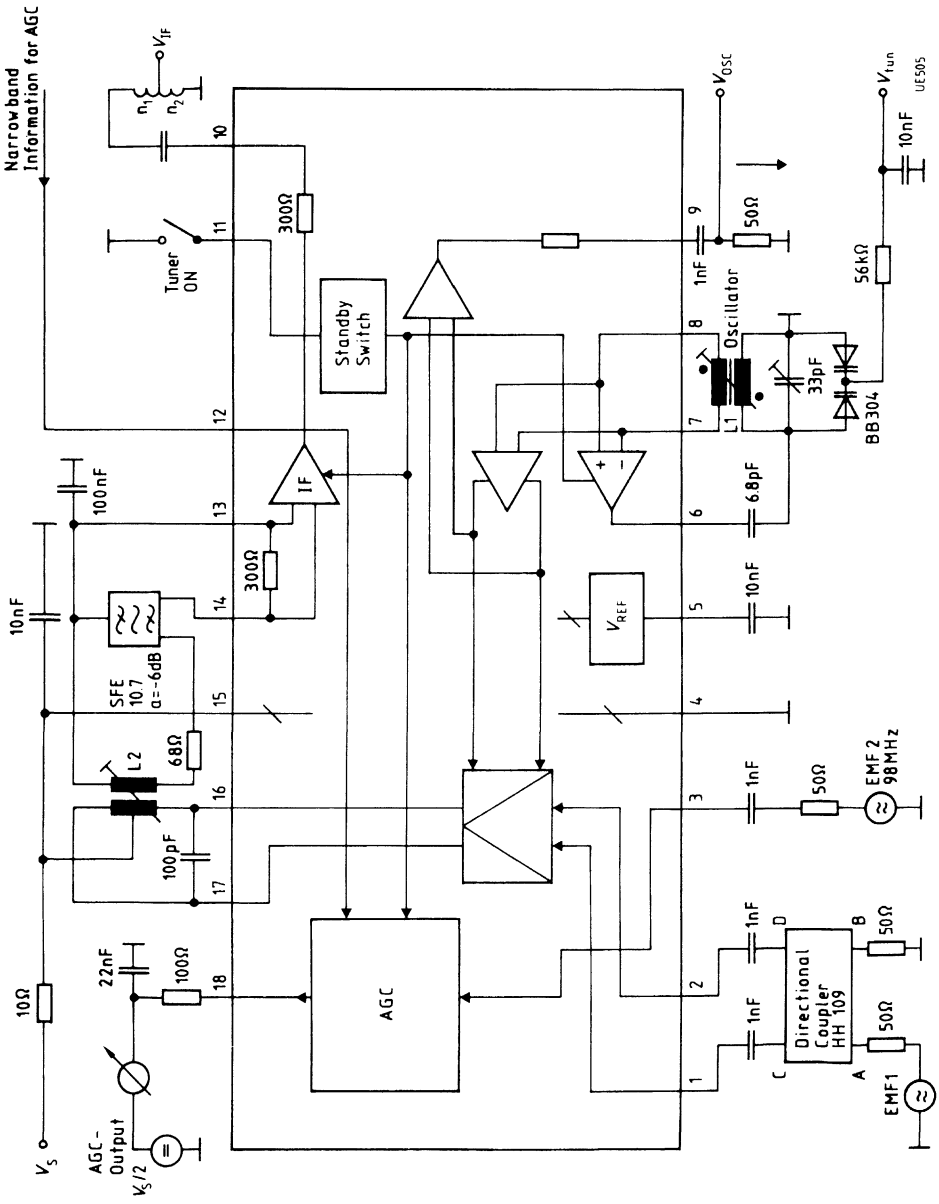
V_{15} = 8.5 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Oscillator						
DC characteristics	V_7, V_8	1.0	1.3	1.5	V	
DC characteristics	V_6	2.4	2.8	3.3	V	
Interference modulation	Δf		2.2		Hz	random sample test
Output signal 50 Ω	V_9	33	45	78	mV_{pp}	
Output impedance (ohmic)	R_9	2.0	2.5	3.0	kΩ	
Control Voltage Generation						
Control voltage	V_{18}	0.7		V_{15}-0.3	V	
Output current	$-I_{18}$	25	90	150	µA	V_3 = 0 oder V_{12} = 550 mV und $V_{18} = V_{15}/2$
Output current	I_{18}	2	3	5	mA	V_3 = 2 V und V_{12} = 1 V
Narrowband-control threshold V_3 = 2 V	V_{12}	450	500	550	mV	
Wideband control threshold	$V_{I\,HF\,EMF2}$	8	17	20	mV	V_{12} = 0.7 V $V_1 = V_{15/2}$

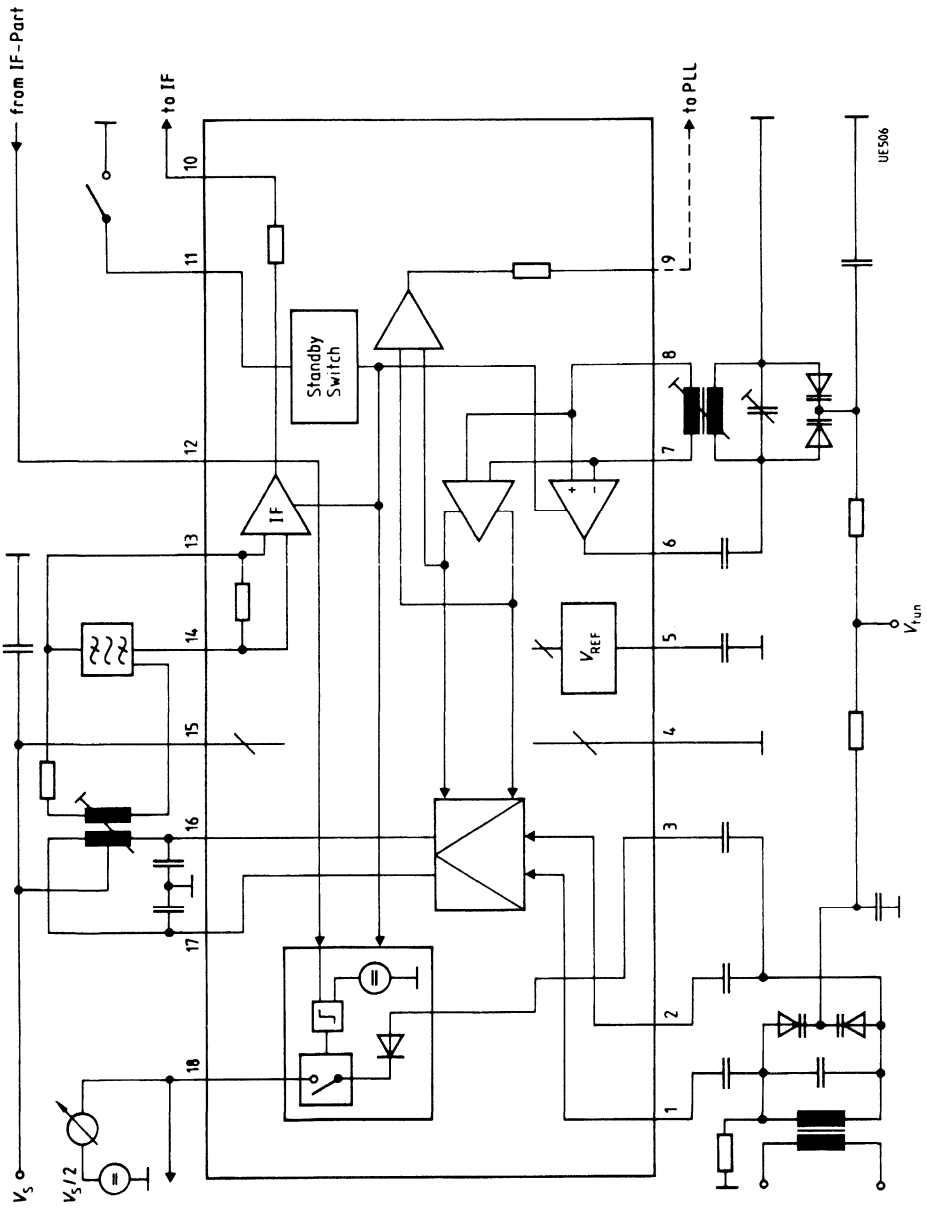
Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Linear IF Amplifier						
Input DC voltage	$V_{13, 14}$	1	1.2	1.5	V	
Output DC voltage	V_{10}	3.7	4.8	6.0	V	
Input resistance	R_{13}	240	300	360	Ω	
Input capacitance	C_{13}		13		pF	random sample test
Output impedance	R_{10}	240	300	360	Ω	
Output capacitance	C_{10}		3		pF	
Voltage gain	G_V		30		dB	$G_V = 20 \lg \frac{V_{10}}{\lvert V_{13}-V_{14}\rvert}$
Noise figure at R_S = 300 Ω	F		6.5		dB	
Standby OFF	V_{11}	3.3		V_{15}	V	

Test Circuit



Application Circuit



SIEMENS

FM-Tuner IC

TUA 1574-X6

Preliminary Data

Bipolar IC

Features

- Double-balanced mixer
- AGC generation
- Strictly symmetrical RF parts
- Decoupled counter outputs
- IF-driver

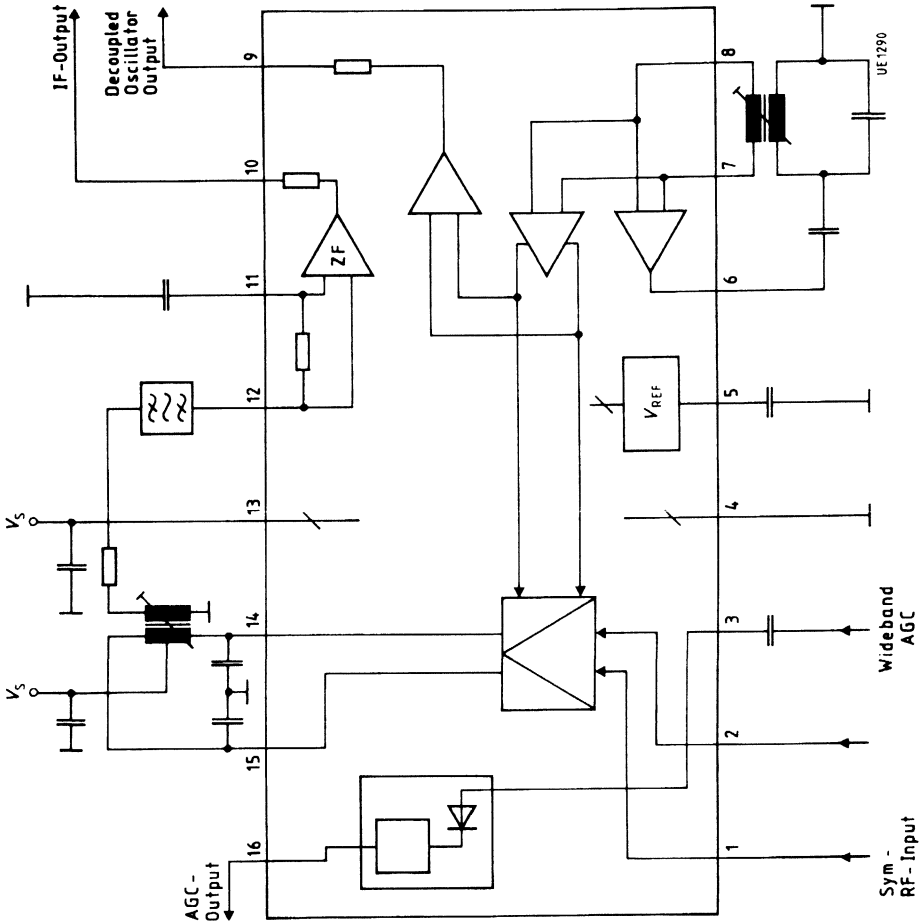
Type	Ordering Code	Package
TUA 1574-X6	Q67000-A5009	P-DSO-16 (SMD)

The TUA 1574-X6 has been designed as monolithic integrated tuner with strictly symmetrical RF parts. In addition the IC provides a pre-stage control and an IF post amplification.

The integrated circuit includes an oscillator with symmetrical input, buffered output and a double balanced mixer for frequency conversion. The resulting IF is amplified in a linear IF driver. The AGC stage integrated for pre-stage control generates wide band information. The IC also includes a reference voltage source.

The TUA 1574-X6 is especially suitable for use in car radios and home receivers with pre-stage control and distributed IF selection.

Block Diagram



Pin Functions

Pin No.	Function
1, 2	**RF Mixer input** Low-impedance (basic circuitry) input directly to the mixer pair.
3	**Input for the wide band information** RF signal is present after pre-stage selection. Strong adjacent channel transmitter activates control.
4	**Ground** Decoupling should be referenced to this pin.
5	**Reference voltage** To be decoupled to pin 4.
6, 7, 8	**Oscillator** 3 point oscillator with low levels especially for tuning vector diodes.
9	**Decoupled oscillator output** The oscillator does not affect this output.
10	**Output IF driver input** Output with 300 Ω corresponding to impedance of conventional IF ceramic filters.
11	**IF driver input** Input for the IF amplifier. This input must be blocked.
12	**IF driver input** 300 Ω input for amplifier.
13	**Supply voltage** Pin should be RF decoupled against pin 4
14, 15	**Mixer output** Symmetrical open collector output.
16	**AGC output** Output can be used as current output (pin diodes) or as voltage output (for bipolar and/or field effect transistors).

Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values		Unit
	V_{13}	min.	max.	
Supply voltage		– 0.3	13.5	V
Mixer	V_{14}, V_{15}	– 0.3	13.5	V
Reference voltage	V_5	– 0.3	7	V

Currents: all pins are short-circuit protected against ground

Operating Range

Supply voltage	V_{13}	7	12	V
Ambient temperature	T_A	– 25	85	°C

Characteristics
V_{13} = 8.5 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption (without mixer)	I_{13}	19	27	33	mA	$I_{13}+I_{14}+I_{15}$
Reference voltage	V_{REF}	3.9	4.1	4.4	V	1
Total gain	Vo	37	39	41	dB	Vo=20log(V_{IF}/EMF1)
Mixer						
Intercept point third order	I_{P3}		115		dB/µV	Random sample test
Noise figure	F		11	14	dB	
Mixer gain	V		10		dB	
Oscillator						
DC characteristics	V_7, V_8	1.0	1.3	1.5	V	
DC characteristics	V_6	2.4	2.8	3.3	V	
Interference modulation	Δf		2.2		Hz	Random sample test
Output signal 50 Ω	V_9	33	45	78	mV_{rms}	
Output impedance (resistive)	R_9	2.0	2.5	3.0	kΩ	
Control Voltage Generation						
Control voltage for pre-stage	V_{16}	0.7		V_{13}–0.3	V	
Output current V_3 = 0 and V_{16} = $V_{12/13}$	$-I_{16}$	25	90	150	µA	
Output current V_3 = 2 V	I_{16}	2	3	5	mA	

Characteristics (cont'd)
T_A = 25 °C

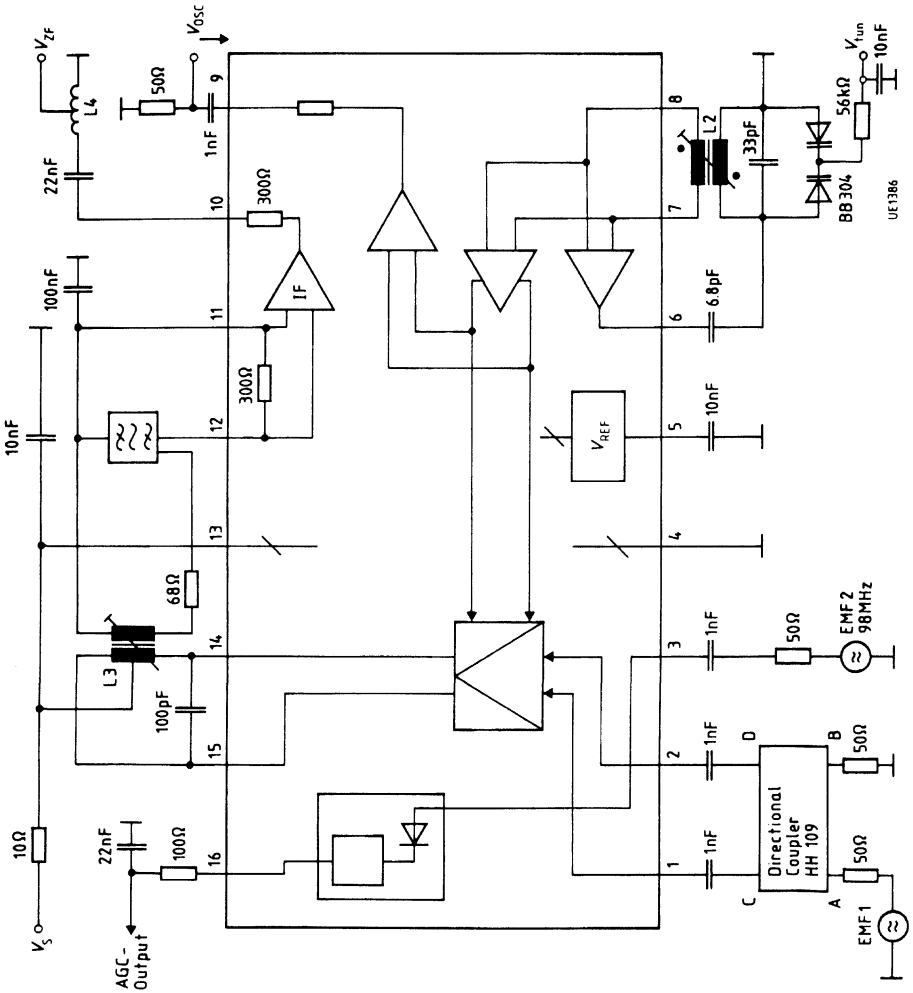
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Wideband control threshold	$V_{I\,HF\,EMF2}$	8	17	20	mV	$V_{16}=V_{12/13}$

Linear IF Amplifier

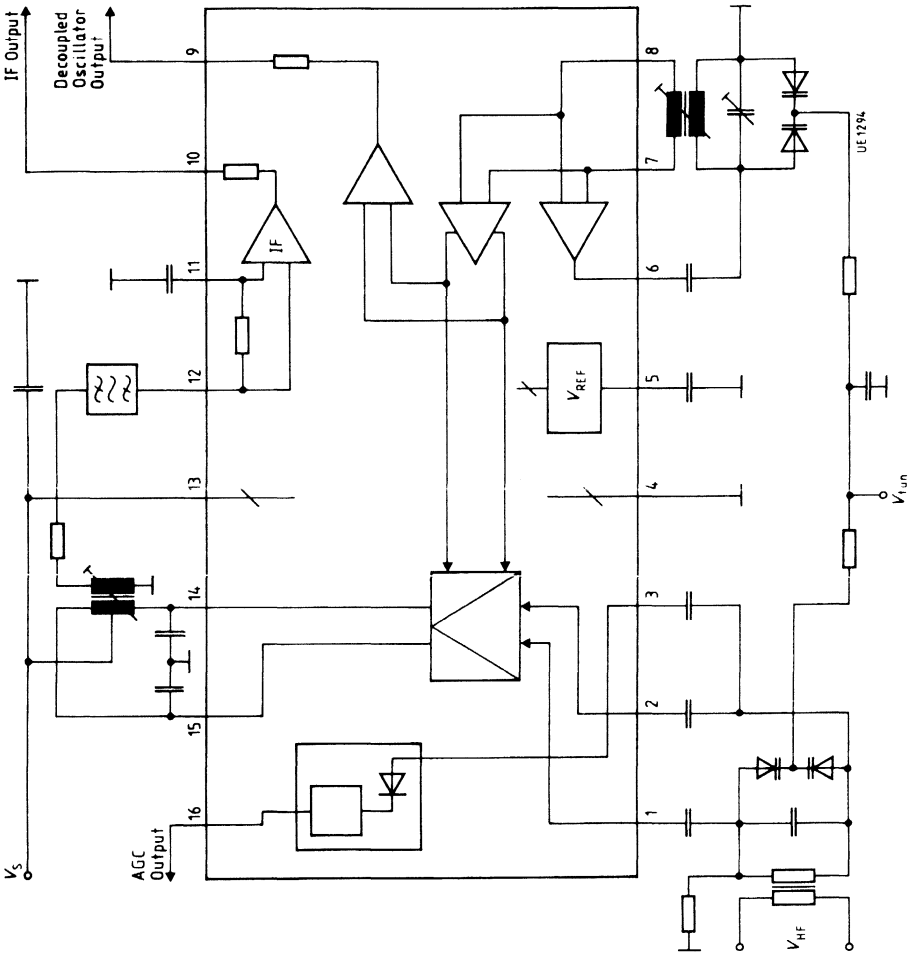
Input DC voltage	V_{11}; V_{12}	1	1.2	1.5	V	
Output DC resistance	V_{10}	1.2	4.8	6.0	V	
Input resistance	$R_{11/12}$	240	300	360	Ω	
Input capacitance	$C_{11/12}$		13		pF	Random sample test
Output resistance	R_{10}	240	300	360	Ω	" " "
Output capacitance	C_{10}		3		pF	" " "
Voltage gain	G_V		30		dB	*)
Noise figure with R_G = 300 Ω	F		6.5		dB	

*) $G_V=20\lg \frac{V_{10}}{(V_{11} - V_{12})}$

Test Circuit



Application Circuit



SIEMENS

VHF/UHF Tuner IC

TUA 2017-X

Preliminary Data

Bipolar IC

Features

- Combined UHF/Hyperband/VHF-Tuner-IC
- 3 oscillators and 3 mixers
- Only 3 frequency bands for the complete frequency range required
- Few external components
- Frequency and amplitude-stable unbalanced oscillator for the frequency range VHF.
- Frequency and amplitude-stable balanced oscillators for the frequency ranges HYPER-band and UHF.
- Optimum suppression of oscillator and input frequency at IF output
- Optimum decoupling of input frequency from oscillator
- Balanced mixer with large dynamic range and high-impedance inputs for the VHF range
- Balanced mixer with large dynamic range and low-impedance inputs for the hyperband and UHF range
- High-impedance balanced SAW driver input
- Low-impedance SAW filter output
- SAW driver with high signal-handling capability
- High decoupling of SAW driver input from output
- Internal band switch
- Low-noise, internal reference voltage

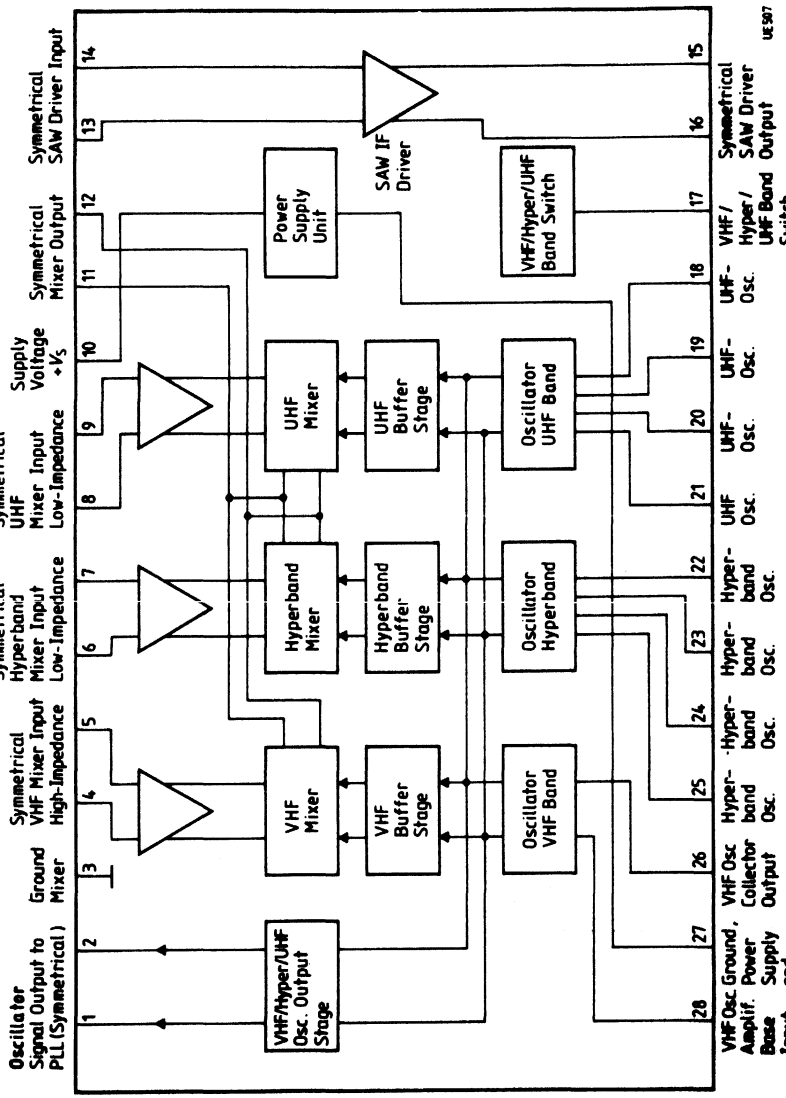
Type	Ordering Code	Package
TUA 2017-X	Q67000-A8239	P-DSO-28 (SMD)

Circuit Description

This integrated circuit permits the design of TV tuners covering the entire frequency range from 48...860 MHz with a division into 3 bands. The application is suitable for all tuners in TV- and VCR-sets.

The IC includes 3 balanced mixers (double push-pull mixer/ring mixer), one unbalanced oscillator for VHF and two balanced oscillators for HYPER and UHF, a SAW driver as well as a reference voltage source and a band switch. A frequency separating filter at the tuner input assigns the TV signal to one of the three bands. The band switch ensures that only one band at a time is activated. In the activated band the signal passes a frontend stage with MOSFET amplifier, a double-tuner bandpass filter and is then fed to the activated balanced mixer input of the TUA 2017, which is a high-impedance stage for the VHF range and a low-impedance stage for the hyperband and UHF range, respectively. The signal is mixed there with the oscillator signal from the activated oscillator section and fed to a common IF stage for all bands. After passing the IF intermediate circuit filter the IF signal is amplified further by a SAW driver section to drive the low-impedance SAW filter.

Block Diagram



Pin Definitions and Functions

Pin No.	Function	Definition
1	Osc. output 1	VHF/HYPER/UHF oscillator signal output to PLL, symmetrical to pin 2
2	Osc. output 2	VHF/HYPER/UHF oscillator. signal output to PLL, symmetrical to pin 1
3	GND mixer	Ground mixer inputs
4	VHF input 1	VHF mixer input high-impedance, symmetrical to pin 5
5	VHF input 2	VHF mixer input high-impedance, symmetrical to pin 4
6	Hyper input 1	Hyper mixer input low-impedance, symmetrical to pin 7
7	Hyper input 2	Hyper mixer input low-impedance, symmetrical to pin 6
8	UHF input 1	UHF mixer input low-impedance, symmetrical to pin 9
9	UFH input 2	UHF mixer input low-impedance, symmetrical to pin 8
10	$+Vs$	Supply voltage
11	Mi. output 1	Open collector mixer output, high-impedance, symmetrical to pin 12
12	Mi. output 2	Open collector mixer output, high-impedance, symmetrical to pin 11
13	OFW driver input 1	SAW driver amplifier input, symmetrical to pin 14
14	OFW driver input 2	SAW driver amplifier input, symmetrical to pin 13
15	OFW driver output 1	SAW driver amplifier output, low-impedance, symmetrical to pin 16
16	OFW driver output 2	SAW driver amplifier output, low-impedance, symmetrical to pin 15
17	Band switching	VHF / HYPER / UHF band switching
18	UHF osc. input 1	UHF oscillator amplifier, high-impedance base input, symmetrical to pin 21
19	UHF osc. output 1	UHF oscillator amplifier, high-impedance collector output, symmetrical to pin 20
20	UHF osc. input 2	UHF oscillator amplifier, high-impedance collector output, symmetrical to pin 19
21	UHF osc. input 2	UHF oscillator amplifier, high-impedance base input, symmetrical to pin 18
22	Hyp. osc. input 1	Hyp. oscillator amplfier, high-impedance base input, symmetrical to pin 25
23	Hyp. osc. output 1	Hyp.-oscillator amplifier, high-impedance collector output, symmetrical to pin 24
24	Hyp. osc. output 2	Hyp. oscillator amplifier, high-impedance collector output, symmetrical to pin 23
25	Hyp. osc. input 2	Hyp. oscillator amplifier, high-impedance base input, symmetrical to pin 22
26	VHF osc. coupl. 1	VHF oscillator coupling , collector output
27	GND	Ground SAW driver, power supply unit, band switch and oscillators
28	VHF osc. coupl. 2	VHF oscillator coupling, base input

Absolute Maximum Ratings
T_A = 25 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage V_S	$V_{10,11,12,27,3}$	– 0.3	14	V	
Current	$I_{10,11,12}$		60	mA	
Switching voltage	V_{17}	– 0.3	+ V_S	V	

Only the considered external circuitry, conform to the measurement circuit 1,
can be applied at the pins1,3,4,5,6,7,8,9,10,11,13,14,15,16,20,21,22,23,24,25,27,28

Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	– 40	125	°C	
Thermal resistance (system air)	$R_{th\ SA}$			K/W	typ. value 75

Operational Range

Supply voltage	V_S	10	13.2	V	
Current consumption	$I_{10,11,12}$	25	53	mA	
VHF mixer input frequency range	f_{VHF}	30	500	MHz	
HYPER mixer input frequency range	f_{HYPER}	30	900	MHz	
UHF mixer input frequency range	f_{VHF}	30	900	MHz	
VHF oscillator-frequency range	f_{OVHF}	30	500	MHz	
HYPER oscillator-frequency range	f_{OHYPER}	30	900	MHz	
UHF oscillator-frequency range	f_{OUHF}	30	900	MHz	
Ambient temperature	T_A	0	70	°C	

Characteristics

V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Current consumption	I_{10}	25	34	43	mA	$V_{11,12} = V_S$; $V_{17} > 1.6$ V	1
Current consumption	I_{10}	19	28	37	mA	$V_{11,12} = V_S$; $V_{17} < 0.9$ V	1
Current consumption	$I_{11/12}$	5	8	11	mA	$V_{11,12} = V_S$	1
VHF Circuit Section							
Switching voltage	V_{17}	0		1	V		1
Switching current	I_{17}			10	µA	V_{17} = 0.5V	1
Oscillator frequency range	f_{VHF}	80		216	MHz	Vd = 0...28 V	1
Oscillator drift	Δf_{VHF}			200	kHz	V_S = 12 V ± 10%	1
Oscillator drift	Δf_{VHF}			400	kHz	ΔT = 25 °C	1
Oscillator drift	Δf_{VHF}			200	kHz	t = 5 sec. to 15 min. after switching on	1
Oscillator level	$V_{1,2}$		700		mV_{rms}	K2 at hot end	1
Oscillator level	$V_{1,2}$		700		mV_{rms}	S10 at hot end	1
Oscillator Output impedance	$R_{1,2}$		100		Ω	parallel	2
	$C_{1,2}$		2		pF	equivalent circuit	
Harmonic ratio	$a_{1,2}$			– 10	dB		1
Interference ratio	$a_{1,2}$			– 10	dB	V_{HF} = 1 Vrms	1
Oscillator pulling	$V_{4,5}$	100	108		dB/µV	Δf=10 kHz in channel K2	1
Oscillator pulling	$V_{4,5}$	100	108		dB/µV	Δf=10 kHz in channel S10	1
Oscillator pulling	$V_{4,5}$	80	88		dB/µV	Δf_{int} = K2 + (N + 5 – 1M Hz)	1
Oscillator pulling	$V_{4,5}$	80	88		dB/µV	Δf_{int} = S10 + (N + 5 – 1 MHz)	1
Mixer gain	G_{VHF}		5		dB	channel 2	1
Mixer gain	G_{VHF}		5		dB	channel S10	1
Mixer noise figure	NF_{VHF}		7.5	9	dB	channel 2	1
Mixer noise figure	NF_{VHF}		7.5	9	dB	channel S10	1
Interference voltage	V_{int}		70		dB/µV	1% cross mod.; K2 ± 2	1
Interference voltage	V_{int}		70		dB/µV	1% cross mod.; S10 ± 2	1
Mixer input impedance	$R_{4,5}$		1		kΩ	parallel	3
	$C_{4,5}$		2		pF	equivalent circuit	
Mixer output impedance	$R_{11,12}$		10		kΩ	parallel	4
	$C_{11,12}$		2		pF	equivalent circuit	
IF-suppression	a_{IF}		20		dB	channel 2	1
IF-suppression	a_{IF}		20		dB	channel S10	1

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Hyper Circuit Section							
Switching voltage	V_{17}	1.6		2.3	V		1
Switching current	I_{17}		10	30	µA	V_{17} = 2.1 V	1
Oscillator frequency range	f_{HYPER}	190		485	MHz	Vd = 0...28 V	1
Oscillator drift	Δf_{HYPER}			400	kHz	V_S = 12 V ± 10 %	1
Oscillator drift	Δf_{HYPER}			500	kHz	ΔT = 25 °C	1
Oscillator drift	Δf_{HYPER}			200	kHz	t = 5 sec. to 15 min. after switching on	1
Oscillator level	$V_{1,2}$		100		mV_{rms}	K5 symmetrical tested	1
Oscillator level	$V_{1,2}$		80		mV_{rms}	S37 symmetrical tested	1
Oscillator	$R_{1,2}$		100		Ω	parallel	2
Output impedance	$C_{1,2}$		2		pF	equivalent circuit	
Harmonic ratio	$a_{1,2}$			– 10	dB		1
Interference ratio	$a_{1,2}$			– 10	dB	V_{HF} = 1 V_{rms}	1
Oscillator pulling	$V_{6,7}$	100	108		dB/µV	Δf=10 kHz in channel K5	1
Oscillator pulling	$V_{6,7}$	100	108		dB/µV	Δf=10 kHz in channel S37	1
Oscillator pulling	$V_{6,7}$	80	88		dB/µV	Δf_{int} = K5 + (N + 5 – 1 MHz)	1
Oscillator pulling	$V_{6,7}$	80	88		dB/µV	Δf_{int} – S37 + (N + 5 – 1 MHz)	1
Mixer gain	G_{HYPER}		5		dB	channel 5	1
Mixer gain	G_{HYPER}		5		dB	channel S37	1
Mixer noise figure	NF_{HYPER}		7.5	9	dB	channel 5	1
Mixer noise figure	NF_{HYPER}		7.5	9	dB	channel S37	1
Interference voltage	V_{int}	97	100		dB/µV	1% cross mod.; K5 ± 2	1
Interference voltage	V_{int}	97	100		dB/µV	1% cross mod.; S37 ± 2	1
Mixer input	$R_{6,7}$		125		Ω	serial equivalent circuit	3
impedance	$C_{6,7}$		10		nH		
Mixer output	$R_{11,12}$		10		kΩ	parallel	4
impedance	$C_{11,12}$		2		pF	equivalent circuit	
IF-suppression	a_{IF}		20		dB	channel 5	1
IF-suppresion	a_{IF}		20		dB	channel S37	1

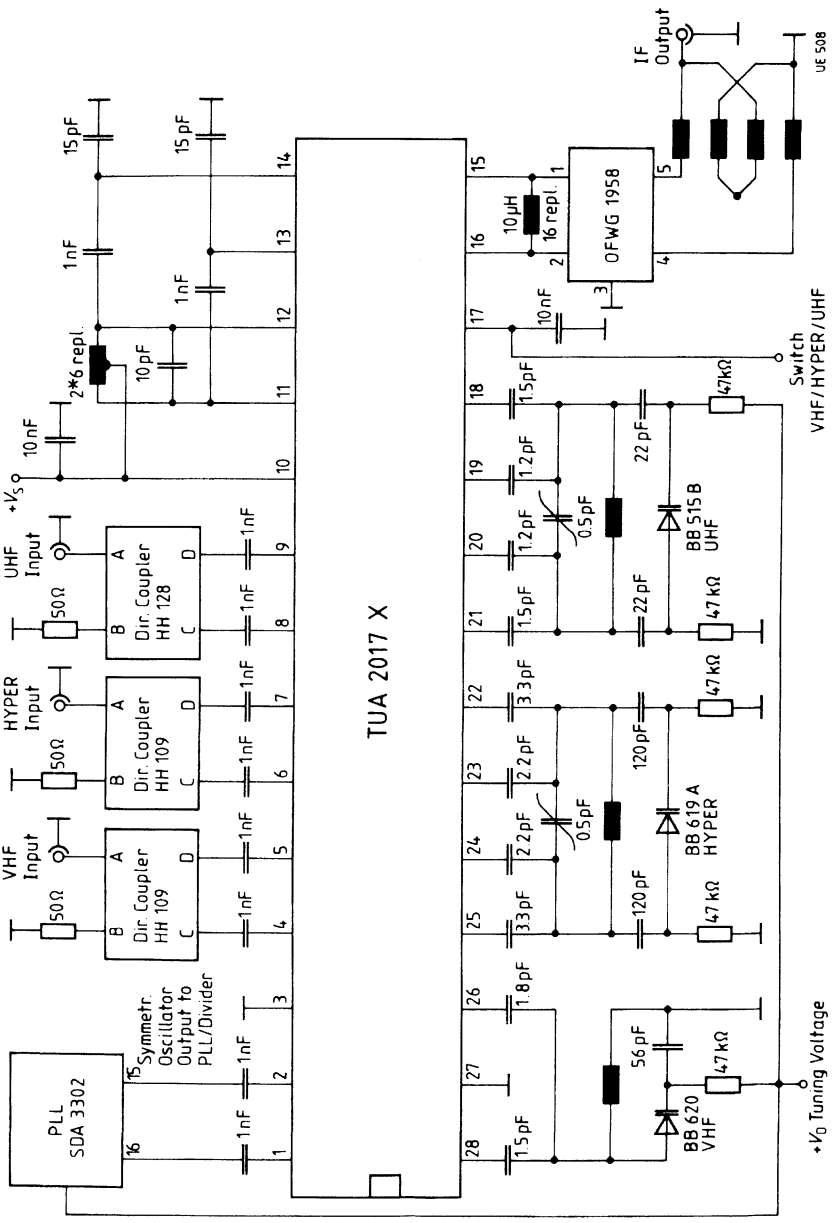
Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
UHF-Circuit Section							
Switching voltage	V_{17}	3.2		≤ V_S	V		1
Switching current	I_{17}		60	300	µA	$V_{17} = V_S$	1
Oscillator frequency range	f_{VHF}	470		900	MHz	Vd = 0...28 V	1
Oscillator drift	Δf_{UHF}			400	kHz	V_S = 12 V ± 10%	1
Oscillator drift	Δf_{UHF}			800	kHz	ΔT = 25 °C	1
Oscillator drift	Δf_{UHF}			200	kHz	t = 5 sec. to 15 min. after switching on	1
Oscillator level	$V_{1,2}$		80		mV_{rms}	K21 symmetrical tested	1
Oscillator level	$V_{1,2}$		50		mV_{rms}	K68 symmetrical tested	1
Oscillator	$R_{1,2}$		100		Ω	parallel	2
Output impedance	$C_{1,2}$		2		pF	equivalent circuit	
Harmonic ratio	$a_{1,2}$			– 10	dB		1
Interference ratio	$a_{1,2}$			– 10	dB	V_{HF} = 1 V_{rms}	1
Oscillator pulling	$V_{8,9}$	100	108		dBµV	Δf=10 kHz in channel K21	1
Oscillator pulling	$V_{8,9}$	100	108		dBµV	Δf=10 kHz in channel K68	1
Oscillator pulling	$V_{8,9}$	80	88		dBµV	Δf_{int} = K21 +(N+5–1 MHz)	1
Oscillator pulling	$V_{8,9}$	80	88		dBµV	Δf_{int} = K68 +(N+5–1 MHz)	1
Mixer gain	G_{UHF}		5		dB	channel 21	1
Mixer gain	G_{UHF}		5		dB	channel K68	1
Mixer noise figure	NF_{UHF}		8	10	dB	channel 21	1
Mixer noise figure	NF_{UHF}		9	11	dB	channel K68	1
Interference voltage	V_{int}	97	100		dB/µV	1% cross mod.; K21 ± 2	1
Interference voltage	V_{int}	97	100		dB/µV	1% cross mod.; K68 ± 2	1
Mixer input	$R_{8,9}$		125		Ω	serial equivalent circuit	3
impedance	$C_{8,9}$		10		nH		
Mixer output	$R_{11,12}$		10		kΩ	parallel	4
impedance	$C_{11,12}$		2		pF	equivalent circuit	
IF-suppression	a_{IF}		20		dB	channel 21	1
IF-suppression	a_{IF}		20		dB	channel 68	1

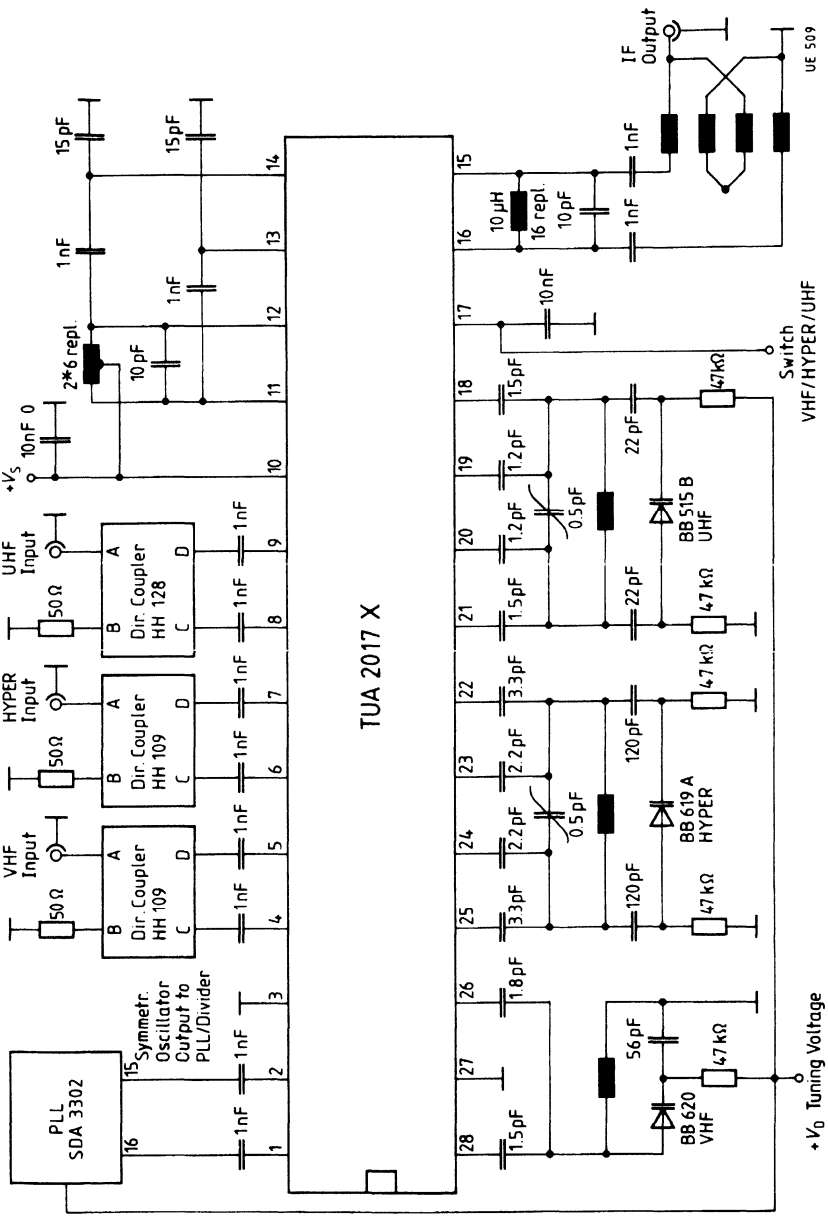
Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
SAW-Driver Section							
SAW driver Input impedance	$R_{13,14}$ $C_{13,14}$		300 2.5		Ω pF	parallel equivalent circuit	5
SAW driver Output impedance	$R_{15,16}$ $C_{15,16}$		100 2.5		Ω pF	parallel equivalent circuit	6
Transmission gain	G_{SD}		16		dB		8
Noise figure	NF_{SD}		10		dB		8
Output voltage linearity	V_{SDO}		26		dBm	total harmonic distortion factor THD = 5%	7
Permissible input voltage	V_{SDI}		3		dBm	for 1 dB compression at the output	7

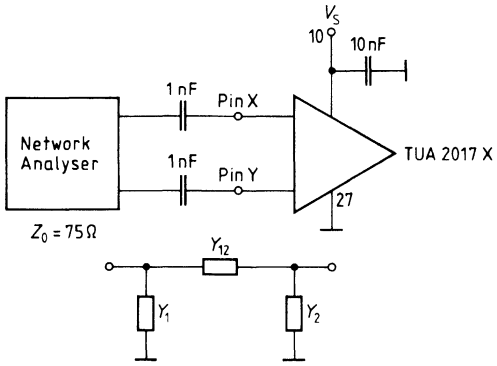
Test Circuit 1



Test Circuit 2



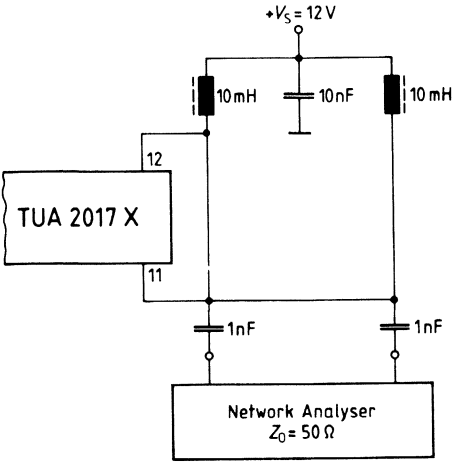
Test Circuit 3



Measurement of the 4-pole matrix S_{11}, S_{12}, S_{21}, S_{22} and calculation of the π-equivalent circuit, which follows from that.

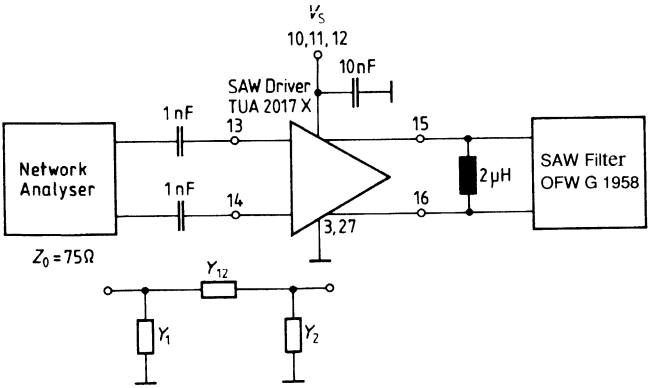
Test Point	Test Frequency in MHz	Pin x	Pin y
Oscillator output impedance	100	1	2
Mixer input impedance VHF	100	4	5
Mixer input impedance HYPER	300	6	7
Mixer input impedance UHF	600	8	9

Test Circuit 4



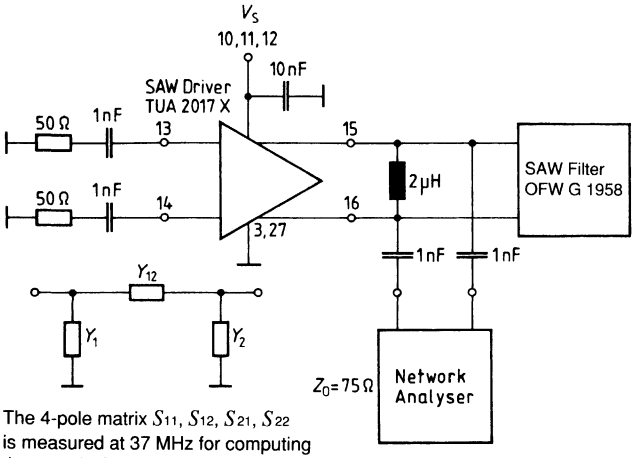
The output capacitance is computed by measuring the 4-pole matrix S_{11}, S_{12}, S_{21}, S_{22} at 37 MHz

Test Circuit 5



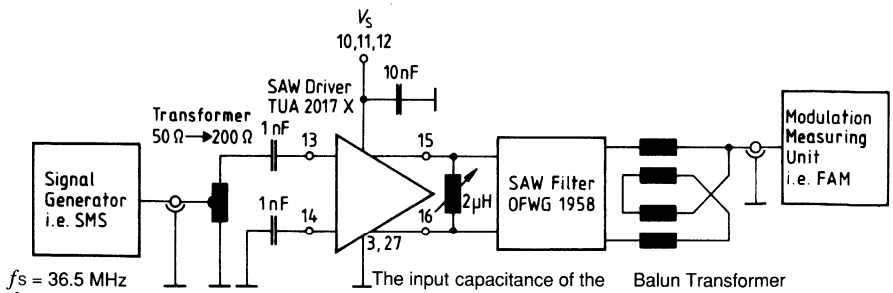
The 4-pole matrix S_{11}, S_{12}, S_{21}, S_{22} is measured at 37 MHz for computing the π-equivalent circuit

Test Circuit 6



The 4-pole matrix S_{11}, S_{12}, S_{21}, S_{22} is measured at 37 MHz for computing the π-equivalent circuit

Test Circuit 7

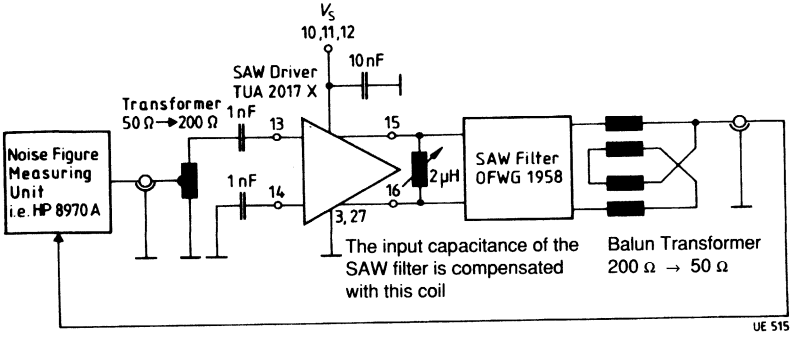


f_S = 36.5 MHz
f_T = 1 kHz
m_S = 80 %
$THD \leq 0.4$ %
R_a= 50 Ω

The input capacitance of the SAW filter is compensated with this coil

Balun Transformer
200 Ω → 50 Ω

Test Circuit 8



LED Driver for Light Spot Displays

UAA 170

Bipolar IC

IC for driving 16 light emitting diodes. Depending on the input voltage, the individual LEDs are driven within one row in form of a light spot. The UAA 170 provides a linear relation between control voltage and the driven LED.

By using an appropriate circuitry, the brightness of the LEDs can be varied and the crossing over of the light spot can be set between "smooth" and "abrupt". By connecting two ICs in parallel, up to 30 LEDs can be driven.

Type	Ordering Code	Package
UAA 170	Q67000-A940	P-DIP-16

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	18	V
Input voltages	V_{11}, V_{12}, V_{13}	6	V
Load current	I_{14}	5	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating Range

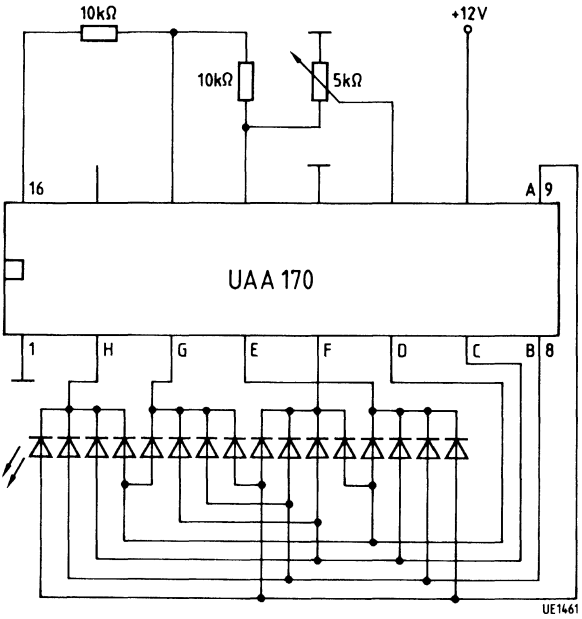
Supply voltage (LED red)[1]	V_S	11 to 18	V
Ambient temperature	T_A	– 25 to 85	°C

1) The lower limit only applies to an LED forward voltage of approx. 1.5 V (red LEDs); the lower limit increases with higher forward voltage

Characteristics
V_S = 12 V; T_A = 25°C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption (I_{14} = 0; I_{16} = 0)	I_S	2	4	10	mA
Control input current	I_{11}	– 2			µA
Reference input current	I_{12}, I_{13}	– 2			µA
Voltage difference	$\Delta V_{12/13}$	1.4		6.0	V
Voltage difference for smooth light transition	$\Delta V_{12/13}$	1.4			V
Voltage difference for abrupt light transition	$\Delta V_{12/13}$	4			V
Voltage difference	$\Delta V_{12/13}$	4			V
Stabilized voltage I_{14} = 300 µA I_{14} = 5 mA	V_{14} V_{14}	 4.5	5.0	6.0	V V
Reference input voltage	$V_{REF\ max}$ $V_{REF\ min}$	1.4 0		6.0 4.6	V V
Tolerance of forward voltages of LEDs, mutually	ΔV_D			0.5	V
Output current for LEDs	ΣI_D		25		mA

Measurement Circuit



Scale Display with Light Emitting Diodes

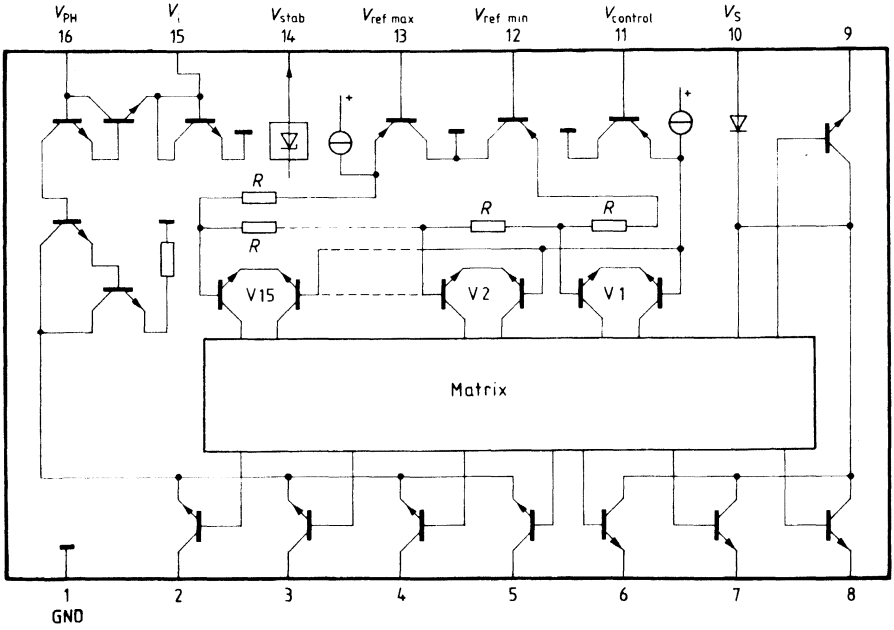
Scale displays by means of a wandering light spot are particularly suitable for indicating approximate values. Applications of this kind are level sensors, VU-meters, tachometers, radio scales etc. When applying the displays in measuring equipment, multicolored light emitting diodes can be used as range limitation. Ring scales are obtained by a circular arrangement of the diodes. The IC UAA 170 has been especially developped for driving a scale of 16 LEDs.

The input voltages at pins 11, 12 and 13 are freely selectable between 0 and 6 V. Any kind of adjustment becomes possible by suitable voltage drivers. The DC value $V_{control}$ is always assigned to a certain spot of the diode chain.

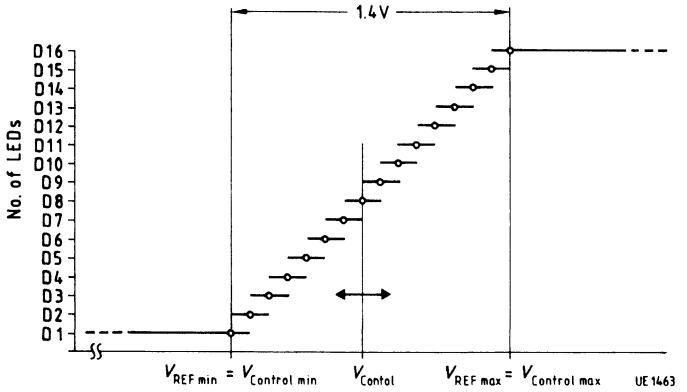
The voltage difference between pins 12 and 13 thereby corresponds to the possible indication range. $\Delta V_{12\,/\,13}$ defines at the same time the light transition between two diodes. With $\Delta V_{12\,/\,13}$ approx. 1.4 V, the light point glides smoothly along the scale. With increasing voltage difference, the passage becomes more abrupt. With $\Delta V_{12\,/\,13}$ approx. 4 V, the light point jumps from diode to diode.

Input voltages beyond the selected indication range cause the diodes D1 or D16 respectively, to light up, identifying only that the range has been exceeded.

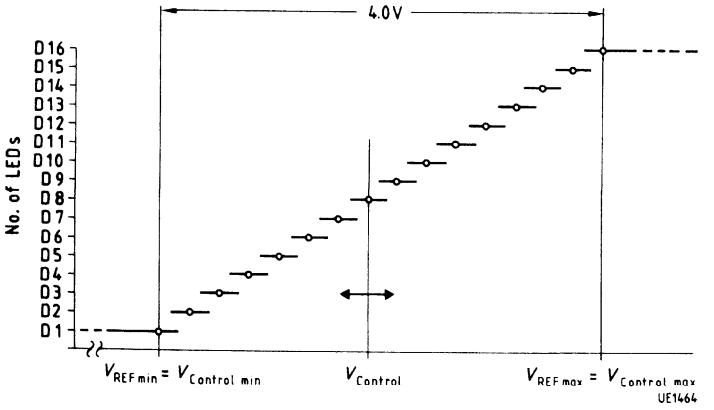
Block Diagram



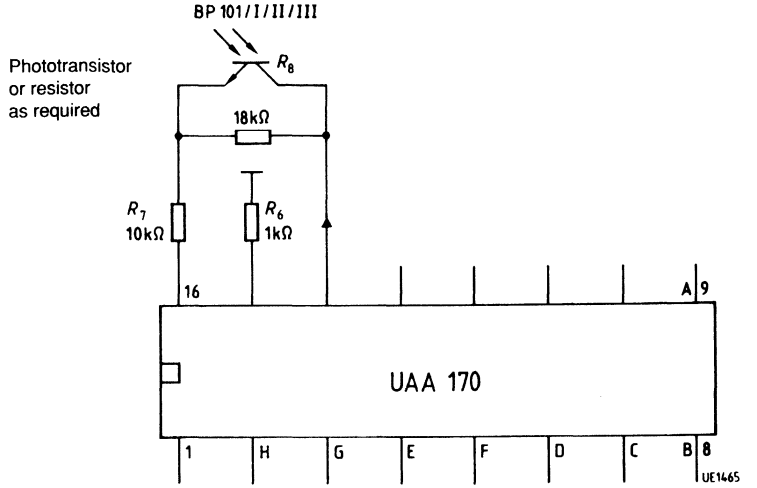
Display with smooth transition UAA 170



Display with abrupt transition UAA 170



Brightness Control

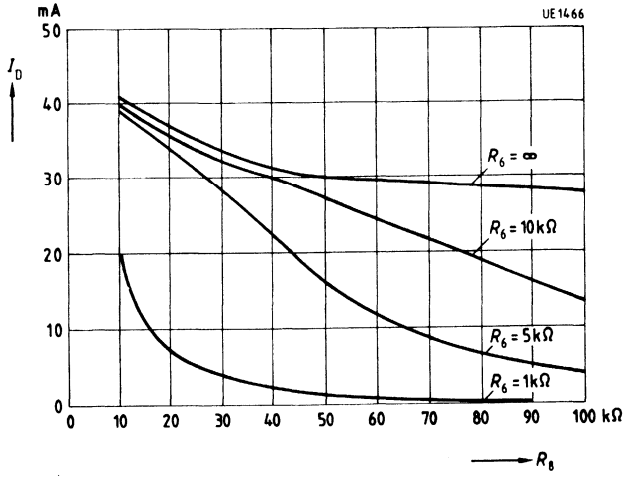


Pins 14, 15, and 16 serve to determine the diode current. Corresponding to the desired light intensity, the forward current of the diodes is linearly variable in the range I_f approx. 0 to 50 mA. The resistance at pin 15 defines the adjusting range. The resistances between pin 14 and 16 determine the current.

With the aid of a phototransistor, such as BP 101, the light intensity of the LEDs can be adjusted to the light fluctuations of the environment.

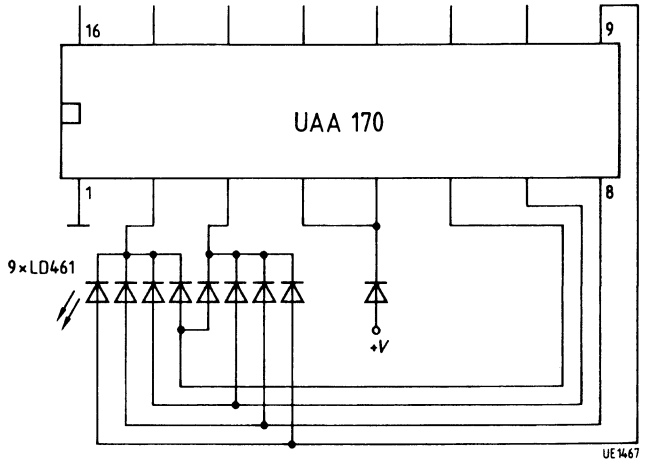
Diode current versus base emitter resistance

V_S = 12 V; T_A = 25 °C; V_{14} = 5.4 V; red LEDs

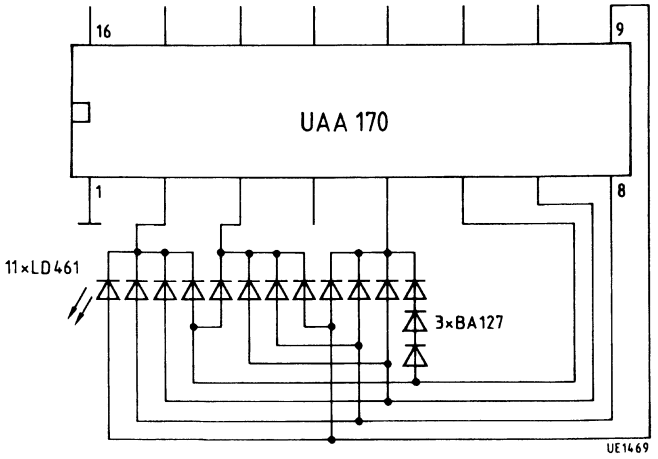


Operation of less than 16 LEDs

Control of 9 LEDs

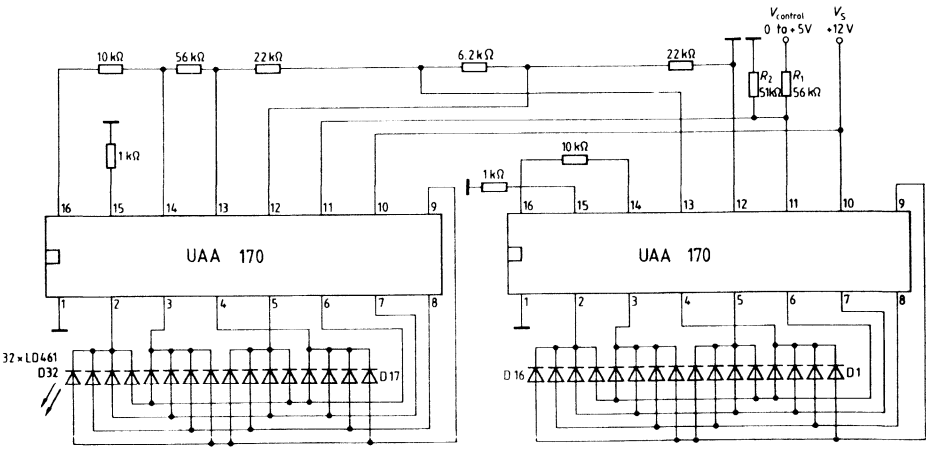


Control of 11 LEDs



Application Circuit for the Control of 30 LEDs with 2 × UAA 170

Range of control voltage $V_{control}$ = 0 to 5 V
Voltage difference $V_{12/13}$ = 2 × 1.2 V = 2.4 V
Since the diodes D16 or D17 are permanently lit when the maximum or minimum voltages V_{13} or V_{12} adjusted by R_3, R_4, R_5, are exceeded or fall short, the diodes should be covered, if necessary.



The figure shows an expansion of the circuit to 30 diodes with 2 ICs UAA 170. The diodes D16 or D17 are permanently lit when the reciprocal absolute ratings are exceeded. They should be covered. The reference voltage $\Delta V_{12/13}$ 2 × 1.2 = 2.4 V is derived from a stabilized DC voltage of typ. 5 V available at pin 14. A resistance of 6.2 kΩ provides an overlapping of the ranges in order to ensure a smooth transition from D15 to D18. The control voltage $V_{control}$ is forwarded in a parallel mode to pins 11 via a divider R_1 : R_2. The voltage divider is to be dimensioned according to the desired input voltage. With a divider current of I = 100 µA and a control voltage of $V_{control}$ = 10 V, the following is valid:

$$R_2 = \frac{\Delta V_{12/13}}{I} = \frac{2.4}{0.1} = 24\ \text{k}\Omega \text{ and}$$

$$R_1 = \frac{V_{control} - \Delta V_{12/13}}{I} = \frac{7.6}{0.1} = 76\ \text{k}\Omega$$

The nearest standard value is R_1 = 75 kΩ. The voltage difference for switching an incremental

step is then $\Delta V_{control} = \frac{10\ \text{V}}{30} = 0.16\ \text{V}$.

SIEMENS

LED Driver for Light Band Displays

UAA 180

Bipolar IC

Integrated circuit for driving 12 light emitting diodes. Corresponding to the input voltage, LEDs forming a light band are controlled similar to a thermometer scale.

By using an appropriate circuitry the brightness of the LEDs can be varied and the light passage between two adjacent LEDs can be set between "smooth" and "abrupt".

Type	Ordering Code	Package
UAA 180	Q67000-A1104	P-DIP-18

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	18	V
Input voltage	V_3 V_{16} V_{17}	6 6 6	V V V
Storage temperature range	T_{stg}	– 40 to 125	°C
Junction temperature	T_j	150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	78	K/W

Operating Range

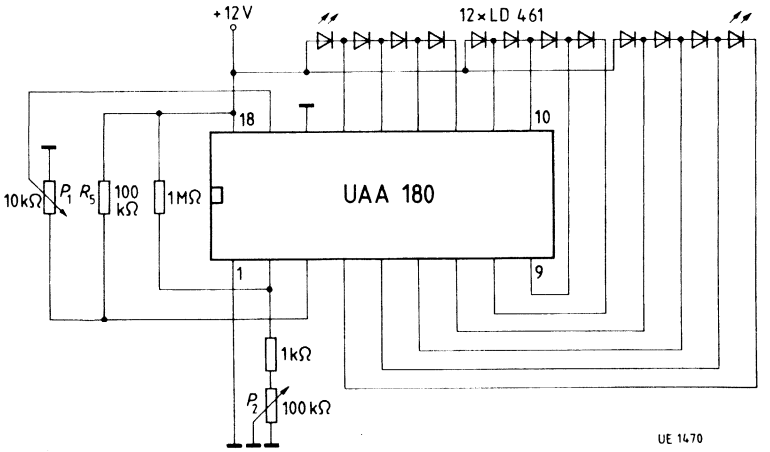
Supply voltage	V_S	10 to 18	V
Ambient temperature	T_A	– 25 to 85	°C

Characteristics

V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption (I_2 = 0) (without LED current)	I_{18}		5.5	8.2	mA
Input currents $V_3 - V_{16} < 2$ V	I_3 I_{16} I_{17}		0.3 0.3 0.3	1 1 1	µA µA µA
Voltage difference for smooth light transition	$\Delta V_{16/3}$	1.0			V
Voltage difference for abrupt light transition	$\Delta V_{16/3}$	4.0			V
Diode current per diode	I_D		10		mA
Tolerance of LED forward voltages	ΔV_D			1.0	V

Measurement Circuit



P 1 Light Band Test
P 2 Brightness Test

Scale Display with Light Emitting Diodes

Scale displays by means of a growing light band are particularly suitable for the measuring of approximate values. Applications of this kind are level sensors, VU meters, tachometers, field strength indicators etc. When applying the displays in measuring equipment, multicolored LEDs can be used as range limitation.

The voltage difference between pins 16 and 3 thereby corresponds to the possible indication range. $\Delta V_{16/3}$ defines at the same time the light passage between two diodes. With $\Delta V_{16\,/\,3} \geq 1$ V, the light band glides smoothly along the scale. With increasing voltage difference, the passage becomes more abrupt. With $\Delta V_{16\,/\,3}$, approx. 4 V, the light band jumps from diode to diode.

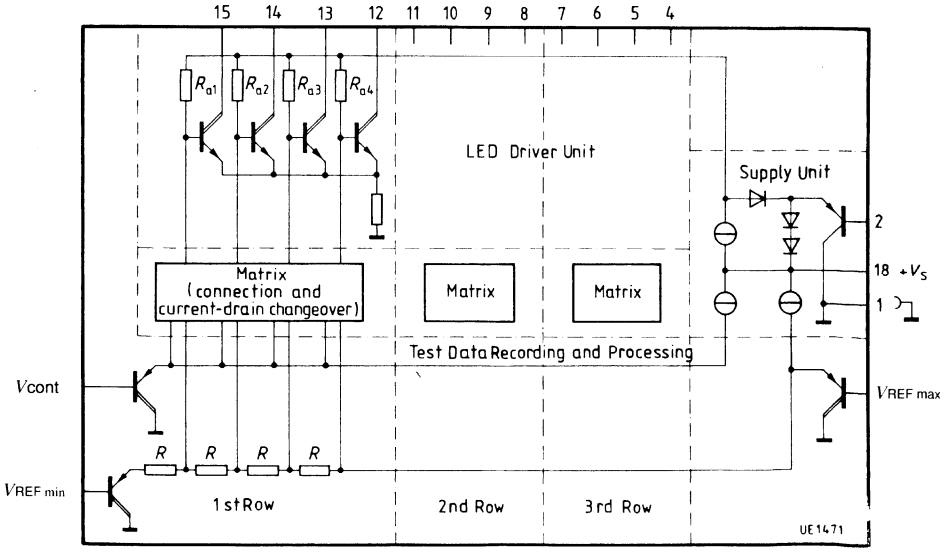
Each quartet must consist of identical diodes in order to maintain its functional characteristics.

It is therefore possible to design the first and third quartet as diodes emitting the color red and the second quartet as diodes emitting the color green to delineate a certain operational area.

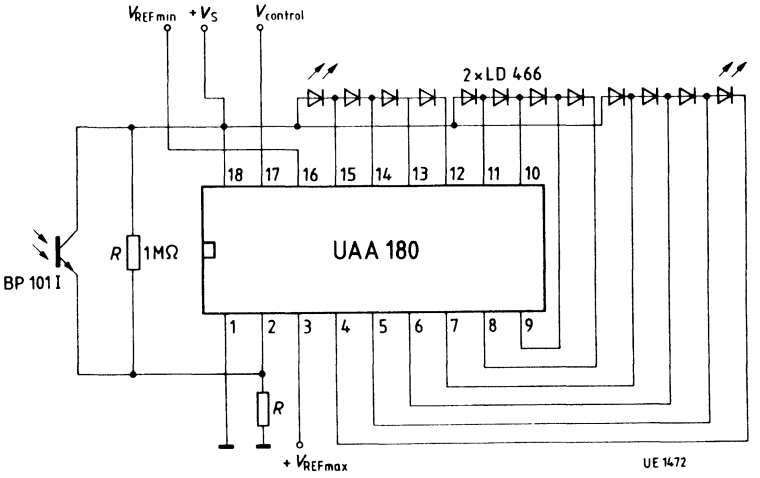
Pin 2 serves to determine the diode current. Corresponding to the desired light intensity, the forward current of the diodes is variably linear in the range I_f approx. 0 to 10 mA.

Application circuit 1 shows the possibility of designing this resistance to be adjustable by means of a phototransistor BP 101, in order to adapt the light intensity to changing ambient brightness. The adjusting range of the diode current lies between I_f approx. 5 mA (BP 101 not lit) and I_f approx. 10 mA (BP 101 fully lit). If pin 2 is open the diode current is 10 mA.

Block Diagram

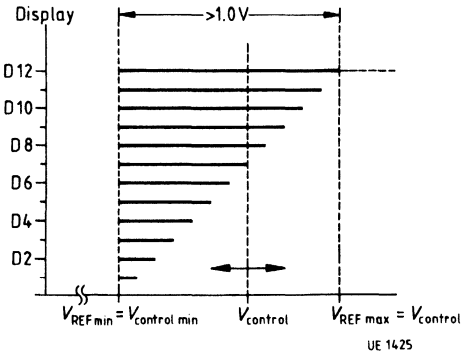


Application Circuit 1



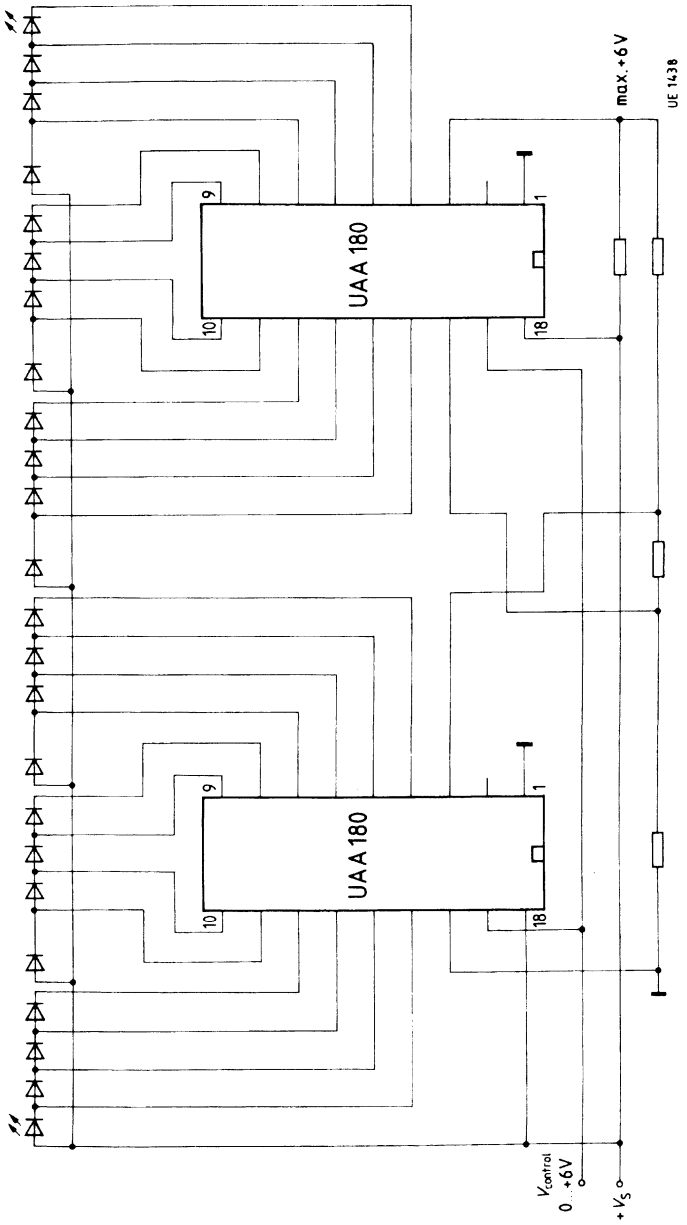
R = 2.2 kΩ...100 kΩ

LED display versus control current



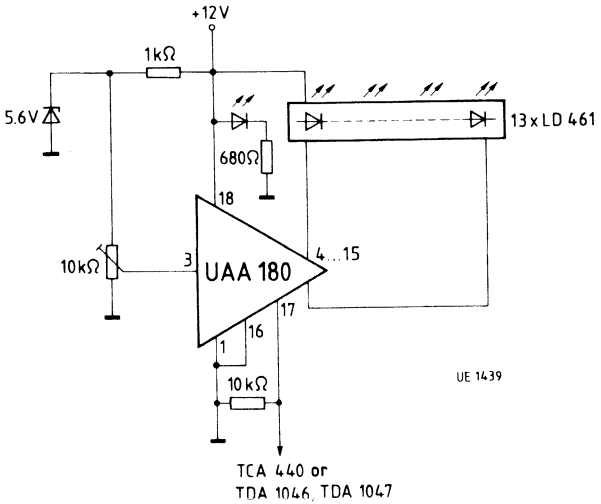
If a quartet does not need the full number of display diodes and if the first connected diodes shall be left luminous at full driving, bridges have to be inserted replacing the missing LEDs. Otherwise the first diodes of the quartet switch off when their display range is exceeded.

Application Circuit 2
for cascading several UAA 180 ICs (up to 7)



Application Circuit 3

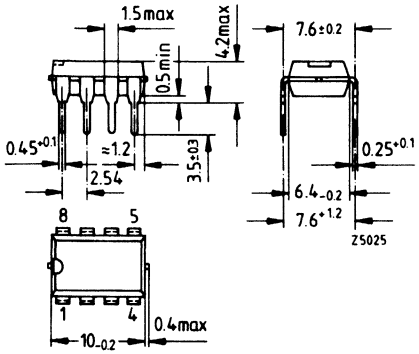
for field strength indication



Gehäusebauformen

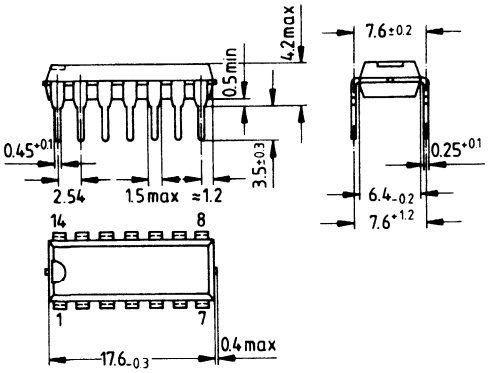
Package Outlines

Plastic Dual-in-Line Package, P-DIP-8
20 A 8 DIN 41870 T9



Approx. weight 0.7 g

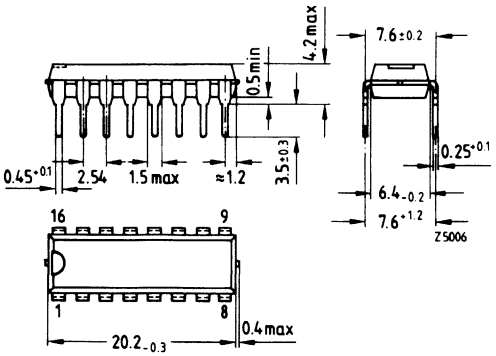
Plastic Dual-in-Line Package, P-DIP-14
20 A 14 DIN 41870 T9



Approx. weight 1.1 g

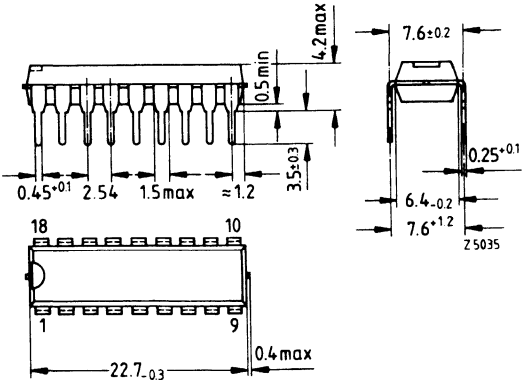
Dimensions in mm

Plastic Dual-in-Line Package, P-DIP-16
20 A 16 DIN 41870 T9



Approx. weight 1.2 g

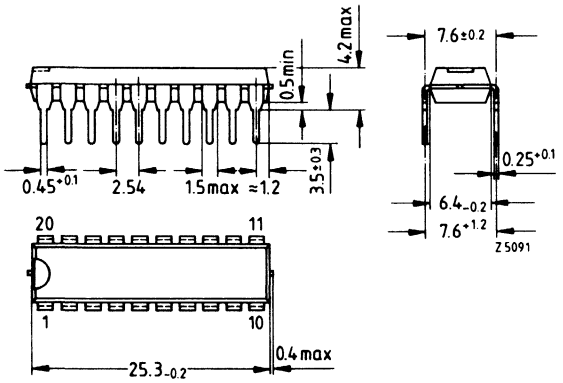
Plastic Dual-in-Line Package, P-DIP-18
20 A 18 DIN 41870 T9



Approx. weight 1.3 g

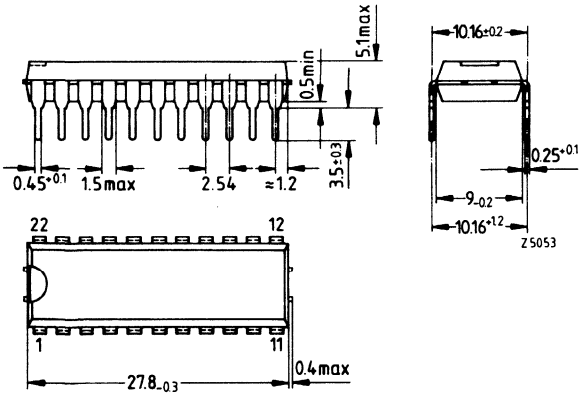
Dimensions in mm

Plastic Dual-in-Line Package, P-DIP-20
20 A 20 DIN 41870 T9



Approx. weight 1.5 g

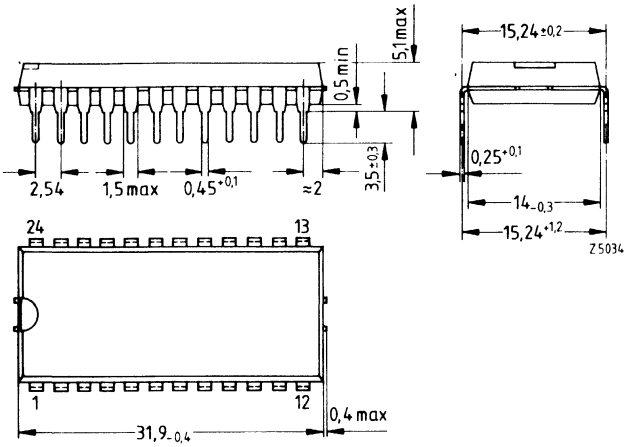
Plastic Dual-in-Line Package, P-DIP-22
20 D 22 DIN 41870 T11



Approx. weight 2.1 g

Dimensions in mm

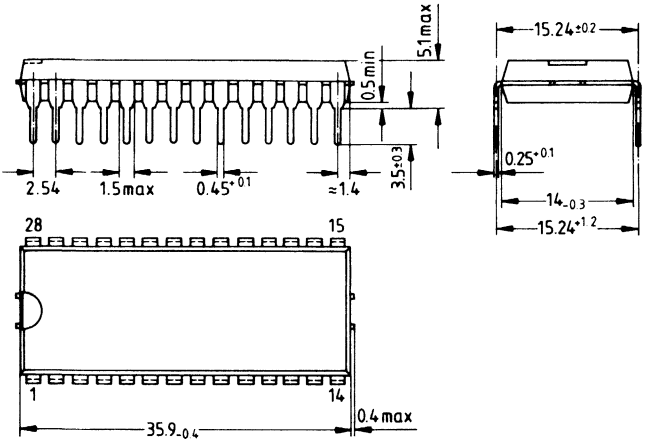
Plastic Dual-in-Line Package, P-DIP-24
20 B 24 DIN 41870 T10



Approx. weight 2.5 g

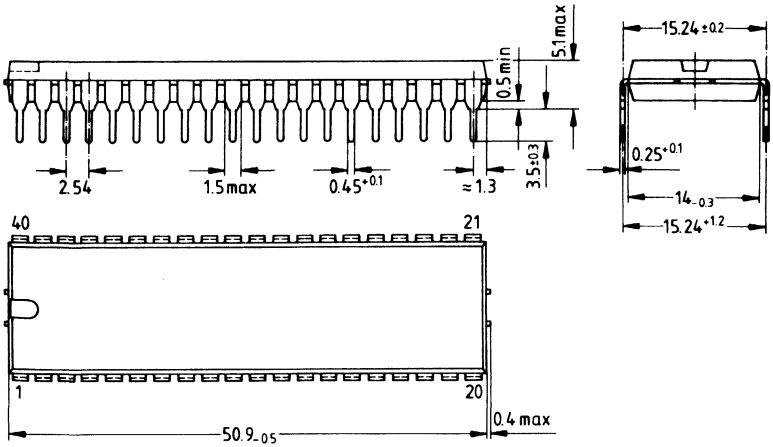
Dimensions in mm

Plastic Dual-in-Line Package, P-DIP-28
20 B 28 DIN 41870 T10



Approx. weight 3 g

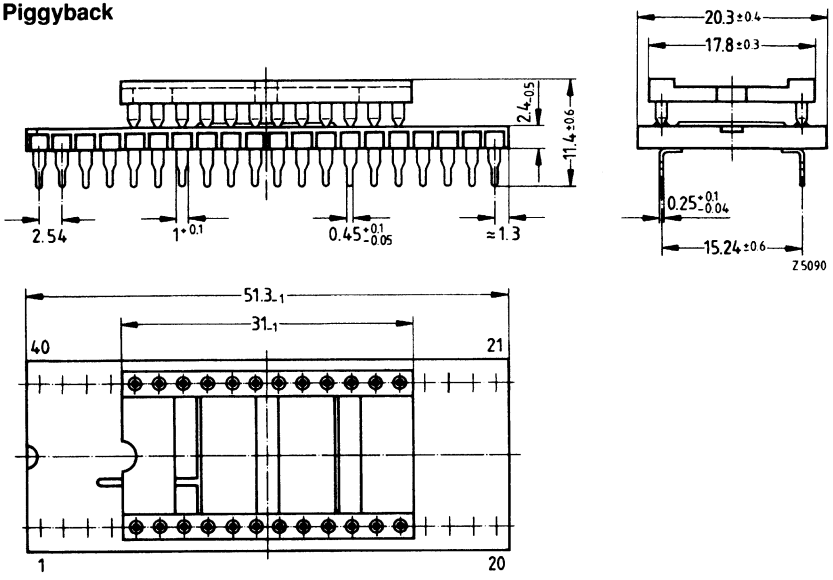
Plastic Dual-in-Line Package, P-DIP-40
20 B 40 DIN 41870 T10



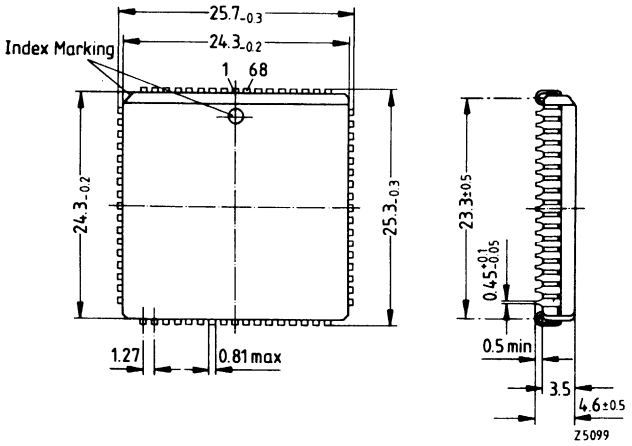
Approx. weight 5.9 g

Dimensions in mm

Piggyback



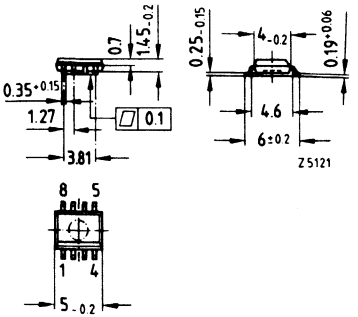
Plastic-Leaded Chip Carrier, PL-CC-68 (SMD)



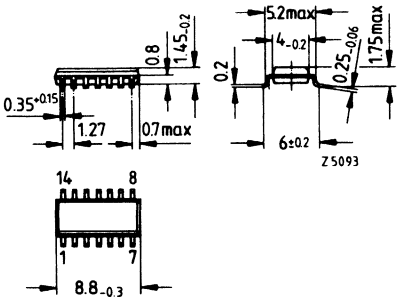
Dimensions in mm

SMD = Surface Mounted Device

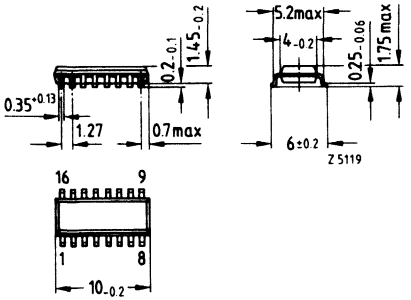
Miniature Plastic Dual-in-Line Package, P-MIP-8-G (SMD)
(Small Outlines)
(similar to P-DSO-8)
24 A 8 DIN 41870 T16



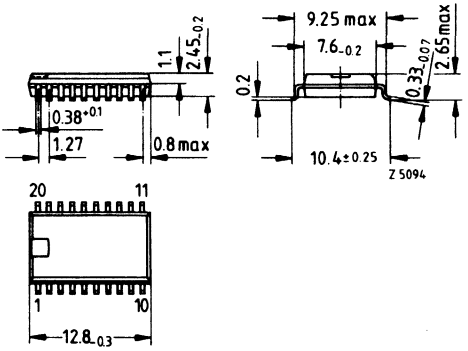
Miniature Plastic Dual-in-Line Package, P-DSO-14 (SMD)
(Small Outlines)
24 A 14 DIN 41870 T16



Miniature Plastic Dual-in-Line Package, P-DSO-16 (SMD)
(Small Outlines)
24 A 16 DIN 41870 T16



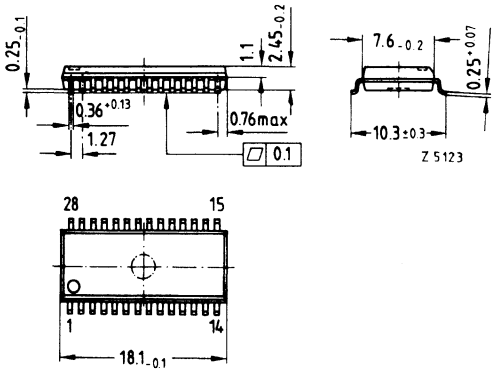
Miniature Plastic Dual-in-Line Package, P-DSO-20 (SMD)
(Small Outlines)
24 B 20 DIN 41870 T17



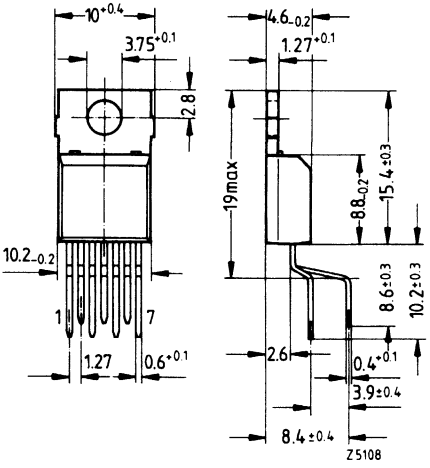
Dimensions in mm

SMD = Surface Mounted Device

Miniature Plastic Dual-in-Line Package, P-DSO-28 (SMD)
(Small Outlines)



Plastic Power Package, P-T66-7-H
(similar to TO-220)

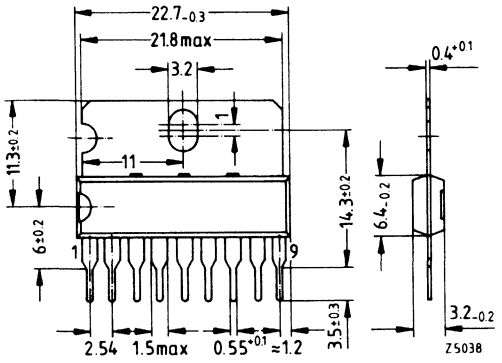


Approx. weight 2.1 g

Dimensions in mm

SMD = Surface Mounted Device

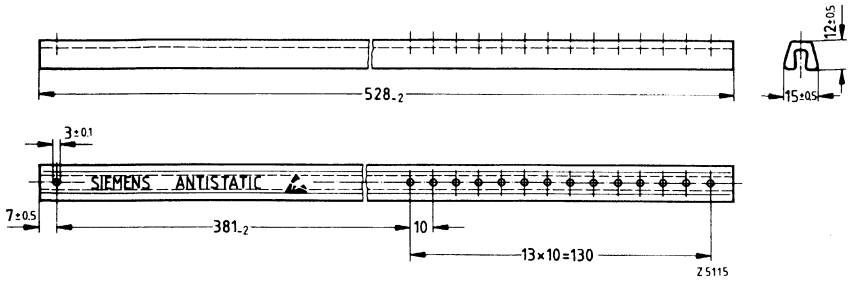
Plastic Single-in-Line Package, P-SIP-9



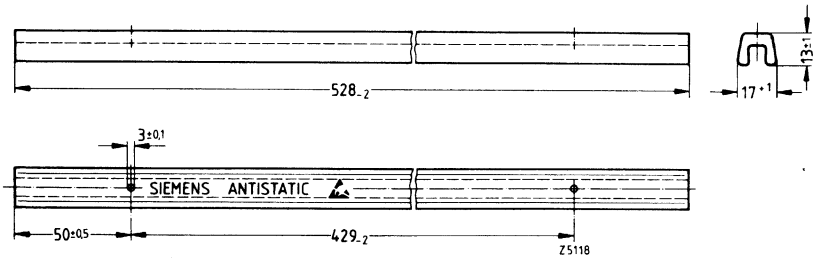
Approx. weight 1.9 g

Dimensions in mm

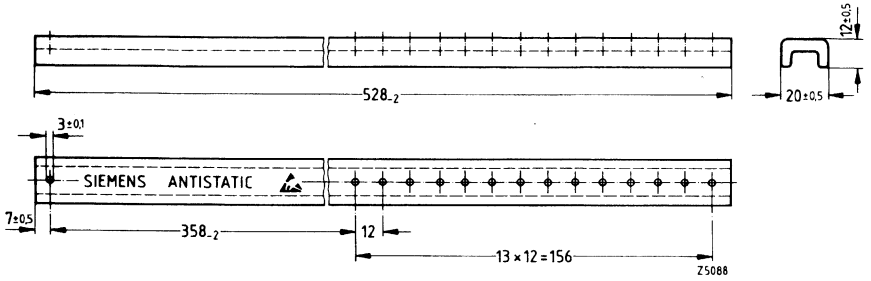
Packages: P-DIP-4; 6; 8; 14; 16; 18; 20



Packages: P-DIP-22



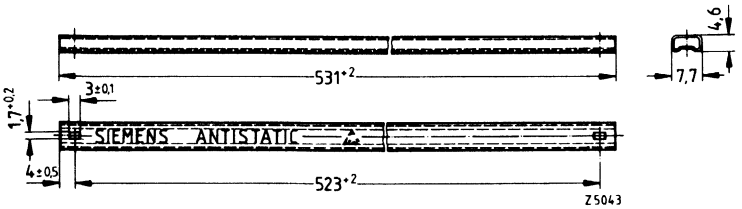
Packages: P-DIP-24; 28; 40



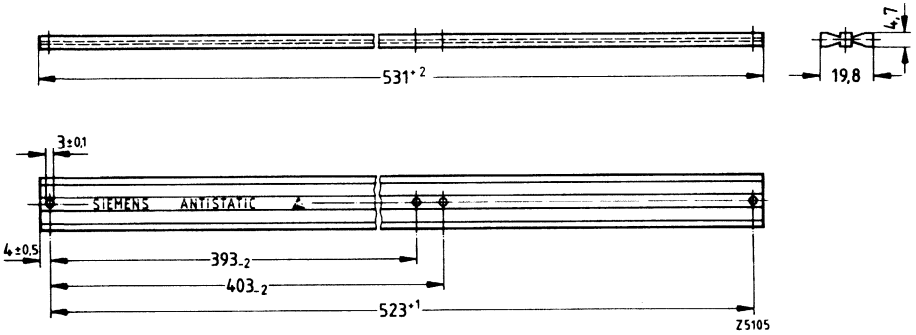
Dimensions in mm

Packaging Rails

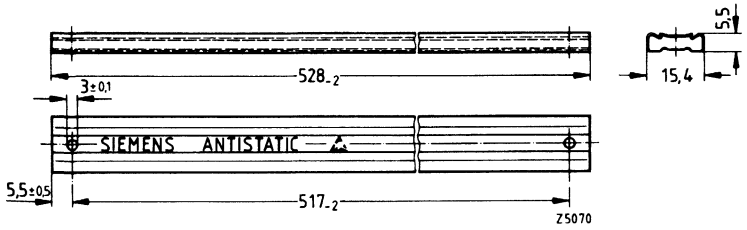
Packages: P-DSO-6; 8; 14; P-MIP-6-G; 8-G



Packages: P-MIP-6; 8

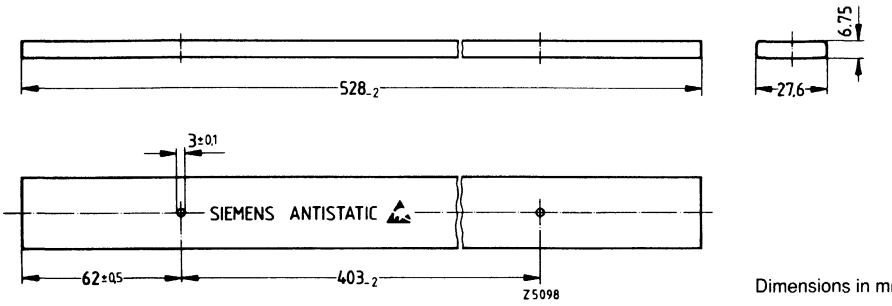


Packages: P-DSO-16; 18; 20; 24; 28; 40



Dimensions in mm

Packages: PL-CC-68



Dimensions in mm

Bereich Halbleiter – Anschriften
Literaturhinweise

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Information on Literature

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Titel Title	Bestell-Nr. Ordering code	DM
Datenbücher / Data Books		
Integrierte Schaltungen für die Unterhaltungselektronik ICs for Entertainment Electronics	B111-B6041-X-X-7400	20,-
Flicker-Free Television	B111-B6125-X-X-7600	15,-
Datenblätter / Data Sheets		
Picture-in-Picture System	B111-B6117-X-X-7600	10,-
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Dig. TV: Feature Box 88	B1-B3935	
Dig. TV: Feature Box 88	B1-B3935-X-X-7600	
Funktion und Anwendung des Sperrwandler-IC TDA 4605	B111-B6090	
Themenschriften / Special-Subject Brochures		
Schaltnetzteile TDA 4600	B1-B3672	
Lieferprogramme / Short form Catalog		
Integrierte Schaltungen, Speicher- und Mikrocomputer-Bausteine Integrated Circuits, Memory and Microcomputer Components	B192-B6337-X-X-7400	

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